

# PSMN1R3-30YL

N-channel 30 V 1.3 mΩ logic level MOSFET in LPAK

Rev. 02 — 25 June 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel MOSFET in LPAK package qualified to 150 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- Advanced TrenchMOS provides low  $R_{DS(on)}$  and low gate charge
- High efficiency gains in switching power convertors
- Improved mechanical and thermal characteristics
- LPAK provides maximum power density in a Power SO8 package

### 1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ;	[1]	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	121	W
$T_j$	junction temperature		-55	-	150	°C
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 100\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped	-	-	383	mJ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ;	-	9.3	-	nC
$Q_{G(tot)}$	total gate charge	$V_{DS} = 12\text{ V}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	46.6	-	nC

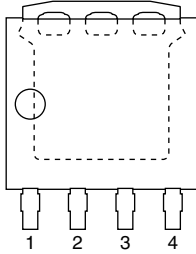
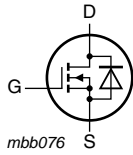
**Table 1. Quick reference ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 100\text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	-	1.8	mΩ
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 17</a>	-	1.04	1.3	mΩ

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>SOT1023 (LFAK2)</b></p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
PSMN1R3-30YL	LFAK2	Plastic single-end surface-mounted package (LFAK2); 4 leads	SOT1023

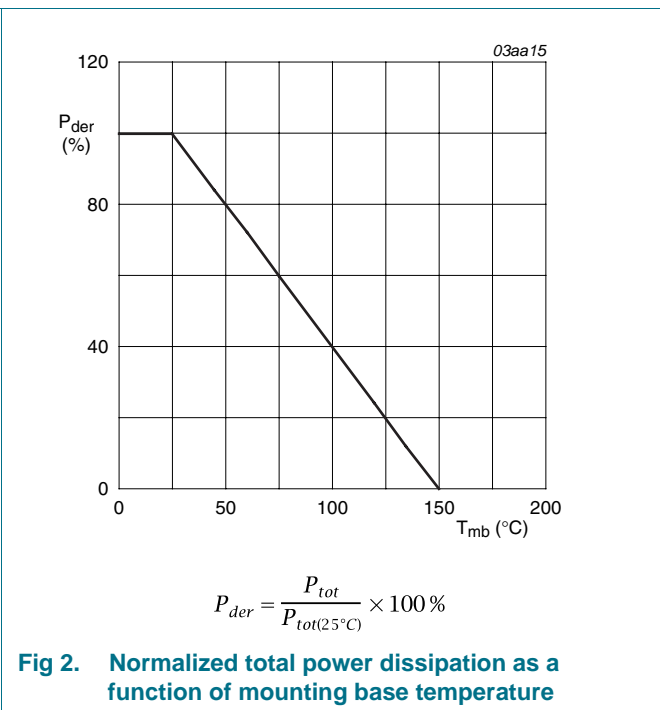
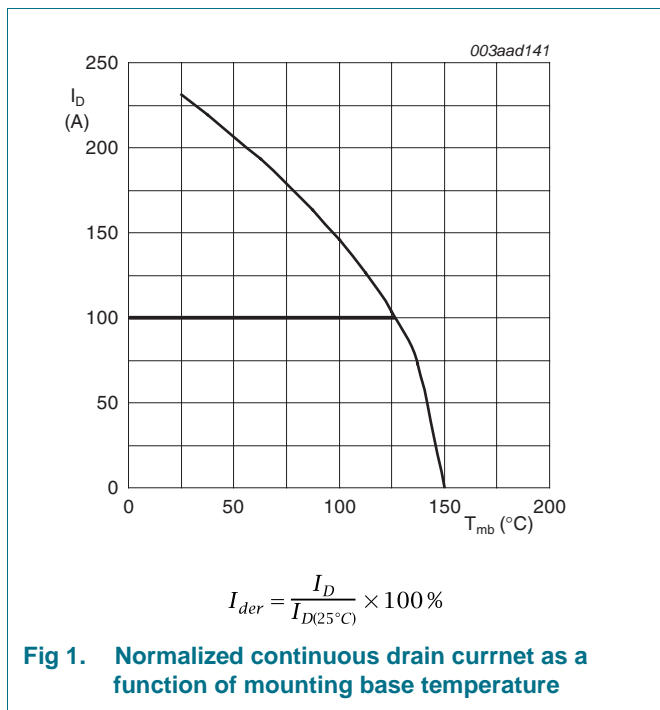
## 4. Limiting values

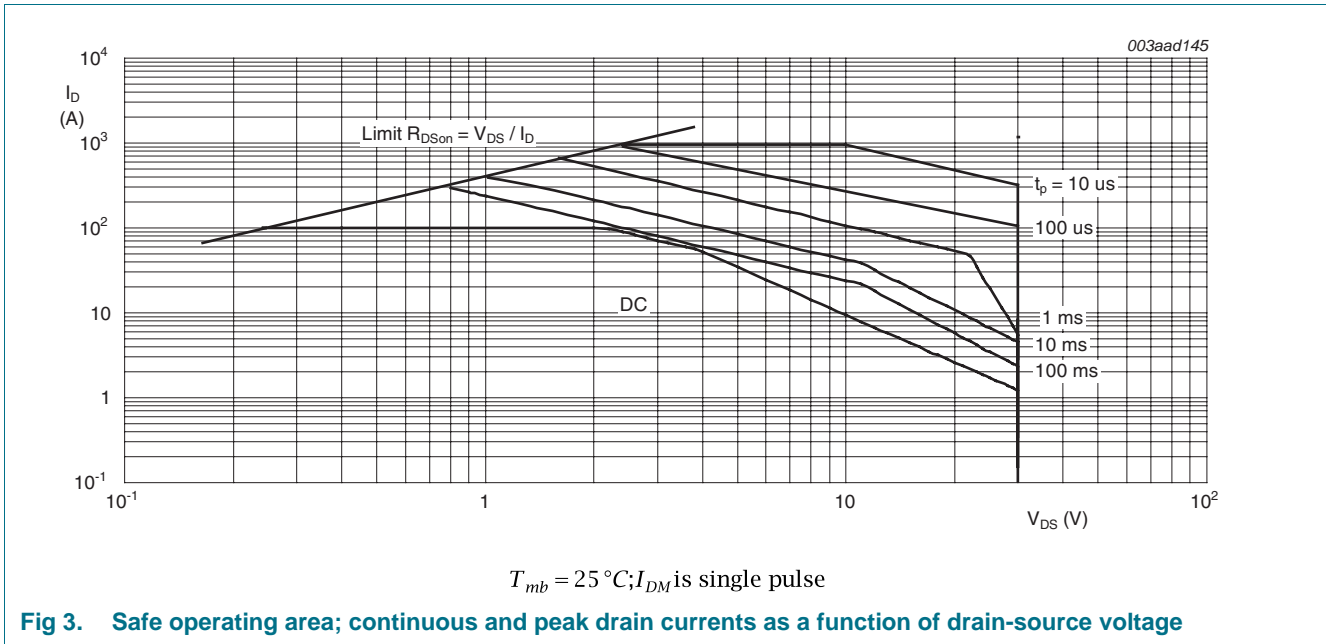
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C	-	30	V
V <sub>DGR</sub>	drain-gate voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C; R <sub>GS</sub> = 20 kΩ	-	30	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see <a href="#">Figure 1</a>	[1]	100	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 1</a>	[1]	100	A
I <sub>DM</sub>	peak drain current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 3</a>	-	923	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	121	W
T <sub>stg</sub>	storage temperature		-55	150	°C
T <sub>j</sub>	junction temperature		-55	150	°C
T <sub>slid(M)</sub>	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C;	[1]	100	A
I <sub>SM</sub>	peak source current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>mb</sub> = 25 °C	-	923	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; unclamped	-	383	mJ

[1] Continuous current is limited by package.

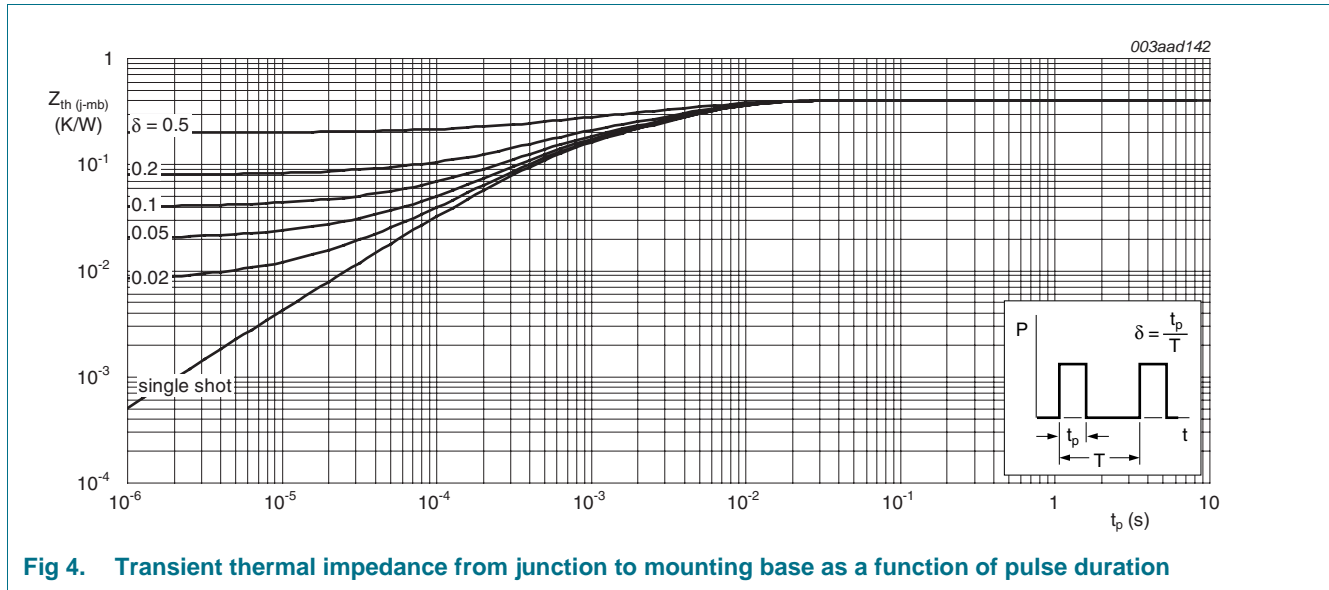




## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.4	1.03	K/W



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

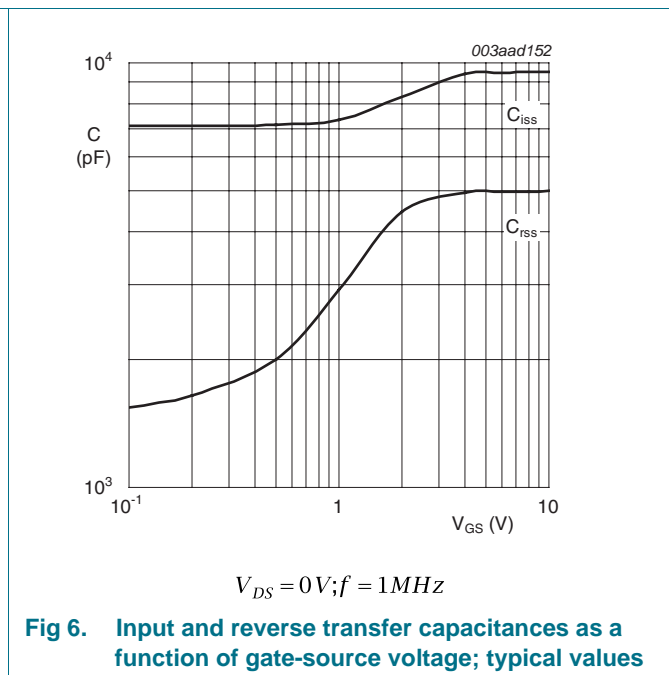
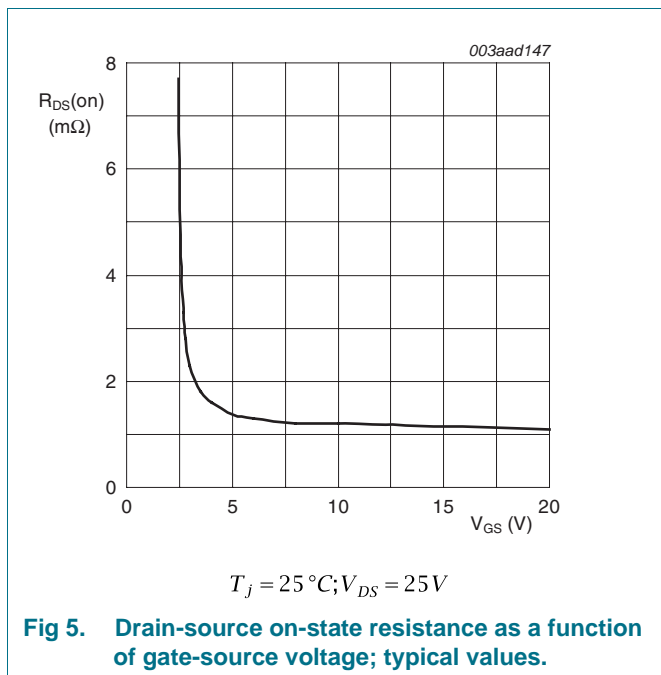
## 6. Characteristics

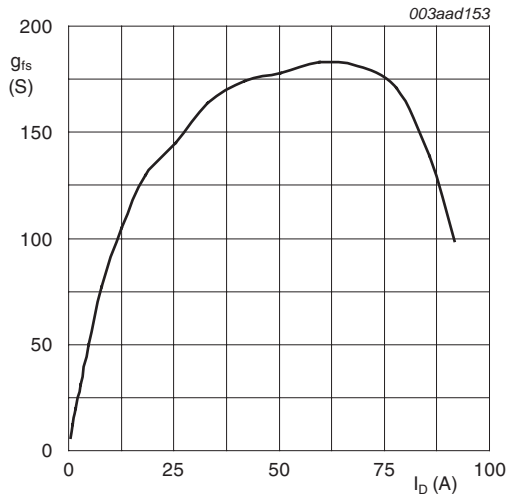
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	1.3	1.7	2.15	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	0.65	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 17</a>	-	1.43	1.95	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	-	1.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	1.9	2.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 17</a>	-	1.04	1.3	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	0.89	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	100	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	90	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	46.6	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	17.9	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 13</a>	-	11	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	6.9	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	9.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 12 \text{ V};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	2.53	-	V
$C_{iss}$	input capacitance	$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 15</a>	-	6227	-	pF
$C_{oss}$	output capacitance		-	1415	-	pF
$C_{rss}$	reverse transfer capacitance		-	619	-	pF

Table 6. Characteristics ...continued

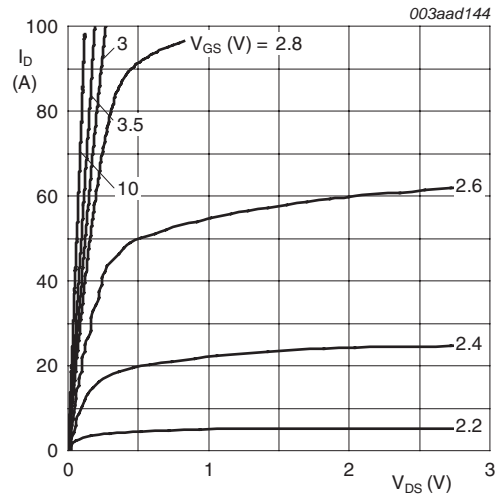
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.5\ \Omega; V_{GS} = 4.5\text{ V};$	-	64	-	ns
$t_r$	rise time	$R_{G(ext)} = 5.6\ \Omega$	-	108	-	ns
$t_{d(off)}$	turn-off delay time		-	106	-	ns
$t_f$	fall time		-	52	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 16</a>	-	0.88	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A/s}; V_{GS} = 0\text{ V};$	-	46	-	ns
$Q_r$	recovered charge	$V_{DS} = 20\text{ V}$	-	53	-	nC





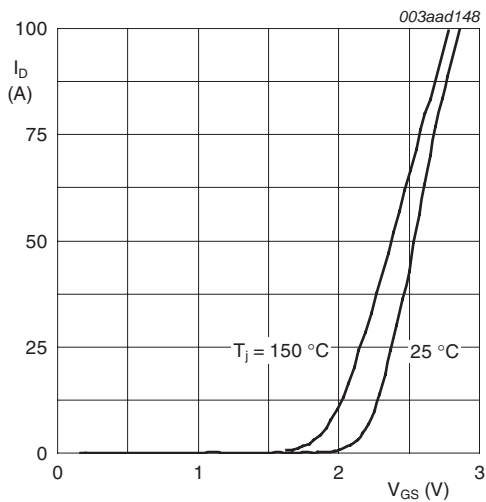
$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

Fig 7. Forward transconductance as a function of drain current; typical values



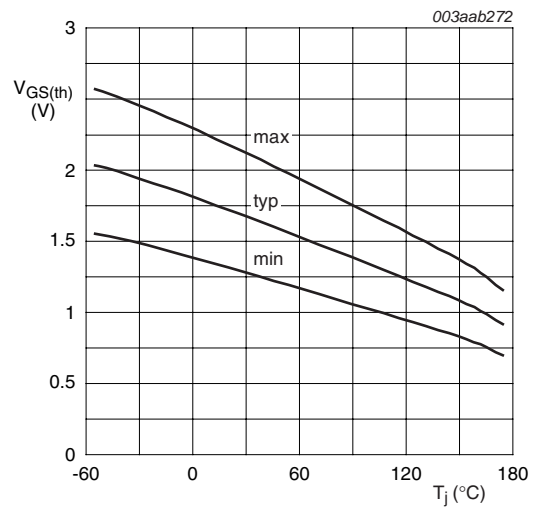
$T_j = 25^\circ\text{C}$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



$V_{DS} > I_D \times R_{DSon}$

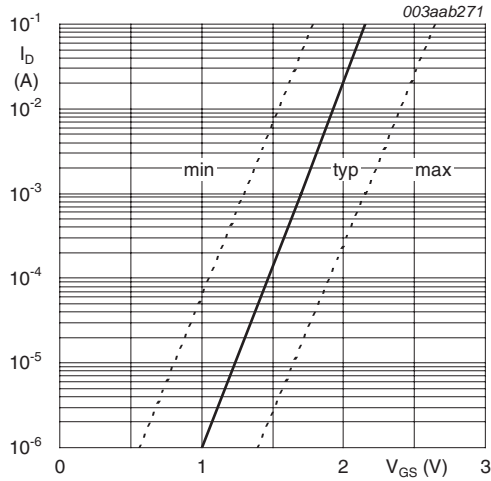
Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$I_D = 1\text{mA}; V_{DS} = V_{GS}$

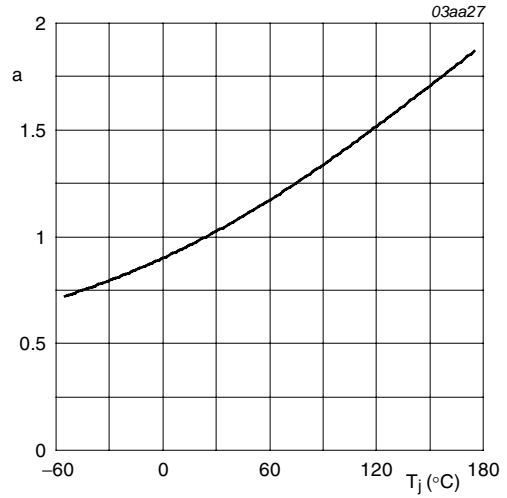
Fig 10. Gate-source threshold voltage as a function of junction temperature





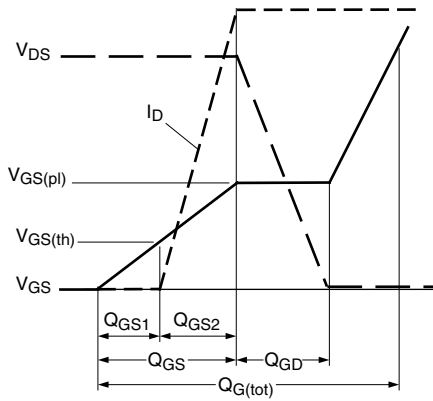
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

**Fig 11. Sub-threshold drain current as a function of gate-source voltage**

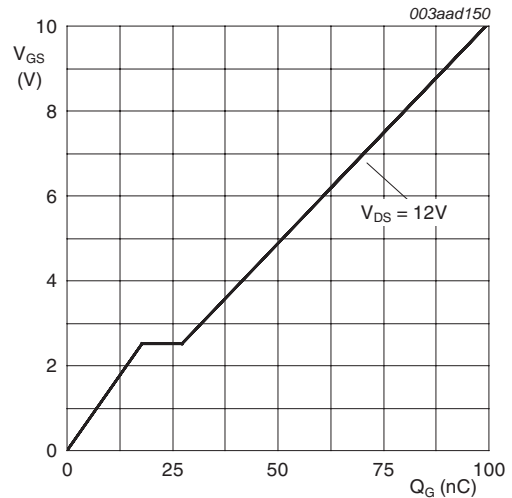


$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

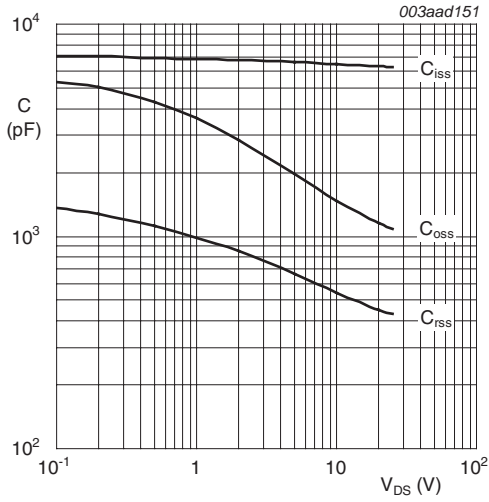


**Fig 13. Gate charge waveform definitions**



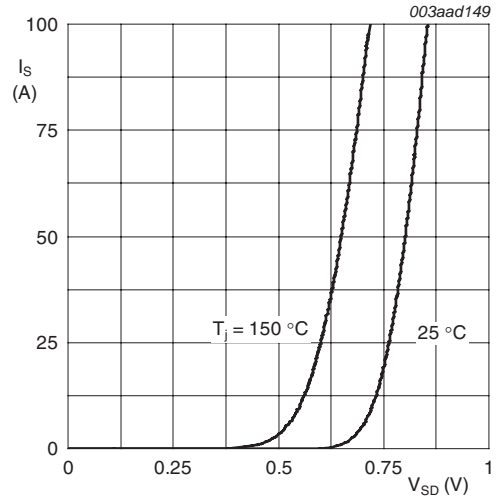
$I_D = 25\text{ A}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**



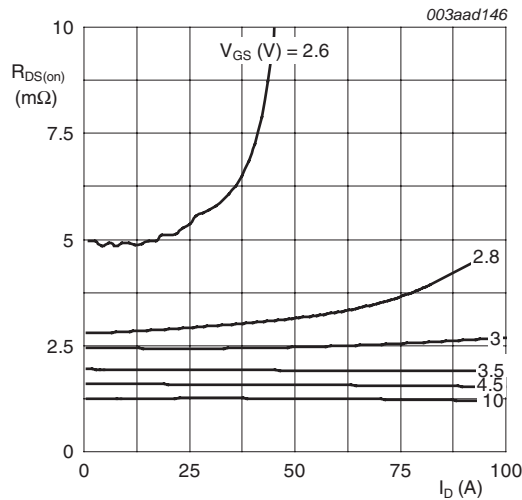
$V_{GS} = 0V; f = 1MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig 16. Source current as a function of source-drain voltage; typical values



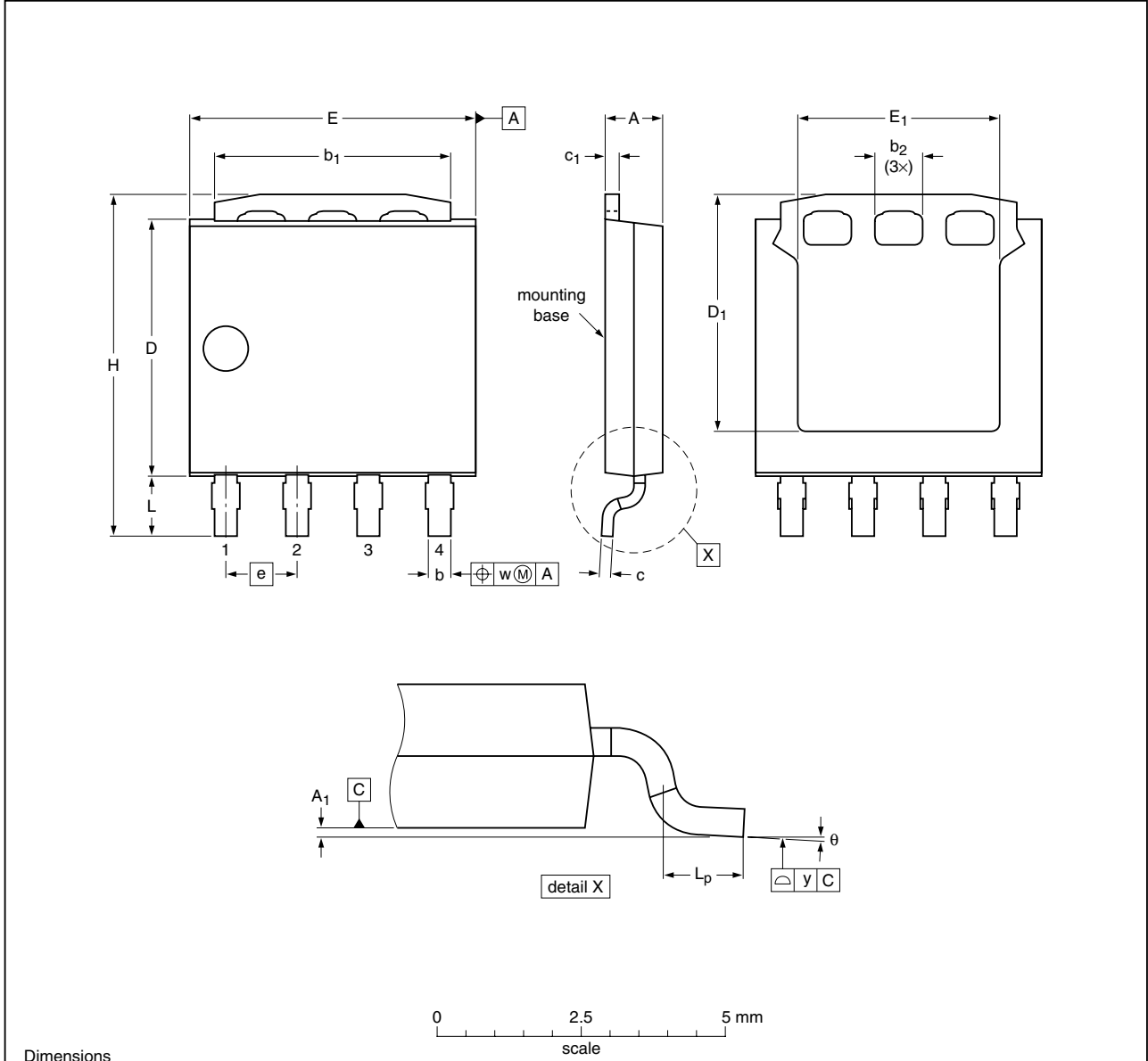
$T_j = 25 °C$

Fig 17. Drain-source on-state resistance as a function of drain current; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK2); 4 leads

SOT1023



Dimensions

Unit	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	c <sub>1</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>p</sub>	w	y	θ
max	1.10	0.15	0.50	4.41		0.25	0.30	4.70	4.45	5.30	3.7		6.2	1.3	0.85			8°
nom				0.85								1.27				0.25	0.1	
min	0.95	0.00	0.35	3.62		0.19	0.24	4.45		4.95	3.5		5.9	0.8	0.40			0°

Note

1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1023\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1023					08-10-13 09-05-26

Fig 18. Package outline SOT1023; Package outline

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN1R3-30YL_2	20090625	Product data sheet	-	PSMN2R3-30YL_1
Modifications:		<ul style="list-style-type: none"><li>• Status changed from objective to product.</li><li>• Various changes to content.</li></ul>		
PSMN1R3-30YL_1	20090528	Objective data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 25 June 2009

Document identifier: PSMN1R3-30YL\_2