LTC6992-1/-2/-3/-4

TimerBlox Voltage-Controlled Pulse Width Modulator (PWM)

FEATURES

- **Pulse Width Modulation (PWM) Controlled by Simple 0V to 1V Analog Input**
- **Four Available Options Define Duty Cycle Limits**
  - **Minimum Duty Cycle at 0% or 5%**
  - **Maximum Duty Cycle at 95% or 100%**
- **Frequency Range: 3.81Hz to 1MHz**
- Single Resistor Programs Frequency with <2.4% Maximum Error
- PWM Duty Cycle Error <4.5% Maximum
- Frequency Modulation (VCO) Capability
- 2.25V to 5.5V Single Supply Operation
- 115µA Supply Current at 100kHz
- 500µs Start-Up Time
- CMOS Output Driver Sources/Sinks 20mA
- –40°C to 125°C Operating Temperature Range
- Available in Low Profile (1mm) SOT-23 (ThinSOT™) and 2mm × 3mm DFN

APPLICATIONS

- LED Dimming Control
- PWM Servo Loops
- High Vibration, High Acceleration Environments
- Portable and Battery-Powered Equipment

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DESCRIPTION

The LTC®6992 is a silicon oscillator with an easy-to-use analog voltage-controlled pulse width modulation (PWM) capability. The LTC6992 is part of the TimerBlox™ family of versatile silicon timing devices.

A single resistor, R_{SET}, programs the LTC6992's internal master oscillator frequency. The output frequency is determined by this master oscillator and an internal frequency divider, N_{DIV}, programmable to eight settings from 1 to 16384.

$$f_{OUT} = \frac{1MHz}{N_{DIV}} \bullet \frac{50k\Omega}{R_{SET}}, N_{DIV} = 1,4,16 \ldots 16384$$

Applying a voltage between 0V and 1V on the MOD pin sets the duty cycle, according to the following formula:

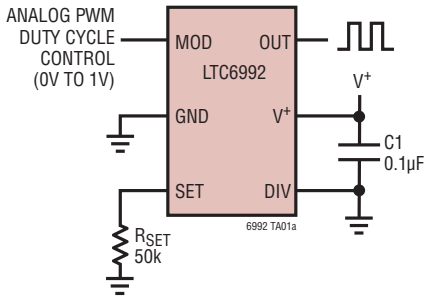
$$\text{Duty Cycle} = \frac{V_{MOD}}{0.8 \bullet V_{SET}} - \frac{1}{8} \cong \frac{V_{MOD} - 100mV}{800mV}$$

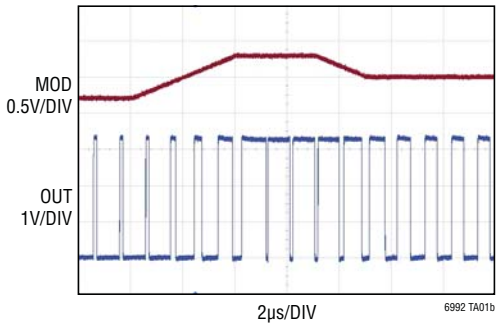
The four versions differ in their minimum/maximum duty cycle. Note that a minimum duty cycle limit of 0% or maximum duty cycle limit of 100% allows oscillations to stop at the extreme duty cycle settings.

DEVICE NAME	PWM DUTY CYCLE RANGE	OUTPUT DUTY CYCLE LIMITS	
		MIN	MAX
LTC6992-1	0% to 100%	GND	V+
LTC6992-2	5% to 95%		
LTC6992-3	0% to 95%	GND	
LTC6992-4	5% to 100%		V+

TYPICAL APPLICATION

1MHz Pulse Width Modulator

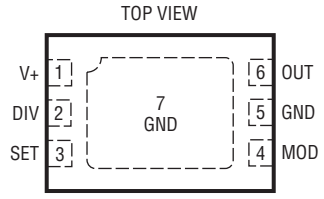




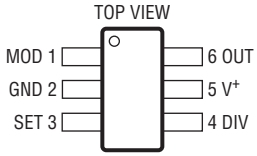
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+) to GND 6V
Maximum Voltage On Any Pin
.....$(GND - 0.3V) \le V_{PIN} \le (V^+ + 0.3V)$
Operating Temperature Range (Note 2)
LTC6992C ..... 0°C to 70°C
LTC6992I .....–40°C to 85°C
LTC6992H..... –40°C to 125°C
Specified Temperature Range (Note 3)
LTC6992C ..... 0°C to 70°C
LTC6992I .....–40°C to 85°C
LTC6992H..... –40°C to 125°C
Junction Temperature ..... 150°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PIN CONFIGURATION



DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 64°C/W, θ_{JC} = 10.6°C/W
EXPOSED PAD (PIN 7) IS GND, PCB CONNECTION IS OPTIONAL



S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 230°C/W, θ_{JC} = 51°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6992CDCB6-1#PBF	LTC6992CDCB6-1#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB6-1#PBF	LTC6992IDCB6-1#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6992HDCB6-1#PBF	LTC6992HDCB6-1#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6992CS6-1#PBF	LTC6992CS6-1#TRPBF	XXXX	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-1#PBF	LTC6992IS6-1#TRPBF	XXXX	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6992HS6-1#PBF	LTC6992HS6-1#TRPBF	XXXX	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6992CDCB6-2#PBF	LTC6992CDCB6-2#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB6-2#PBF	LTC6992IDCB6-2#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6992HDCB6-2#PBF	LTC6992HDCB6-2#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6992CS6-2#PBF	LTC6992CS6-2#TRPBF	XXXX	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-2#PBF	LTC6992IS6-2#TRPBF	XXXX	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6992HS6-2#PBF	LTC6992HS6-2#TRPBF	XXXX	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6992CDCB6-3#PBF	LTC6992CDCB6-3#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB6-3#PBF	LTC6992IDCB6-3#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6992HDCB6-3#PBF	LTC6992HDCB6-3#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6992CS6-3#PBF	LTC6992CS6-3#TRPBF	XXXX	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-3#PBF	LTC6992IS6-3#TRPBF	XXXX	6-Lead Plastic TSOT-23	–40°C to 85°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6992HS6-3#PBF	LTC6992HS6-3#TRPBF	XXXX	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6992CDCB6-4#PBF	LTC6992CDCB6-4#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB6-4#PBF	LTC6992IDCB6-4#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6992HDCB6-4#PBF	LTC6992HDCB6-4#TRPBF	XXXX	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6992CS6-4#PBF	LTC6992CS6-4#TRPBF	XXXX	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-4#PBF	LTC6992IS6-4#TRPBF	XXXX	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6992HS6-4#PBF	LTC6992HS6-4#TRPBF	XXXX	6-Lead Plastic TSOT-23	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 2.25V to 5.5V, V_{MOD} = 0V to V_{SET}, DIVCODE = 0 to 15 (N_{DIV} = 1 to 16,384), R_{SET} = 50k to 800k, R_{LOAD} = 5k, C_{LOAD} = 5pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillation Frequency							
f_{OUT}	Output Frequency			3.81		1000000	Hz
Δf_{OUT}	Frequency Accuracy (Note 4)	3.81Hz ≤ f_{OUT} ≤ 1MHz	 ●		±0.8	±1.7 ±2.4	% %
$\Delta f_{OUT}/\Delta T$	Frequency Drift Over Temperature		●		±0.005		%/°C
$\Delta f_{OUT}/\Delta V^+$	Frequency Drift Over Supply	V^+ = 4.5V to 5.5V V^+ = 2.25V to 4.5V	● ●		0.25 0.08	0.65 0.18	%/V %/V
	Period Jitter (Note 11)	N_{DIV} = 1			1.2		$\%_{P-P}$
		N_{DIV} = 4			0.4 0.07		$\%_{P-P}$ $\%_{RMS}$
		N_{DIV} = 16			0.15 0.022		$\%_{P-P}$ $\%_{RMS}$
	Long-Term Stability of Output Frequency (Note 9)				TBD		ppm/√kHz
BW_{FM}	Frequency Modulation Bandwidth				TBD		kHz
$t_{S,FM}$	Frequency Change Settling Time (Note 10)	$t_{MASTER} = t_{OUT}/N_{DIV}$			TBD		µs
Pulse Width Modulation							
ΔD	PWM Duty Cycle Accuracy	V_{MOD} = 0.2 • V_{SET} to 0.8 • V_{SET} V_{MOD} < 0.2 • V_{SET} or V_{MOD} > 0.8 • V_{SET}	● ●		±1.5 ±2.0	±4.5 ±4.9	% %
D_{MAX}	Maximum Duty Cycle Limit	LTC6992-1/LTC6992-3, POL = 0, V_{MOD} = 1V	●	100			%
		LTC6992-2/LTC6992-4, POL = 0, V_{MOD} = 1V	●	90.5	95	99	%
D_{MIN}	Minimum Duty Cycle Limit	LTC6992-1/LTC6992-4, POL = 0, V_{MOD} = 0V	●			0	%
		LTC6992-2/LTC6992-3, POL = 0, V_{MOD} = 0V	●	1	5	9.5	%
BW_{PWM}	PWM Duty Cycle Bandwidth				TBD		kHz
$t_{S,PWM}$	Duty Cycle Setting Time (Note 6)	$t_{MASTER} = t_{OUT}/N_{DIV}$			TBD		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 2.25V to 5.5V, V_{MOD} = 0V to V_{SET}, DIVCODE = 0 to 15 (N_{DIV} = 1 to 16,384), R_{SET} = 50k to 800k, R_{LOAD} = 5k, C_{LOAD} = 5pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supply								
V^+	Operating Supply Voltage Range			●	2.25		5.5	V
	Power-On Reset Voltage			●			1.95	V
I_S	Supply Current	R_L = ∞, R_{SET} = 50k, N_{DIV} = 1	V^+ = 5.5V	●		365	450	µA
			V^+ = 2.25V	●		225	285	µA
		R_L = ∞, R_{SET} = 50k, N_{DIV} = 4	V^+ = 5.5V	●		350	420	µA
			V^+ = 2.25V	●		225	280	µA
		R_L = ∞, R_{SET} = 50k, $N_{DIV} \geq 16$	V^+ = 5.5V	●		325	390	µA
			V^+ = 2.25V	●		215	265	µA
		R_L = ∞, R_{SET} = 800k, N_{DIV} = 1 to 16, 384	V^+ = 5.5V	●		120	170	µA
			V^+ = 2.25V	●		105	150	µA
Analog Inputs								
V_{SET}	Voltage at SET Pin			●	0.97	1.00	1.03	V
$\Delta V_{SET}/\Delta T$	V_{SET} Drift Over Temperature			●		±75		µV/°C
R_{SET}	Frequency-Setting Resistor			●	50		800	kΩ
	MOD Pin Input Capacitance					2.5		pF
	MOD Pin Input Current			●			±10	nA
$V_{MOD,HI}$	V_{MOD} Voltage for Maximum Duty Cycle	LTC6992-1/LTC6992-4, POL = 0, D = 100% LTC6992-2/LTC6992-3, POL = 0, D = 95%		● 		0.90•V_{SET} 0.86•V_{SET}	0.936•V_{SET}	V V
$V_{MOD,LO}$	V_{MOD} Voltage for Minimum Duty Cycle	LTC6992-1/LTC6992-3, POL = 0, D = 0% LTC6992-2/LTC6992-4, POL = 0, D = 5%		●	0.064•V_{SET}	0.10•V_{SET} 0.14•V_{SET}		V V
V_{DIV}	DIV Pin Voltage			●	0		V^+	V
$\Delta V_{DIV}/\Delta V^+$	DIV Pin Valid Code Range (Note 5)	Deviation from Ideal V_{DIV}/V^+ = (DIVCODE + 0.5)/16		●			±1.5	%
	DIV Pin Input Current			●			±10nA	
Digital Output								
$I_{OUT(MAX)}$	Output Output Current			●		±20		mA
V_{OH}	High Level Output Voltage	V^+ = 5.5V	I_{OUT} = –1mA I_{OUT} = –16mA	● ●	5.45 4.84	5.48 5.15		V V
		V^+ = 3.3V	I_{OUT} = –1mA I_{OUT} = –10mA	● ●	3.24 2.75	3.27 2.99		V V
		V^+ = 2.25V	I_{OUT} = –1mA I_{OUT} = -8mA	● ●	2.17 1.58	2.21 1.88		V V
V_{OL}	Low Level Output Voltage	V^+ = 5.5V	I_{OUT} = 1mA I_{OUT} = 16mA	● ●		0.02 0.26	0.04 0.54	V V
		V^+ = 3.3V	I_{OUT} = 1mA I_{OUT} = 10mA	● ●		0.03 0.22	0.05 0.46	V V
		V^+ = 2.25V	I_{OUT} = 1mA I_{OUT} = 8mA	● ●		0.03 0.26	0.07 0.54	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 2.25V to 5.5V, V_{MOD} = 0V to V_{SET}, DIVCODE = 0 to 15 (N_{DIV} = 1 to 16,384), R_{SET} = 50k to 800k, R_{LOAD} = 5k, C_{LOAD} = 5pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_r	Output Rise Time (Note 8)	V^+ = 5.5V V^+ = 3.3V V^+ = 2.25V			1.1 1.7 2.7		ns ns ns
t_f	Output Fall Time (Note 8)	V^+ = 5.5V V^+ = 3.3V V^+ = 2.25V			1.0 1.6 2.4		ns ns ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6992C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 3: The LTC6992C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6992C is designed, characterized and expected to meet specified performance from –40°C to 85°C but it is not tested or QA sampled at these temperatures. The LTC6992I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6992H is guaranteed to meet specified performance from –40°C to 125°C.

Note 4: Frequency accuracy is defined as the deviation from the f_{OUT} equation, assuming R_{SET} is used to program the frequency.

Note 5: See Operation section, Table 1 and Figure 2 for a full explanation of how the DIV pin voltage selects the value of DIVCODE.

Note 6: Duty cycle setting time is the is the amount of time required for the output to settle within ±1% of the final duty cycle after a ±10% change in the setting (±80mV step in V_{MOD}).

Note 7: To conform to the Logic IC Standard, current out of a pin is arbitrarily given a negative value.

Note 8: Output rise and fall times are measured between the 10% and the 90% power supply levels with 5pF output load. These specifications are based on characterization.

Note 9: Long term drift on silicon oscillators is primarily due to the movement of ions and impurities within the silicon and is tested at 30°C under otherwise nominal operating conditions. Long term drift is specified as ppm/$\sqrt{kHr}$ due to the typically non-linear nature of the drift. To calculate drift for a set time period, translate that time into thousands of hours, take the square root and multiply by the typical drift number. For instance, a year is 8.77kHr and would yield a drift of 888ppm at 300ppm/$\sqrt{kHr}$. Drift without power applied to the device may be approximated as 1/10th of the drift with power, or 30ppm/$\sqrt{kHr}$ for a 300ppm/$\sqrt{kHr}$ device.

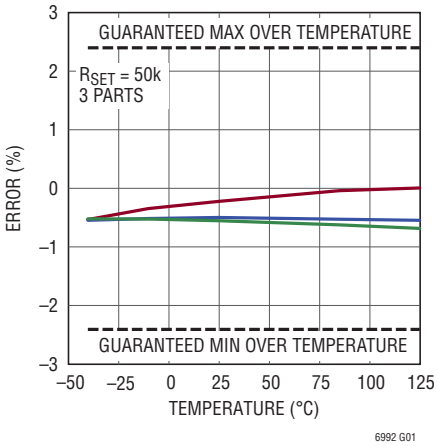
Note 10: Frequency change settling time is the amount of time required for the output to settle within ±1% of the final frequency after a 0.5x or 2x change in I_{SET}.

Note 11: Jitter is the ratio of the peak-to-peak deviation of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

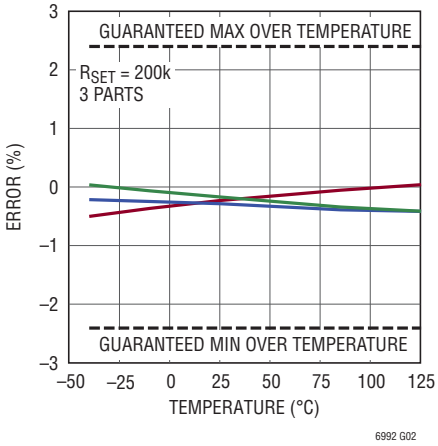
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

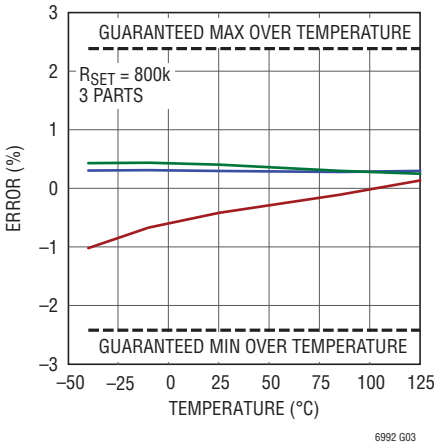
Frequency Error vs Temperature



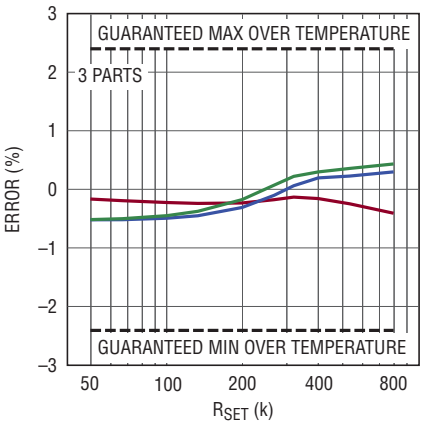
Frequency Error vs Temperature



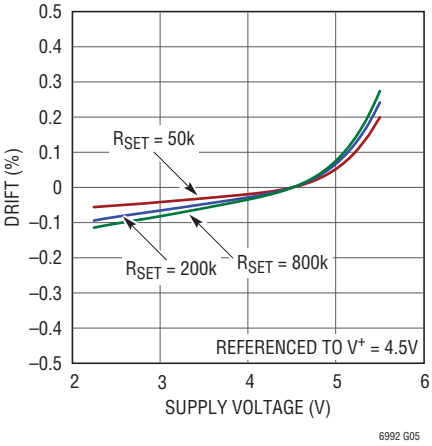
Frequency Error vs Temperature



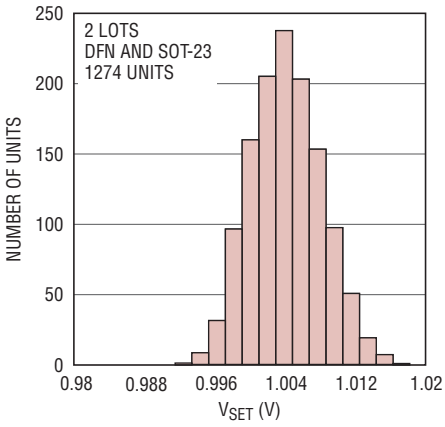
Frequency Error vs R_{SET}



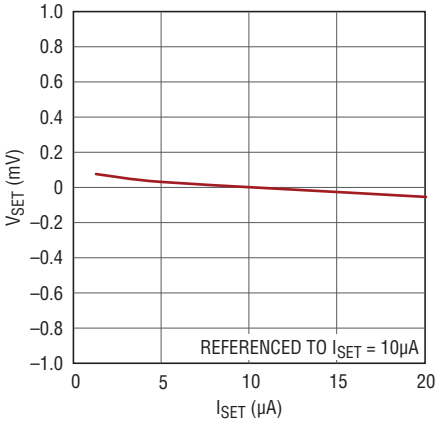
Frequency Drift vs Supply Voltage



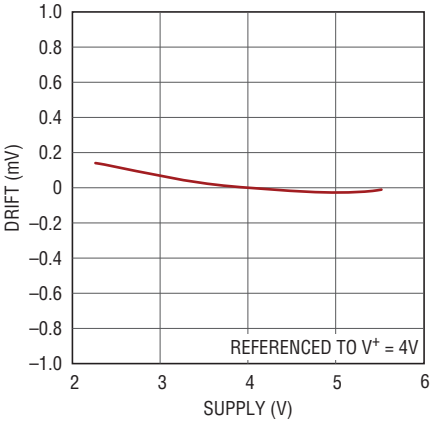
Typical V_{SET} Distribution



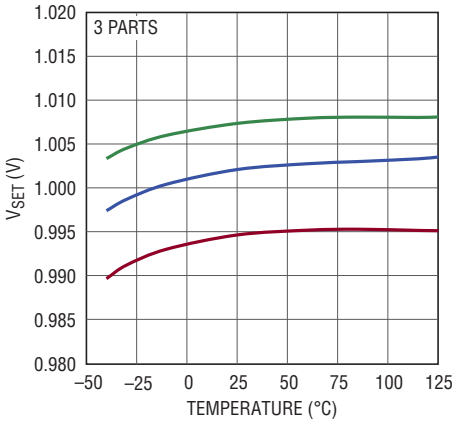
V_{SET} Drift vs I_{SET}



V_{SET} Drift vs Supply



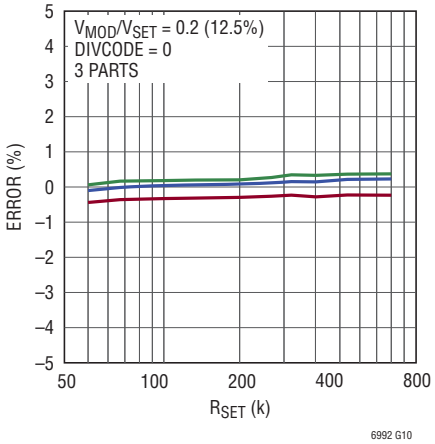
V_{SET} vs Temperature



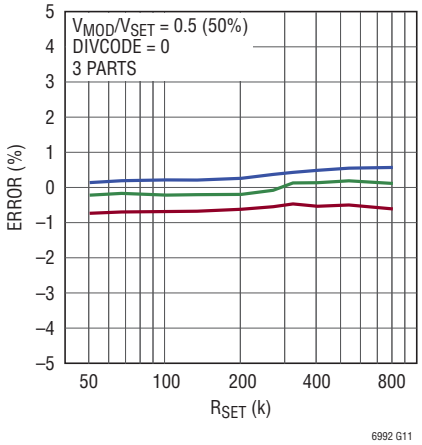
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

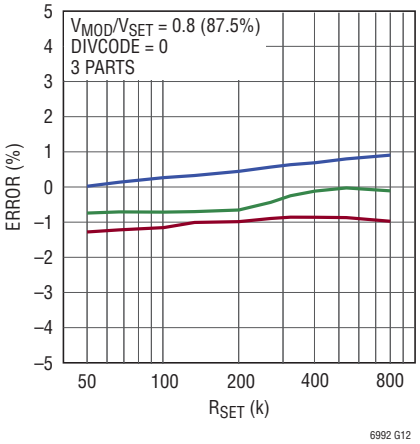
N_{DIV} = 1 Duty Cycle Error vs R_{SET}



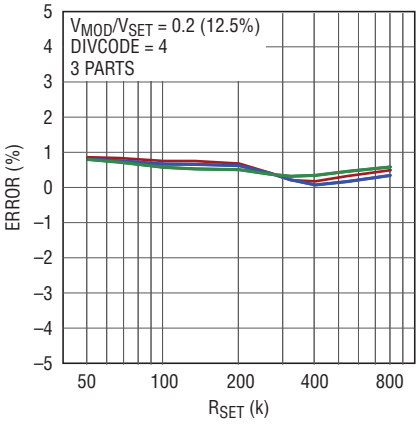
N_{DIV} = 1 Duty Cycle Error vs R_{SET}



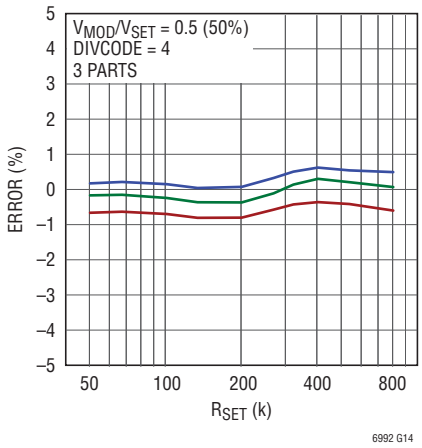
N_{DIV} = 1 Duty Cycle Error vs R_{SET}



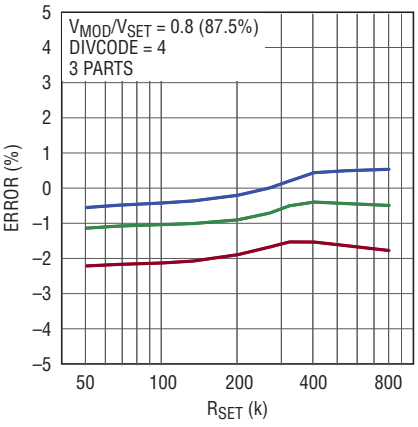
N_{DIV} > 1 Duty Cycle Error vs R_{SET}



N_{DIV} > 1 Duty Cycle Error vs R_{SET}



N_{DIV} > 1 Duty Cycle Error vs R_{SET}



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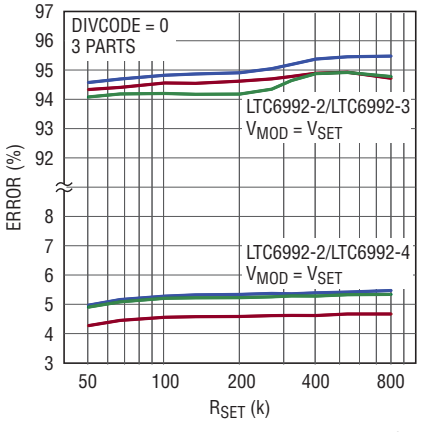
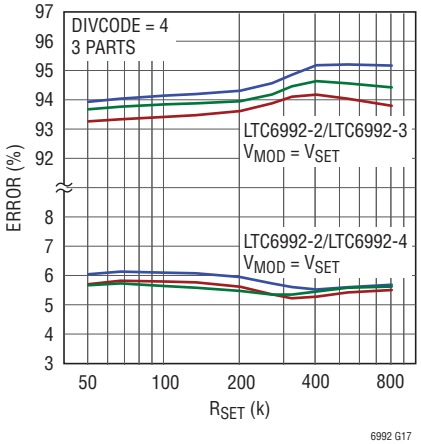


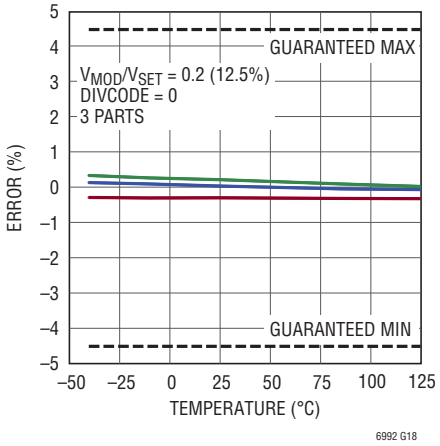
N_{DIV} > 1 Duty Cycle Error vs R_{SET}



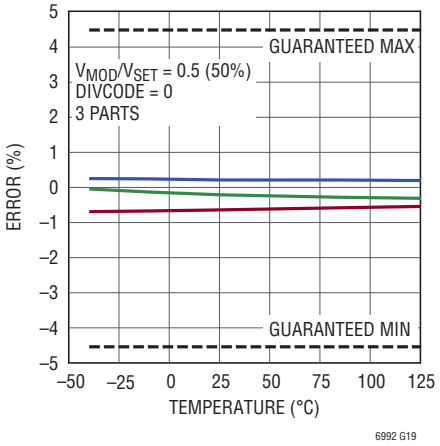
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

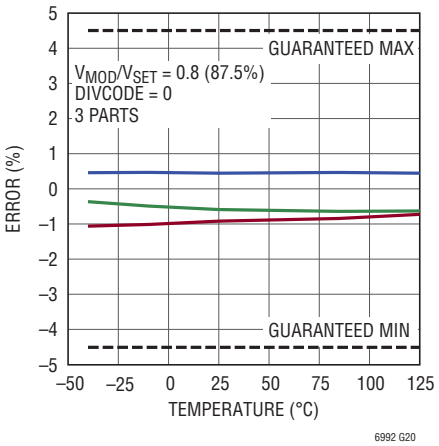
N_{DIV} = 1 Duty Cycle Error vs Temperature



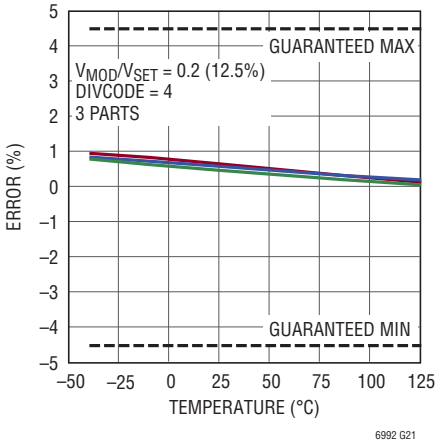
N_{DIV} = 1 Duty Cycle Error vs Temperature



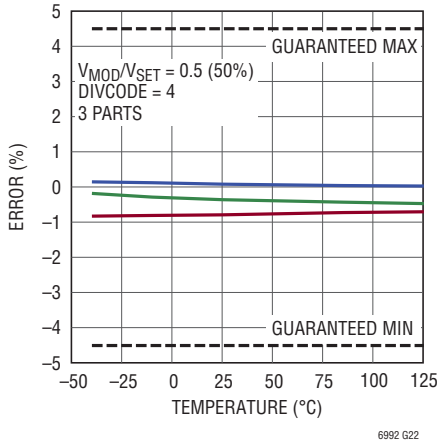
N_{DIV} = 1 Duty Cycle Error vs Temperature



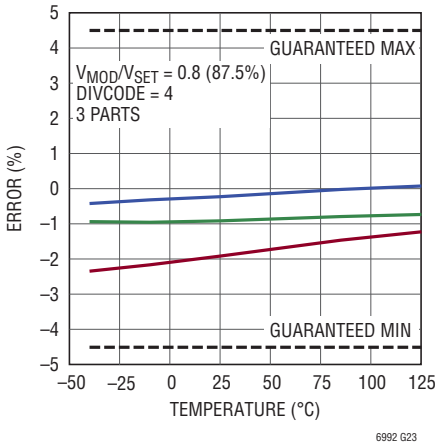
N_{DIV} > 1 Duty Cycle Error vs Temperature



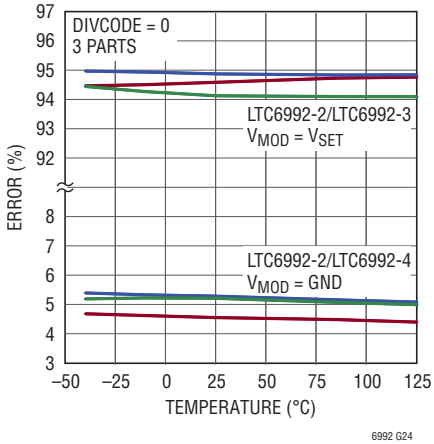
N_{DIV} > 1 Duty Cycle Error vs Temperature



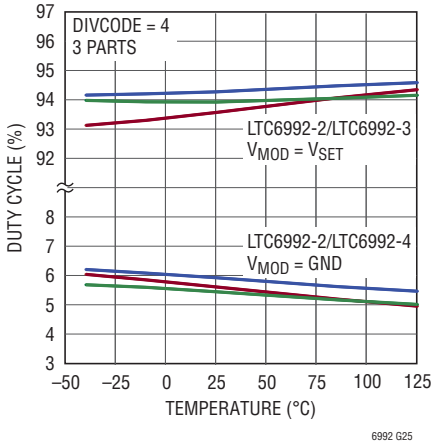
N_{DIV} > 1 Duty Cycle Error vs Temperature



N_{DIV} = 1 Duty Cycle Clamps vs Temperature



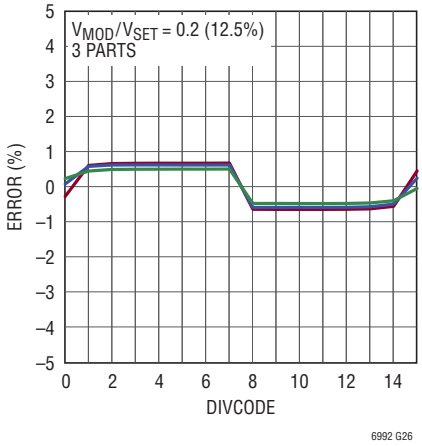
N_{DIV} > 1 Duty Cycle Clamps vs Temperature



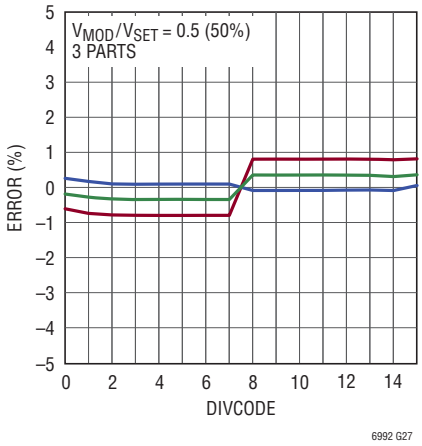
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

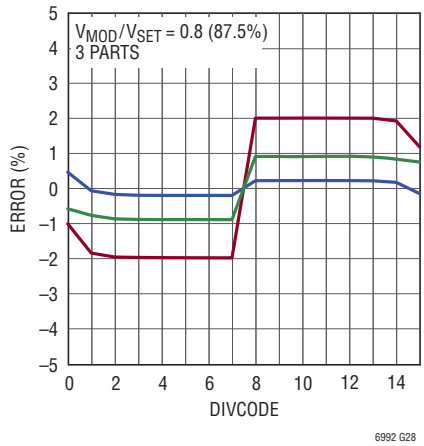
Duty Cycle Error vs DIVCODE



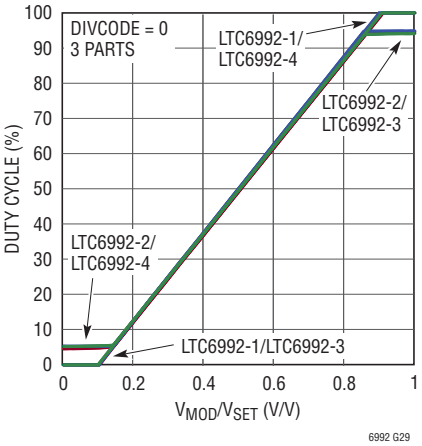
Duty Cycle Error vs DIVCODE



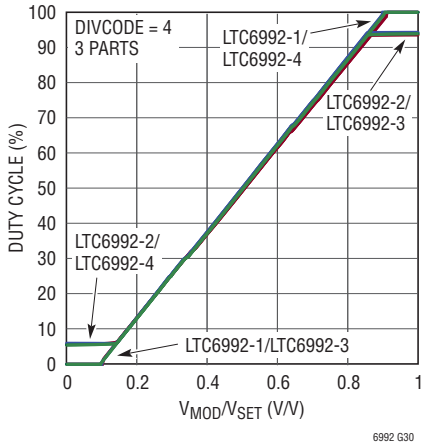
Duty Cycle Error vs DIVCODE



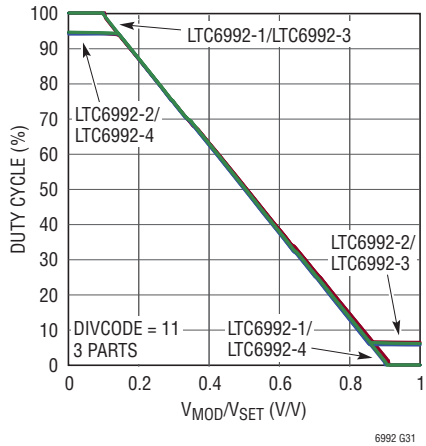
N_{DIV} = 1 Duty Cycle vs V_{MOD}/V_{SET}



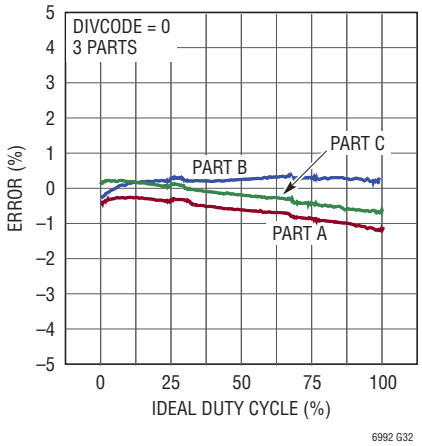
N_{DIV} > 1 Duty Cycle vs V_{MOD}/V_{SET}



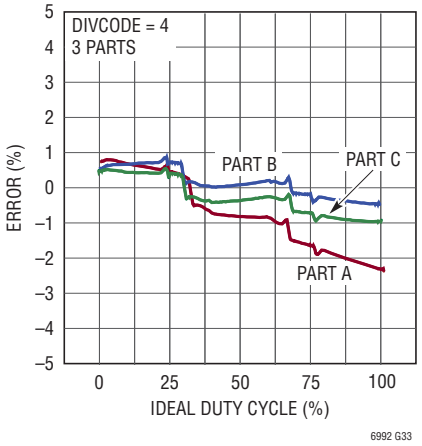
N_{DIV} > 1 Duty Cycle vs V_{MOD}/V_{SET}



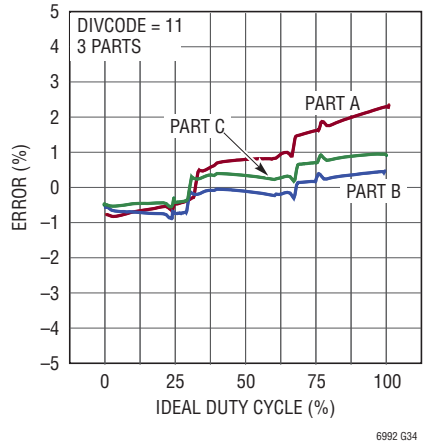
N_{DIV} = 1 Duty Cycle Error vs Ideal



N_{DIV} > 1 Duty Cycle Error vs Ideal



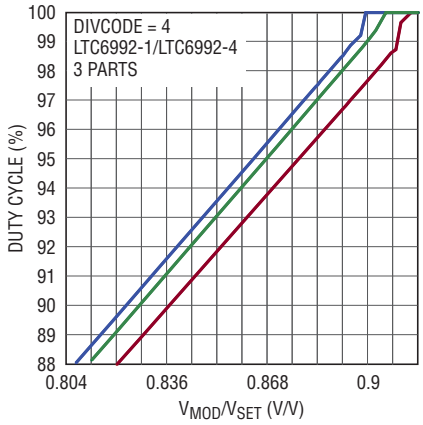
N_{DIV} > 1 Duty Cycle Error vs Ideal



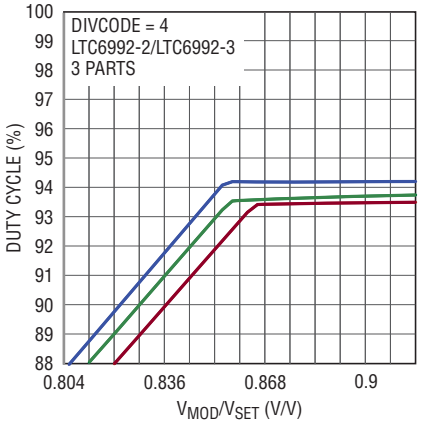
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

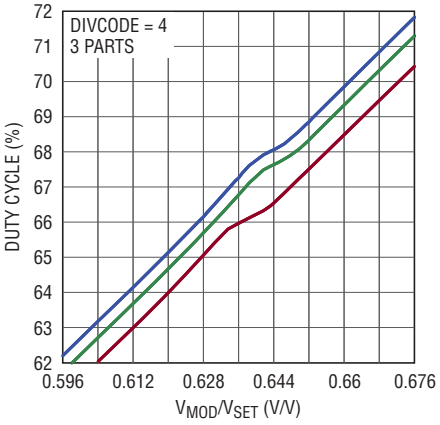
Linearity Near 100% Duty Cycle



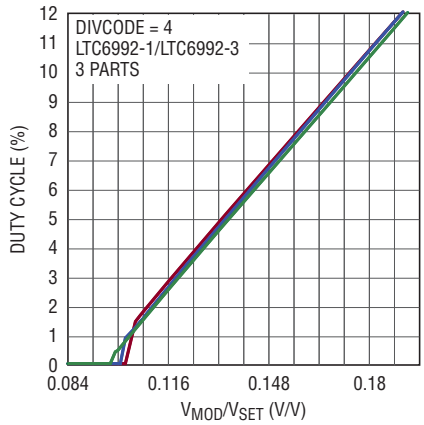
Linearity Near 95% Duty Cycle



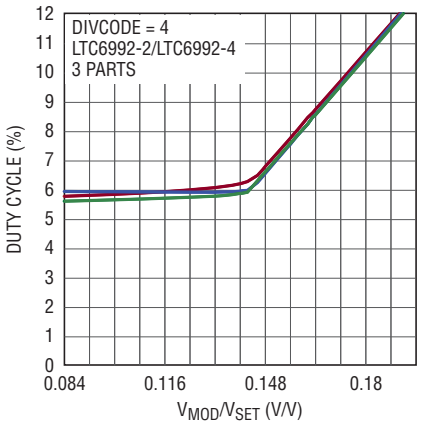
Linearity Near 67% Duty Cycle



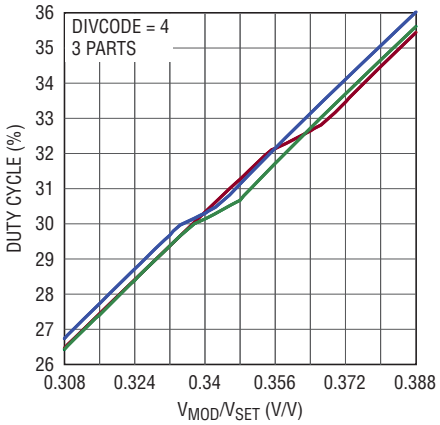
Linearity Near 0% Duty Cycle



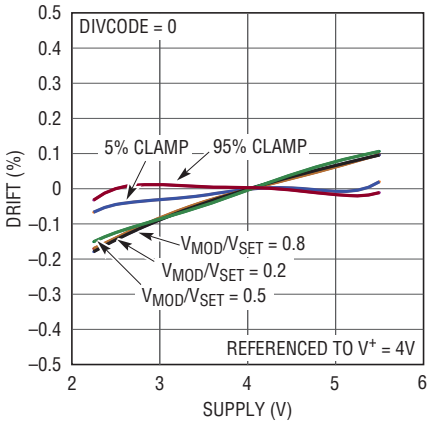
Linearity Near 5% Duty Cycle



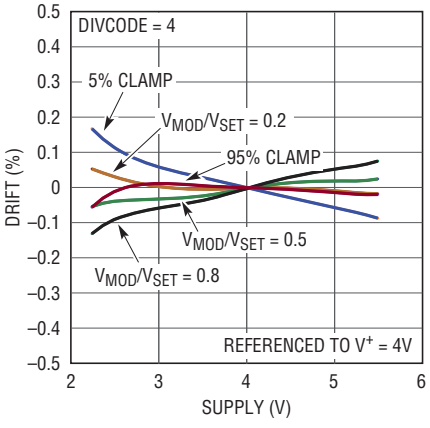
Linearity Near 31% Duty Cycle



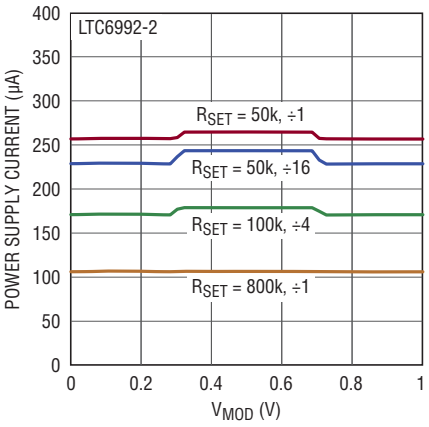
Duty Cycle Drift vs Supply



N_{DIV} > 1 Duty Cycle Drift vs Supply



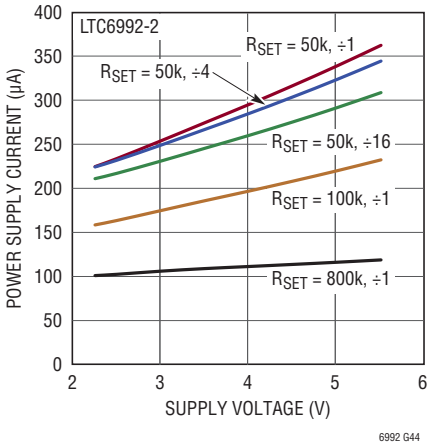
Supply Current vs V_{MOD}



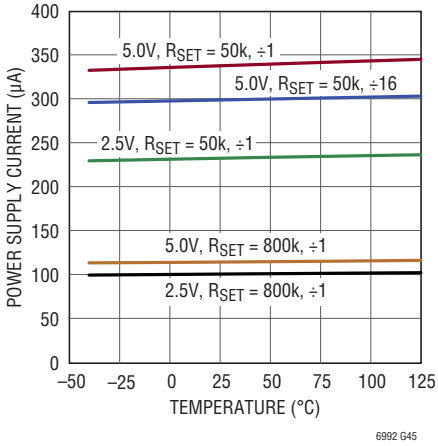
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

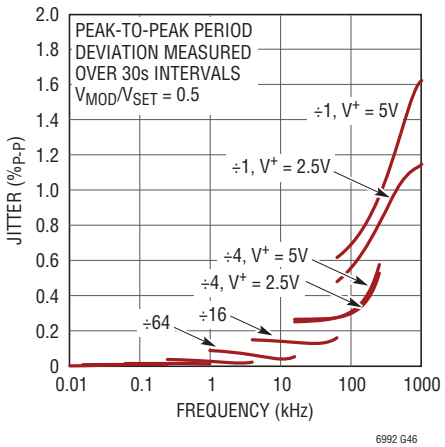
Supply Current vs Supply Voltage



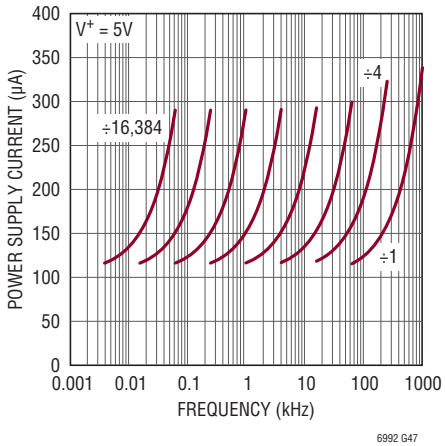
Supply Current vs Temperature



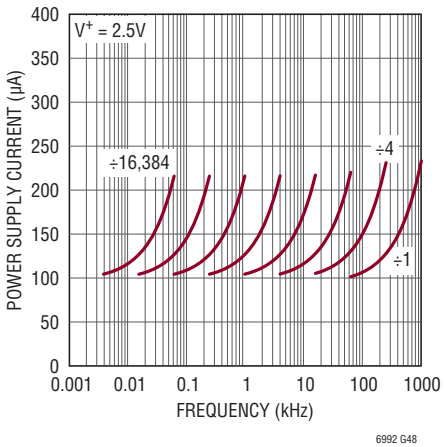
Jitter vs Frequency



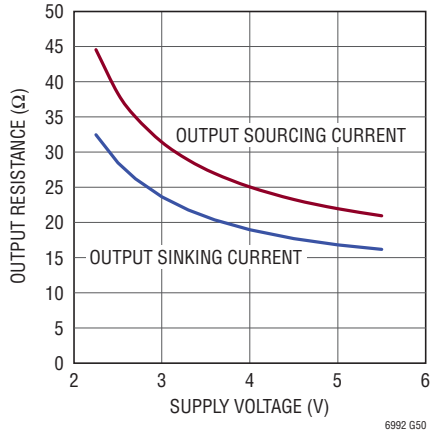
Supply Current vs Frequency, 5V



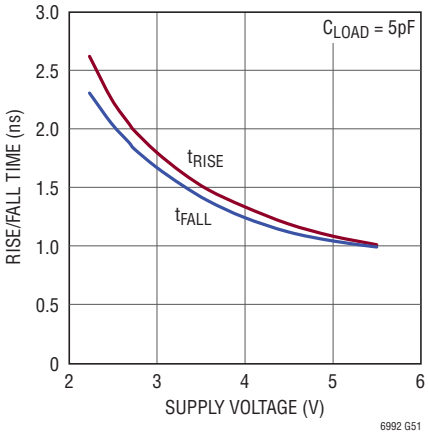
Supply Current vs Frequency, 2.5V



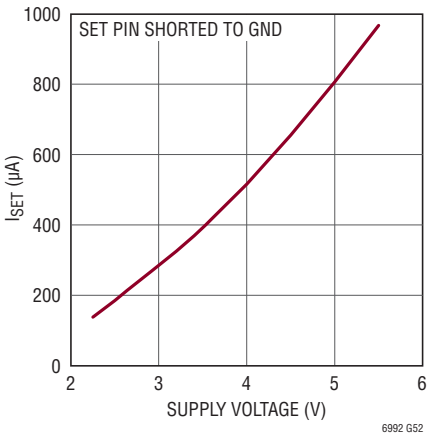
Output Resistance vs Supply Voltage



Rise and Fall Time vs Supply Voltage



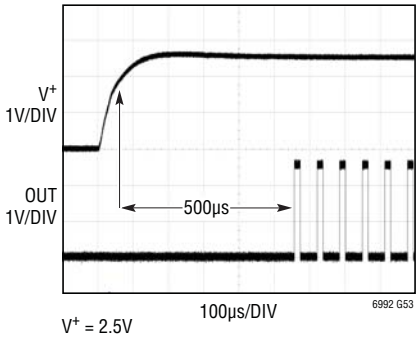
Typical I_{SET} Current Limit vs V^+



TYPICAL PERFORMANCE CHARACTERISTICS

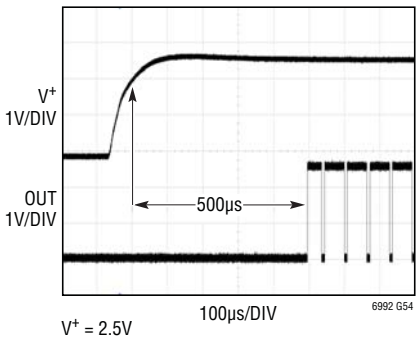
V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

Typical Start-Up, POL = 0



V^+ = 2.5V
DIVCODE = 3 (÷64)
R_{SET} = 50k
V_{MOD} = 0.3V (~25% DUTY CYCLE)

Typical Start-Up, POL = 1



V^+ = 2.5V
DIVCODE = 12 (÷64, POL = 1)
R_{SET} = 50k
V_{MOD} = 0.2V (~87.5% DUTY CYCLE)

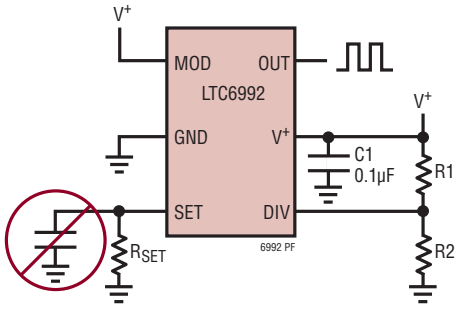
PIN FUNCTIONS (DCB/S6)

V^+ (Pin 1/Pin 5): Supply Voltage (2.25V to 5.5V). This supply must be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1µF capacitor.

DIV (Pin 2/Pin 4): Programmable Divider and Polarity Input. A V^+ referenced A/D converter monitors the DIV pin voltage (V_{DIV}) to determine a 4-bit result (DIVCODE). V_{DIV} may be generated by a resistor divider between V^+ and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that V_{DIV} settles quickly. The MSB of DIVCODE (POL) determines if the PWM signal is inverted before driving the output. Setting POL = 1 results in a negative transfer function (duty cycle decreasing as V_{MOD} increases).

SET (Pin 3/Pin 3): Frequency-Setting Input. The voltage on the SET pin (V_{SET}) is regulated to 1V above GND. The amount of current sourced from the SET pin (I_{SET}) programs the master oscillator frequency. The I_{SET} current range is 1.25µA to 20µA. The output oscillation will stop if I_{SET} drops below approximately 500nA. A resistor connected between SET and GND is the most accurate way to set the frequency. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less than 100pF maintains the stability of the feedback circuit regulating the V_{SET} voltage.



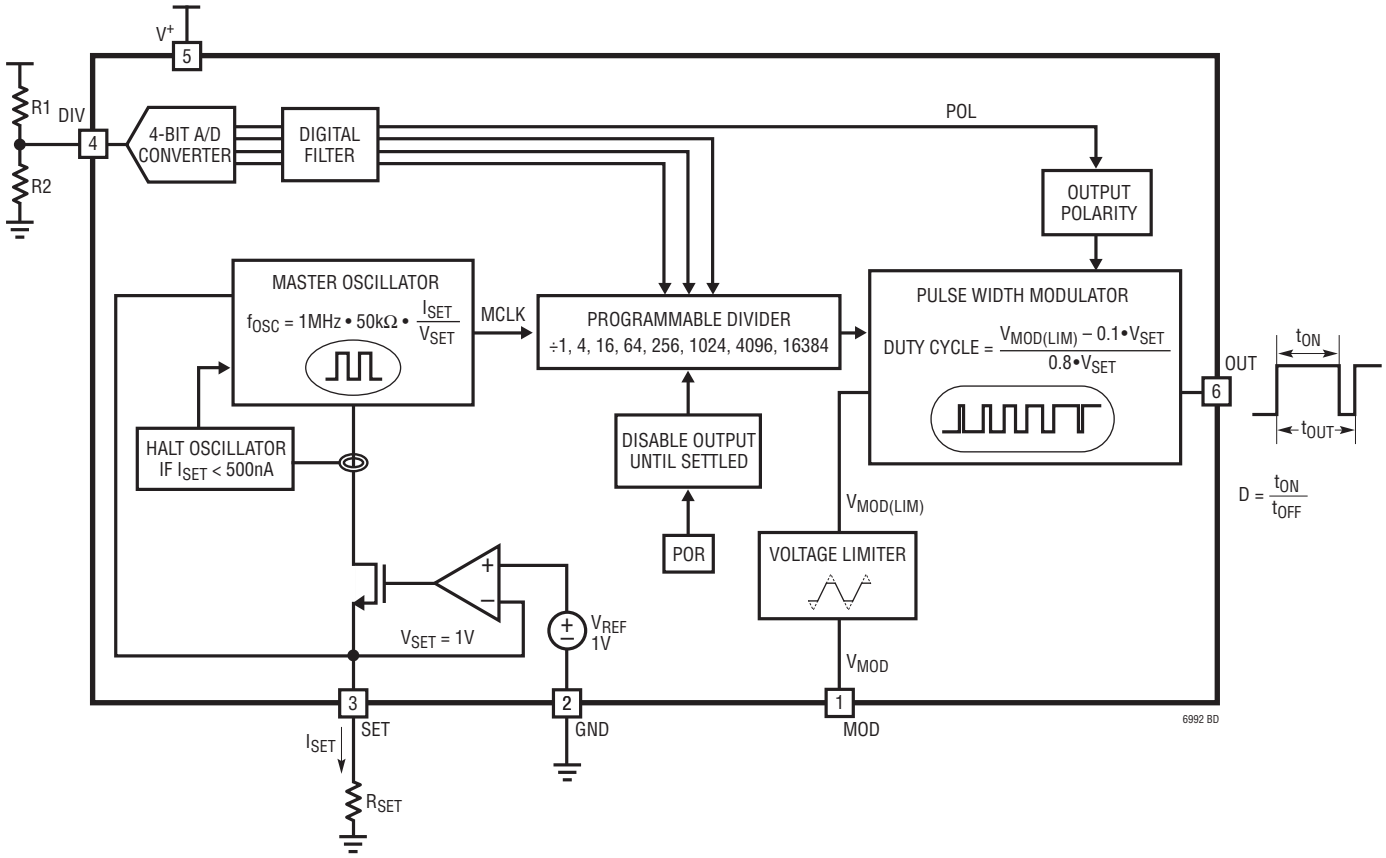
PIN FUNCTIONS (DCB/S6)

MOD (Pin 4/Pin 1): Pulse-Width Modulation Input. The voltage on the MOD pin controls the output duty cycle. The linear control range is between $0.1 \bullet V_{SET}$ and $0.9 \bullet V_{SET}$ (approximately 100mV to 900mV). Beyond those limits the output will either clamp at 5% or 95%, or stop oscillating (0% or 100% duty cycle), depending on the version.

GND (Pin 5/Pin 2): Ground. Tie to a low inductance ground plane for best performance.

OUT (Pin 6/Pin 6): Oscillator Output. The OUT pin swings from GND to V^+ with an output resistance of approximately 30Ω. The duty cycle is determined by the voltage on the MOD pin. When driving an LED or other low-impedance load a series output resistor should be used to limit source/sink current to 20mA.

BLOCK DIAGRAM (S6 Package Pin Numbers Shown)



OPERATION

The LTC6992 is built around a master oscillator with a 1MHz maximum frequency. The oscillator is controlled by the SET pin current (I_{SET}) and voltage (V_{SET}), with a 1MHz • 50k conversion factor that is accurate to ±0.8% under typical conditions.

$$f_{MASTER} = \frac{1}{t_{MASTER}} = 1MHz \bullet 50k \bullet \frac{I_{SET}}{V_{SET}}$$

A feedback loop maintains V_{SET} at 1V ±30mV, leaving I_{SET} as the primary means of controlling the output frequency. The simplest way to generate I_{SET} is to connect a resistor (R_{SET}) between SET and GND, such that $I_{SET} = V_{SET}/R_{SET}$. The master oscillator equation reduces to:

$$f_{MASTER} = \frac{1}{t_{MASTER}} = \frac{1MHz \bullet 50k}{R_{SET}}$$

From this equation it is clear that V_{SET} drift will not affect the output frequency when using a single program resistor (R_{SET}). Error sources are limited to R_{SET} tolerance and the inherent frequency accuracy Δf_{OUT} of the LTC6992.

R_{SET} may range from 50k to 800k (equivalent to I_{SET} between 1.25µA and 20µA).

The LTC6992 includes a programmable frequency divider which can further divide the frequency by 1, 4, 16, 64, 256, 1024, 4096 or 16384 before driving the OUT pin. The divider ratio N_{DIV} is set by a resistor divider attached to the DIV pin.

$$f_{OUT} = \frac{1}{t_{OUT}} = \frac{1MHz \bullet 50k}{N_{DIV}} \bullet \frac{I_{SET}}{V_{SET}}$$

With R_{SET} in place of V_{SET}/I_{SET} the equation reduces to:

$$f_{OUT} = \frac{1}{t_{OUT}} = \frac{1MHz \bullet 50k}{N_{DIV} \bullet R_{SET}}$$

DIVCODE

The DIV pin connects to an internal, V^+ referenced 4-bit A/D converter that monitors the DIV pin voltage (V_{DIV}) to determine the DIVCODE value. DIVCODE programs two settings on the LTC6992:

1. DIVCODE determines the output frequency divider setting, N_{DIV}.
2. DIVCODE determines the output polarity, via the POL bit.

V_{DIV} may be generated by a resistor divider between V^+ and GND as shown in Figure 1.

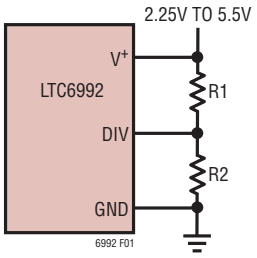


Figure 1. Simple Technique for Setting DIVCODE

OPERATION

Table 1. DIVCODE Programming

DIVCODE	POL	N_{DIV}	RECOMMENDED f_{OUT}	R1 (kΩ)	R2 (kΩ)	V_{DIV}/V^+
0	0	1	62.5kHz to 1MHz	Open	Short	≤0.03125 ±0.015
1	0	4	15.63kHz to 250kHz	976	102	0.09375 ±0.015
2	0	16	3.906kHz to 62.5kHz	976	182	0.15625 ±0.015
3	0	64	976.6Hz to 15.63kHz	1000	280	0.21875 ±0.015
4	0	256	244.1Hz to 3.906kHz	1000	392	0.28125 ±0.015
5	0	1024	61.04Hz to 976.6Hz	1000	523	0.34375 ±0.015
6	0	4096	15.26Hz to 244.1Hz	1000	681	0.40625 ±0.015
7	0	16384	3.815Hz to 61.04Hz	1000	887	0.46875 ±0.015
8	1	16384	3.815Hz to 61.04Hz	887	1000	0.53125 ±0.015
9	1	4096	15.26Hz to 244.1Hz	681	1000	0.59375 ±0.015
10	1	1024	61.04Hz to 976.6Hz	523	1000	0.65625 ±0.015
11	1	256	244.1Hz to 3.906kHz	392	1000	0.71875 ±0.015
12	1	64	976.6Hz to 15.63kHz	280	1000	0.78125 ±0.015
13	1	16	3.906kHz to 62.5kHz	182	976	0.84375 ±0.015
14	1	4	15.63kHz to 250kHz	102	976	0.90625 ±0.015
15	1	1	62.5kHz to 1MHz	Short	Open	≥0.96875 ±0.015

Table 1 offers recommended 1% resistor values that accurately produce the correct voltage division as well as the corresponding N_{DIV} and POL values for the recommended resistor pairs. Other values may be used as long as:

1. The V_{DIV}/V^+ ratio is accurate to ±1.5% (including resistor tolerances and temperature effects)
2. The driving impedance (R1||R2) does not exceed 500kΩ.

If the voltage is generated by other means (i.e. the output of a DAC) it must track the V^+ supply voltage. The last column in Table 1 shows the ideal ratio of V_{DIV} to the supply voltage, which can also be calculated as:

$$\frac{V_{DIV}}{V^+} = \frac{DIVCODE + 0.5}{16} \pm 1.5\%$$

For example, if the supply is 3.3V and the desired DIVCODE is 4, V_{DIV} = 0.281 • 3.3V = 928mV ± 50mV.

Figure 2 illustrates the information in Table 1, showing that N_{DIV} is symmetric around the DIVCODE midpoint.

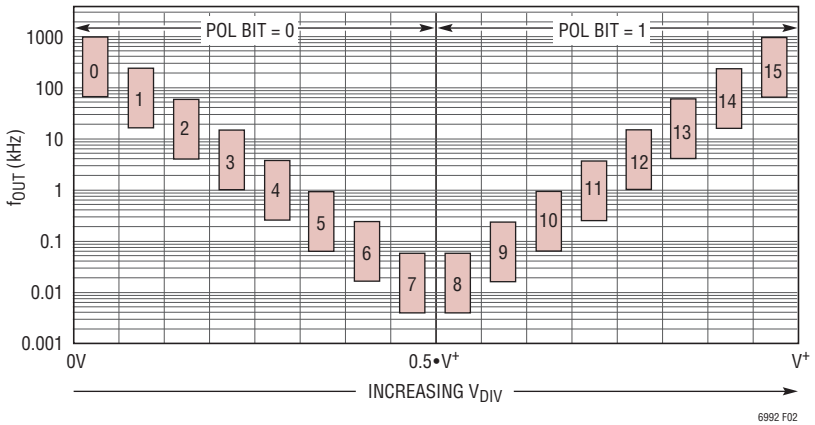


Figure 2. Frequency Range and POL Bit vs DIVCODE

OPERATION

Pulse Width (Duty Cycle) Modulation

The MOD pin is a high impedance analog input providing direct control of the output duty cycle. The duty cycle is proportional to the voltage applied to the MOD pin, V_{MOD}.

$$\text{Duty Cycle} = D = \frac{V_{MOD}}{0.8 \bullet V_{SET}} - \frac{1}{8}$$

The PWM duty cycle accuracy ΔD specifies that the above equation is valid to within ±4.5% for V_{MOD} between 0.2 • V_{SET} and 0.8 • V_{SET} (12.5% to 87.5% duty cycle).

Since V_{SET} = 1V ±30mV, the duty cycle equation may be approximated by the following equation.

$$\text{Duty Cycle} = D \cong \frac{V_{MOD} - 100mV}{800mV}$$

The V_{MOD} control range is approximately 0.1V to 0.9V. Driving V_{MOD} beyond that range (towards GND or V^+) will have no further affect on the duty cycle.

Duty Cycle Limits

The only difference between the four versions of the LTC6992 is the limits, or clamps, placed on the output duty cycle. The LTC6992-1 generates output duty cycles ranging from 0% to 100%, meaning the output can stop oscillating and rest at GND or V^+.

The LTC6992-2 will never stop oscillating, regardless of the V_{MOD} level. Internal clamping circuits limit its duty cycle to a 5% to 95% range (1% to 99% guaranteed). Therefore, its V_{MOD} control range is 0.14 • V_{SET} to 0.86 • V_{SET} (approximately 0.14V to 0.86V).

The LTC6992-3 and LTC6992-4 complete the family by providing one-sided clamping. The LTC6992-3 allows 0% to 95% duty cycle, and the LTC6992-4 allows 5% to 100% duty cycle.

Output Polarity (POL Bit)

The duty cycle equation describes a proportional transfer function, where duty cycle increases as V_{MOD} increases. The LTC6992 includes a POL bit (determined by the DIVCODE as described earlier) that inverts the output signal. This makes the duty cycle gain negative, reducing duty cycle as V_{MOD} increases.

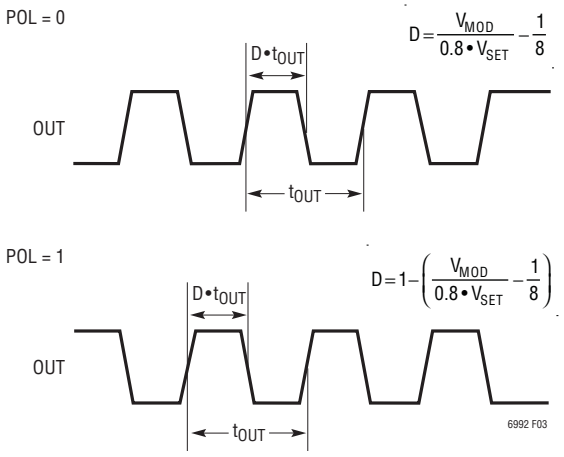


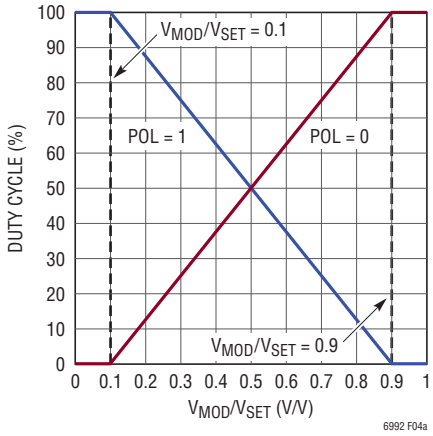
Figure 3. POL Bit Functionality

OPERATION

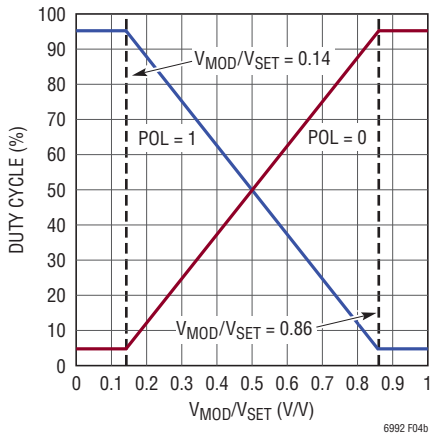
POL = 1 forces a simple logic inversion, so it changes the duty cycle range of the LTC6992-3 (making it 100% to 5%) and LTC6992-4 (making it 95% to 0%). These transfer functions are detailed in Figure 4.

Table 2. Duty Cycle Ranges

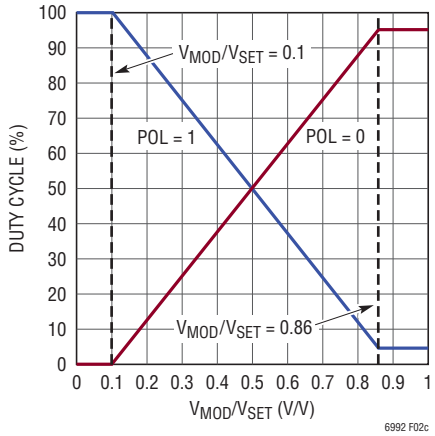
PART NUMBER	DUTY CYCLE RANGE vs V_{MOD} = 0V → 1V	
	POL = 0	POL = 1
LTC6992-1	0% to 100%	100% to 0%
LTC6992-2	5% to 95%	95% to 5%
LTC6992-3	0% to 95%	100% to 5%
LTC6992-4	5% to 100%	95% to 0%



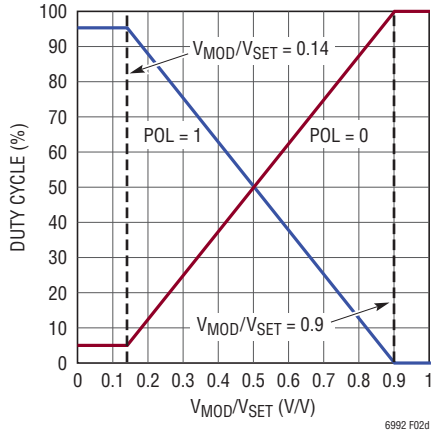
LTC6992-1



LTC6992-2



LTC6992-3



LTC6992-4

Figure 4. PWM Transfer Functions for All LTC6992 Family Parts

OPERATION

Changing DIVCODE After Start-Up

Following start-up, the A/D converter will continue monitoring V_{DIV} for changes. Changes to DIVCODE will be recognized slowly, as the LTC6992 places a priority on eliminating any "wandering" in the DIVCODE. The typical delay depends on the difference between the old and new DIVCODE settings and is proportional to the master oscillator period.

$$t_{DIVCODE} = 16 \bullet (\Delta DIVCODE + 6) \bullet t_{MASTER}$$

A change in DIVCODE will not be recognized until it is stable, and will not pass through intermediate codes. A digital filter is used to guarantee the DIVCODE has settled to a new value before making changes to the output. Then the output will make a clean (glitchless) transition to the new divider setting.

Start-Up Time

When power is first applied to the LTC6992 the power-on reset (POR) circuit will initiate the start-up time, t_{START}. The OUT pin is held low during this time. The typical value for t_{START} ranges from 0.5ms to 8ms depending on the master oscillator frequency (independent of N_{DIV}):

$$t_{START(TYP)} = 500 \bullet t_{MASTER}$$

The output will begin oscillating after t_{START}. If POL = 0 the first pulse has the correct width. If POL = 1 (DIVCODE ≥ 8), the first pulse width can be shorter or longer than expected, depending on the duty cycle setting, and will never be less than 25% of t_{OUT}.

During start-up, the DIV pin A/D converter must determine the correct DIVCODE before the output is enabled. The start-up time may increase if the supply or DIV pin voltages are not stable. For this reason, it is recommended to minimize the capacitance on the DIV pin so it will properly track V^+. Less than 100pF will not affect performance.

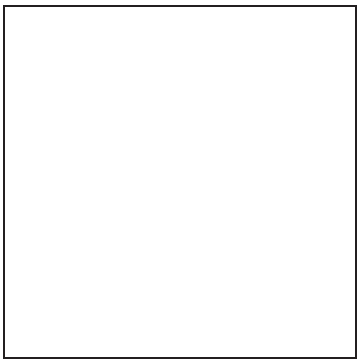


Figure 5. DIVCODE Change from 5 to 2

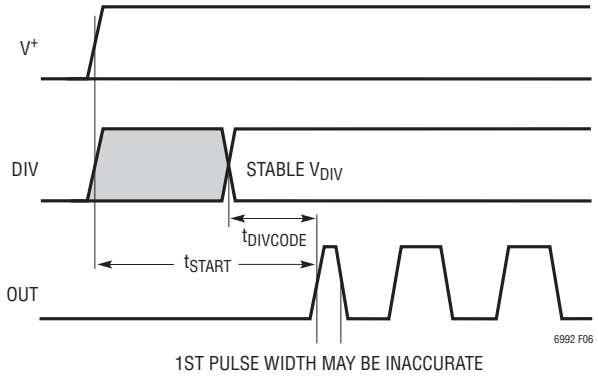


Figure 6. Start-Up Timing Diagram

APPLICATIONS INFORMATION

Basic Operation

The simplest and most accurate method to program the LTC6992 is to use a single resistor, R_{SET}, between the SET and GND pins. The design procedure is a four step process. After choosing the POL bit setting and proper LTC6992 version, select the N_{DIV} value and then calculate the value for the R_{SET} resistor.

Step 1: Selecting the POL Bit Setting

Most applications will use POL = 0, resulting in a positive transfer function. However, some applications may require a negative transfer function, where increasing V_{MOD} reduces the output duty cycle. For example, if the LTC6992 is used in a feedback loop, POL = 1 may be required to achieve negative feedback.

Step 2: Selecting the LTC6992 Version

The difference between the LTC6992 versions is observed at the endpoints of the duty cycle control range. Applications that require the output never stop oscillating should use the LTC6992-2. If it is better to allow the output to rest at GND or V^+ (0% or 100% duty cycle, respectively), select the LTC6992-1.

The LTC6992-3 and LTC6992-4 clamp the duty cycle at only one end of the control range, allowing the output to stop oscillating at the other extreme. If POL = 1 the clamp will swap from low duty cycle to high, or vice-versa. Refer to Table 2 and Figure 4 for assistance in selecting the proper version.

Step 3: Selecting the N_{DIV} Frequency Divider Value

As explained earlier, the voltage on the DIV pin sets the DIVCODE which determines both the POL bit and the N_{DIV} value. For a given output frequency, N_{DIV} should be selected to be within the following range.

$$\frac{62.5kHz}{f_{OUT}} \leq N_{DIV} \leq \frac{1MHz}{f_{OUT}} \quad (1a)$$

To minimize supply current, choose the lowest N_{DIV} value (generally recommended). For faster start-up or decreased jitter, choose a higher N_{DIV} setting. Alternatively, use Table 1 as a guide to select the best N_{DIV} value for the given application.

With POL already chosen, this completes the selection of DIVCODE. Use Table 1 to select the proper resistor divider or V_{DIV}/V^+ ratio to apply to the DIV pin.

Step 4: Calculate and Select R_{SET}

The final step is to calculate the correct value for R_{SET} using the following equation.

$$R_{SET} = \frac{1MHz \bullet 50k}{N_{DIV} \bullet f_{OUT}} \quad (1b)$$

Select the standard resistor value closest to the calculated value.

Example: Design a PWM circuit that satisfies the following requirements:

- f_{OUT} = 20kHz
- Positive V_{MOD} to duty cycle response
- Output can reach 100% duty cycle, but not 0%
- Minimum power consumption

Step 1: Selecting the POL Bit Setting

For positive transfer function (duty cycle increases with V_{MOD}), choose POL = 0.

Step 2: Selecting the LTC6992 Version

To limit the minimum duty cycle, but allow the maximum duty cycle to reach 100%, choose LTC6992-4. (Note that if POL = 1 the LTC6992-3 would be the correct choice.)

Step 3: Selecting the N_{DIV} Frequency Divider Value

Choose an N_{DIV} value that meets the requirements of Equation (1a).

$3.125 \leq N_{DIV} \leq 50$

Potential settings for N_{DIV} include 4 and 16. N_{DIV} = 4 is the best choice, as it minimizes supply current by using a large R_{SET} resistor. POL = 0 and N_{DIV} = 4 requires DIVCODE = 1. Using Table 1, choose the R1 and R2 values to program DIVCODE = 1.

APPLICATIONS INFORMATION

Step 4: Select R_{SET}

Calculate the correct value for R_{SET} using Equation (1b).

$$R_{SET} = \frac{1MHz \bullet 50k}{4 \bullet 20kHz} = 625k$$

Since 625k is not available as a standard 1% resistor, substitute 619k if a 0.97% frequency shift is acceptable. Otherwise, select a parallel or series pair of resistors such as 309k and 316k to attain a more precise resistance.

The completed design is shown in Figure 7.

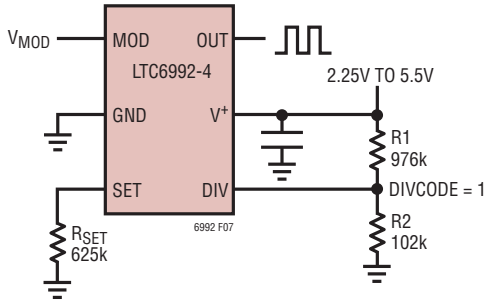


Figure 7. 20kHz PWM Oscillator

Duty Cycle Sensitivity to ΔV_{SET}

The output duty cycle is proportional to the ratio of V_{MOD}/V_{SET}. Since V_{SET} can vary up to ±30mV from 1V it can effectively gain or attenuate V_{MOD}, as shown below when ΔV_{SET} is added to the equation.

$$D = \frac{V_{MOD}}{0.8 \bullet (V_{SET} + \Delta V_{SET})} - \frac{1}{8}$$

The simplifying assumption of $\Delta V_{SET} = 0V$ creates the potential for additional duty cycle error, which increases with V_{MOD}, reaching a maximum of 3.4% if $\Delta V_{SET} = -30mV$.

$$\Delta D \cong \frac{V_{MOD}}{800mV} \bullet \frac{\Delta V_{SET}}{V_{SET}} \cong -\left(D_{ideal} + \frac{1}{8}\right) \bullet \frac{\Delta V_{SET}}{V_{SET}}$$

Figure 8 demonstrates the worst-case impact of this variation (if V_{SET} is at its 0.97V or 1.03V limits).

This error is in addition to the inherent PWM duty cycle accuracy spec ΔD (±4.5%), so care should be taken if accuracy at high duty cycles (V_{MOD} near 0.9V) is critical.

Some applications can eliminate ΔV_{SET} sensitivity by making V_{MOD} proportional to V_{SET}. For example, Figure 9 shows a simple circuit for generating an arbitrary duty cycle. The equation for duty cycle does not depend on V_{SET} at all.

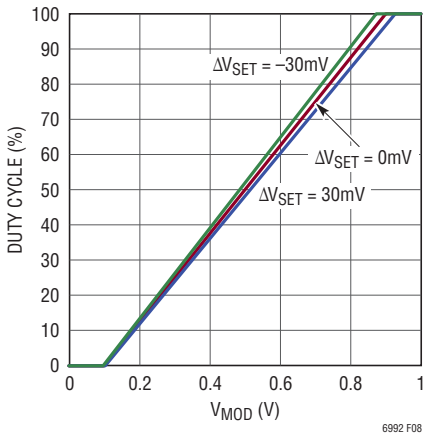


Figure 8. Duty Cycle Variation Due to ΔV_{SET}

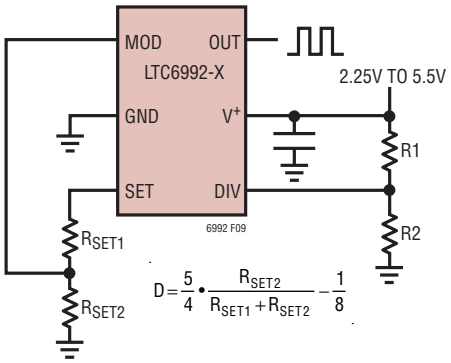


Figure 9. Fixed-Frequency, Arbitrary Duty Cycle Oscillator

I_{SET} Extremes (Master Oscillator Frequency Extremes)

Pushing I_{SET} outside of the recommended 1.25µA to 20µA range forces the master oscillator to operate outside of the 62.5kHz to 1MHz range in which it is most accurate.

The oscillator will still function with reduced accuracy for $I_{SET} < 1.25µA$. At approximately 500nA, the oscillator output will be frozen in its current state. The output could halt in a high or low state. This avoids introducing short pulses while frequency modulating a very low frequency output.

APPLICATIONS INFORMATION

At the other extreme, it is not recommended to operate the master oscillator beyond 2MHz because the accuracy of the DIV pin ADC will suffer.

Pulse Width Modulation Bandwidth and Settling Time

The LTC6992 will respond to changes in V_{MOD} up to a –3dB bandwidth of TBD (see Figure 10). This makes it easy to stabilize a feedback loop around the LTC6992, since it does not introduce a low frequency pole.

Duty cycle settling time depends on the master oscillator frequency. Following a ±100mV step change in V_{MOD}, the duty cycle takes approximately TBD master clock cycles (TBD • t_{MASTER}) to settle to within 1% of the final value. An example is shown in Figure 11.

Frequency Modulation and Settling Time

In addition to pulse-width modulation, the LTC6992 can be frequency modulated by varying I_{SET}. The LTC6992 will respond to changes in I_{SET} up to a –3dB bandwidth of TBD • f_{OUT} (see Figure 12).

Following a 2x or 0.5x step change in I_{SET}, the output frequency takes approximately TBD master clock cycles (TBD • t_{MASTER}) to settle to within 1% of the final value. An example is shown in Figure 13.

Figure 10. PWM Frequency Response

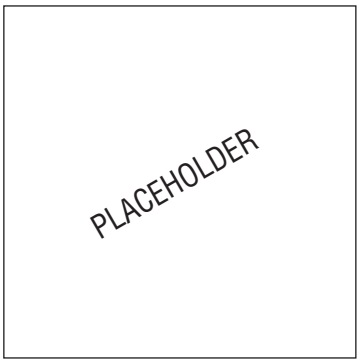


Figure 12. Frequency Modulation Bandwidth

Figure 11. PWM Settling Time

Figure 13. Frequency Change Settling Time

APPLICATIONS INFORMATION

Power Supply Current

The power supply current varies with frequency, supply voltage and output loading. It can be estimated under any condition using the following equation:

If N_{DIV} = 1 (DIVCODE = 0 or 15):

$$I_{S(TYP)} \approx V^+ \bullet f_{OUT} \bullet (39pF + C_{LOAD})$$

$$\cdots + \frac{V^+}{320k\Omega} + \frac{V^+}{2 \bullet R_{LOAD}} + 2.2 \bullet I_{SET} + 85\mu A$$

If N_{DIV} > 1 (DIVCODE = 1 or 14):

$$I_{S(TYP)} \approx V^+ \bullet \frac{f_{OUT}}{N_{DIV}} \bullet 27pF + V^+ \bullet f_{OUT} \bullet (27pF + C_{LOAD})$$

$$\cdots + \frac{V^+}{320k\Omega} + \frac{V^+}{2 \bullet R_{LOAD}} + 2.6 \bullet I_{SET} + 90\mu A$$

SUPPLY BYPASSING AND PCB LAYOUT GUIDELINES

The LTC6992 is a 2.4% accurate silicon oscillator when used in the appropriate manner. The part is simple to use and by following a few rules, the expected performance is easily achieved. The most important use issues involve adequate supply bypassing and proper PCB layout.

Figure 14 shows example PCB layouts for both the TSOT-23 and DFN packages using 0603 sized passive components. The layouts assume a two layer board with a ground plane layer beneath and around the LTC6992. These layouts are a guide and need not be followed exactly.

1. Connect the bypass capacitor, C1, directly to the V^+ and GND pins using a low inductance path. The connection from C1 to the V^+ pin is easily done directly on the top layer. For the DFN package, C1's connection to GND is also simply done on the top layer. For the TSOT-23, OUT can be routed through the C1 pads to allow a good C1 GND connection. If the PCB design rules do not allow that, C1's GND connection can be accomplished through multiple vias to the ground plane. Multiple vias for both the GND pin connection to the ground plane and the C1 connection to the ground plane are recommended to minimize the inductance. Capacitor C1 should be a 0.1µF ceramic capacitor.
2. Place all passive components on the top side of the board. This minimizes trace inductance.
3. Place R_{SET} as close as possible to the SET pin and make a direct, short connection. The SET pin is a current summing node and currents injected into this pin directly modulate the operating frequency. Having a short connection minimizes the exposure to signal pickup.
4. Connect R_{SET} directly to the GND pin. Using a long path or vias to the ground plane will not have a significant affect on accuracy, but the direct, short connection is recommended and easy to apply.
5. Use a ground trace to shield the SET pin. This provides another layer of protection from radiated signals.
6. Place R1 and R2 close to the DIV pin. A direct, short connection to the DIV pin minimizes the external signal coupling.

APPLICATIONS INFORMATION

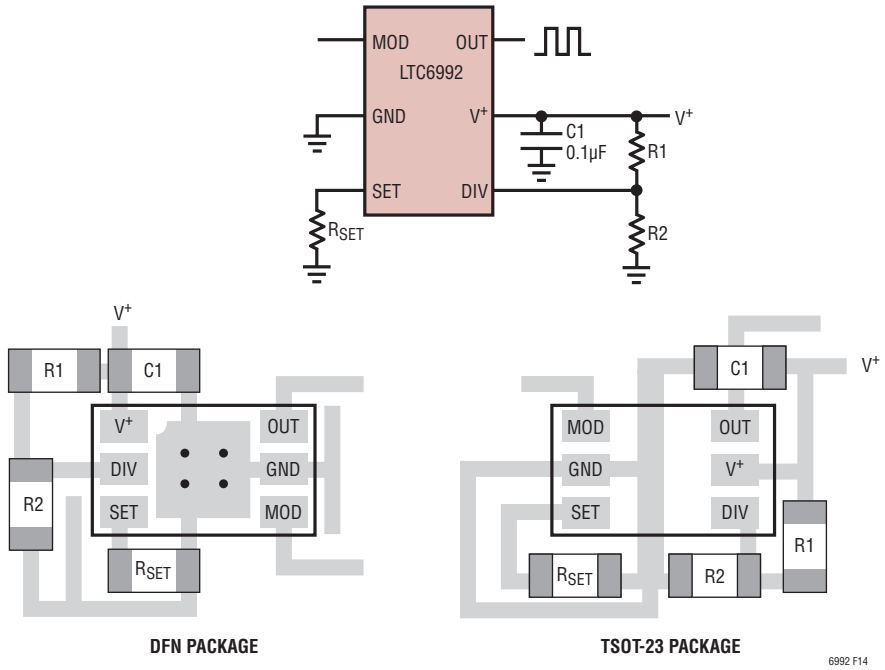
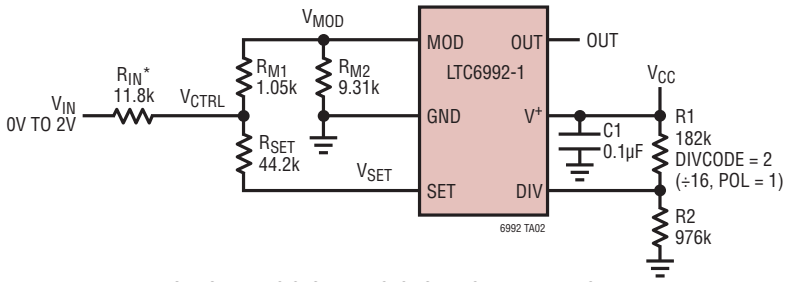


Figure 14. Supply Bypassing and PCB Layout

TYPICAL APPLICATIONS

Constant On-Time Modulator



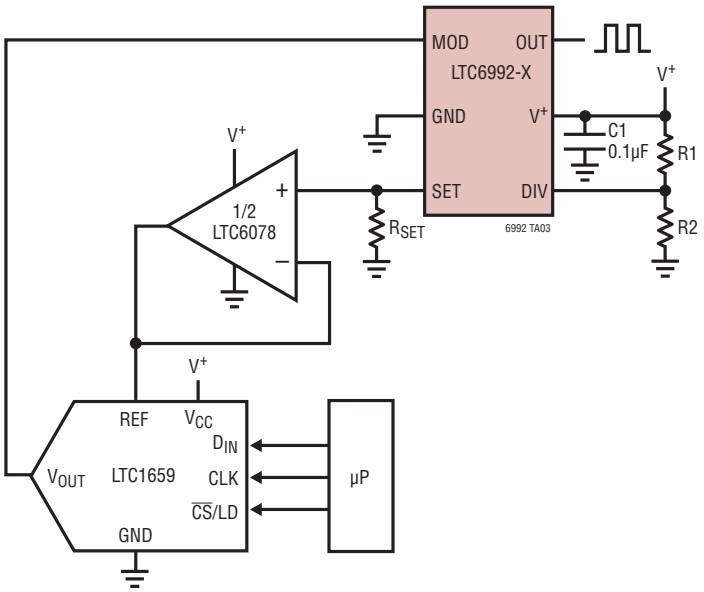
*OPTIONAL RESISTOR ADJUSTS FOR DESIRED V_{IN} RANGE.

$$\text{IF } \frac{R_{M2}}{R_{M1}+R_{M2}} = 0.9 \text{ THEN } t_{ON} = N_{DIV} \bullet 1.125\mu s \bullet \frac{R_{SET}}{50k}$$

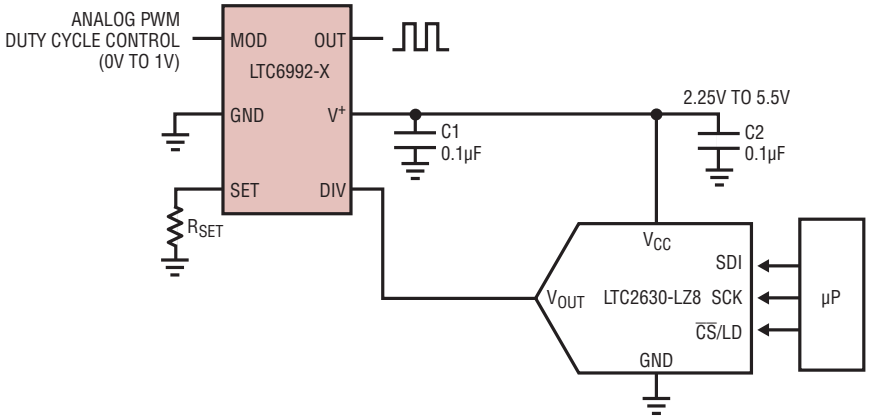
AS V_{IN} INCREASES, t_{OUT} INCREASES AND DUTY CYCLE DECREASES (BECAUSE POL = 1) TO MAINTAIN A CONSTANT t_{ON}. FOR CONSTANT OFF-TIME, JUST CHANGE DIVCODE SO POL = 0.

TYPICAL APPLICATIONS

Digitally Controlled Duty Cycle with Internal V_{REF} Reference Variation Eliminated



Programming N_{DIV} Using an 8-Bit DAC

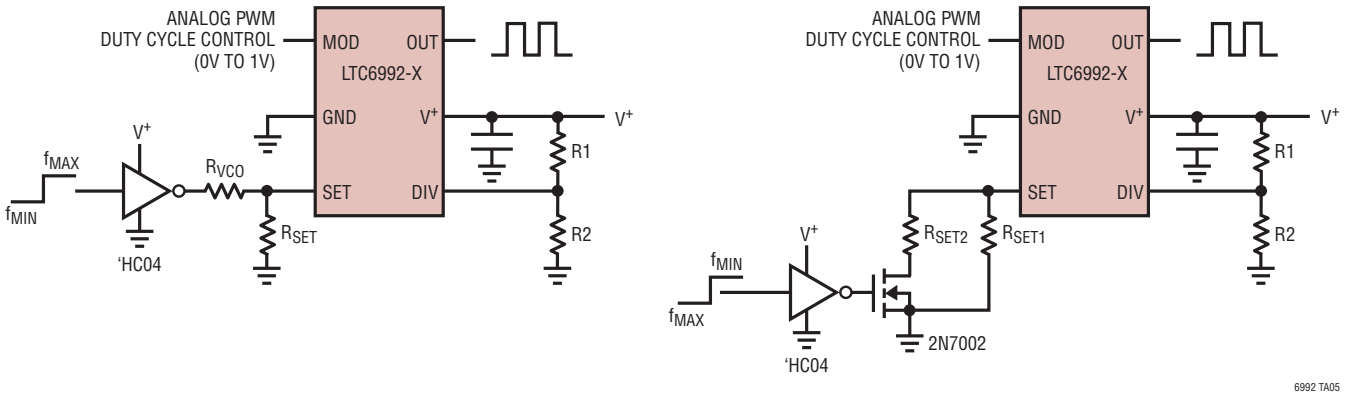


DIVCODE	DAC CODE
0	0
1	24
2	40
3	56
4	72
5	88
6	104
7	120
8	136
9	152
10	168
11	184
12	200
13	216
14	232
15	≥255

6992 TA04

TYPICAL APPLICATIONS

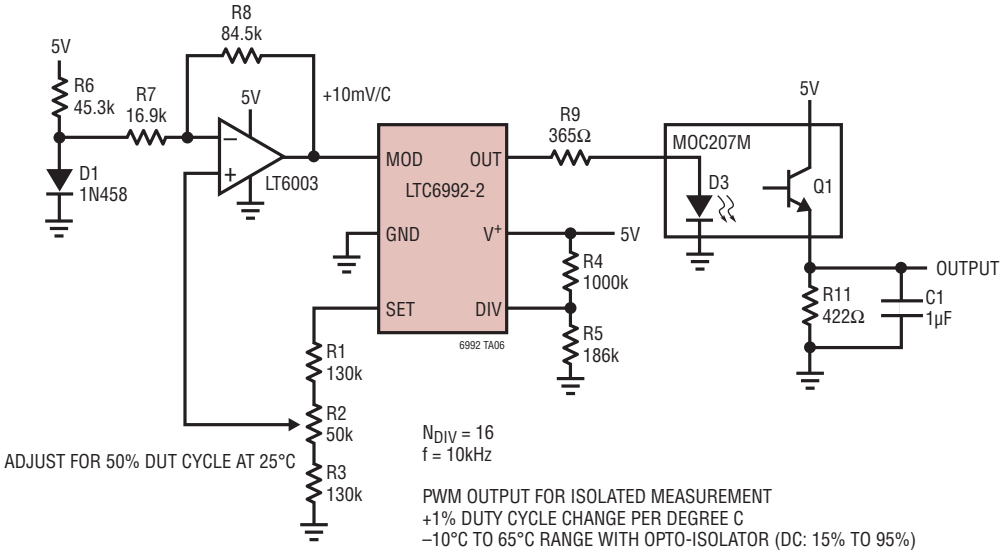
Changing Between Two Frequencies



NOTES
WHILE THIS CIRCUIT IS SIMPLER THAN THE CIRCUIT TO THE RIGHT, ITS FREQUENCY ACCURACY IS WORSE DUE TO THE EFFECT OF V^+ SUPPLY VARIATION FROM SYSTEM TO SYSTEM AND OVER TEMPERATURE.

NOTES
1. WHEN THE NMOSFET IS OFF, THE FREQUENCY IS SET BY $R_{SET} = R_{SET1}$.
2. WHEN THE NMOSFET IS ON, THE FREQUENCY IS SET BY $R_{SET} = R_{SET1} \parallel R_{SET2}$.
3. V^+ SUPPLY VARIATION IS NOT A FACTOR AS THE SWITCHING RESISTOR IS EITHER FLOATING OR CONNECTED TO GROUND.

Simple Diode Temperature Sensor

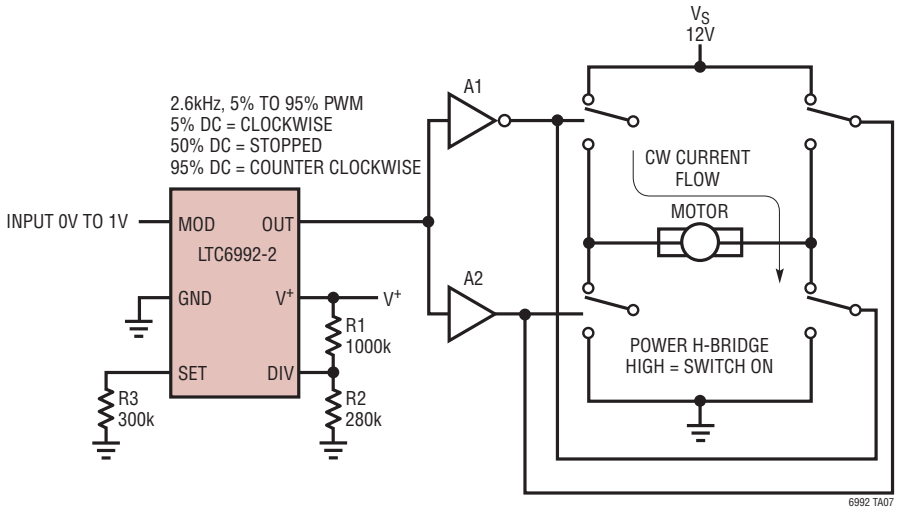


$N_{DIV} = 16$
f = 10kHz

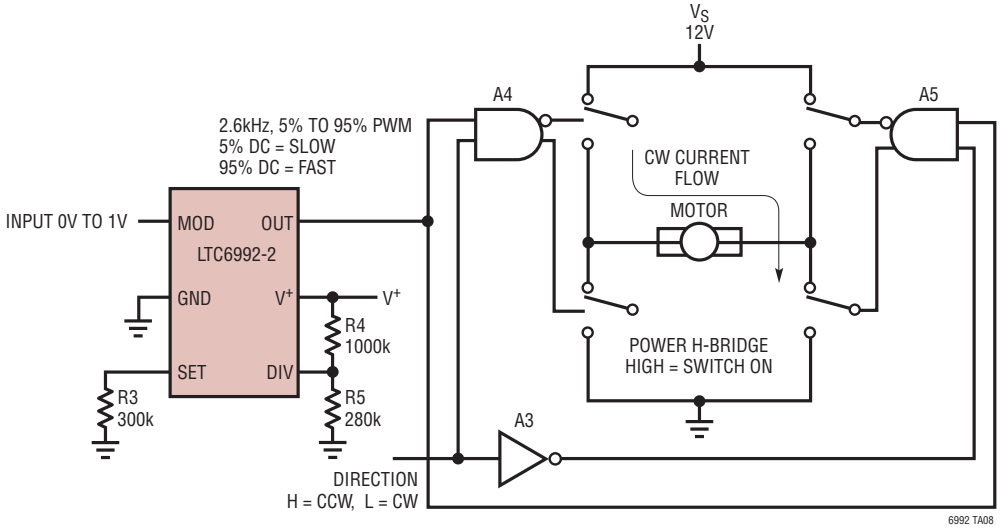
PWM OUTPUT FOR ISOLATED MEASUREMENT
+1% DUTY CYCLE CHANGE PER DEGREE C
–10°C TO 65°C RANGE WITH OPTO-ISOLATOR (DC: 15% TO 95%)

TYPICAL APPLICATIONS

Motor Speed/Direction Control for Full H-Bridge (Locked Anti-Phase Drive)

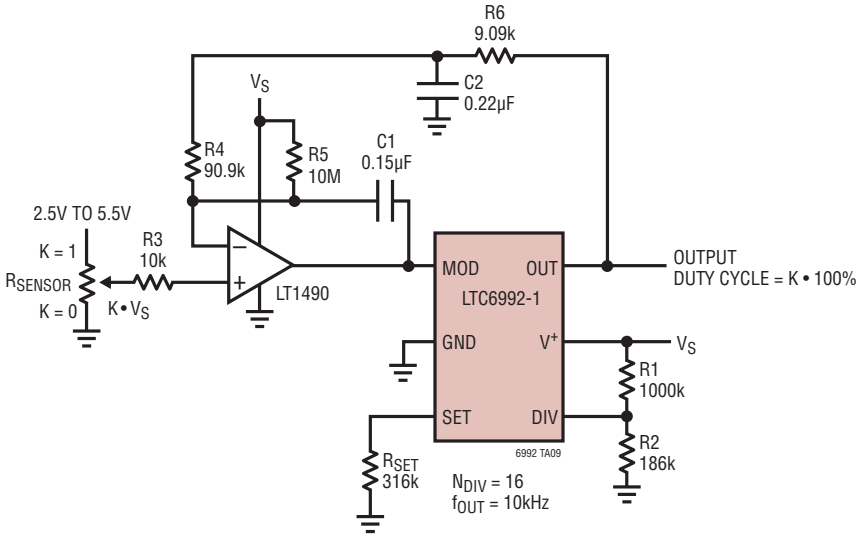


Motor Speed/Direction Control for Full H-Bridge (Sign/Magnitude Drive)

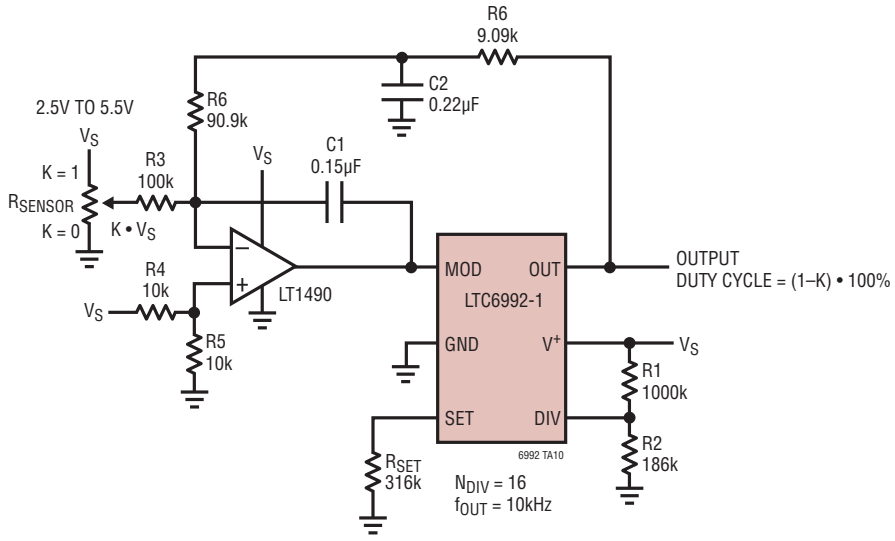


TYPICAL APPLICATIONS

Ratiometric Sensor to Pulse Width, Non-Inverting Response

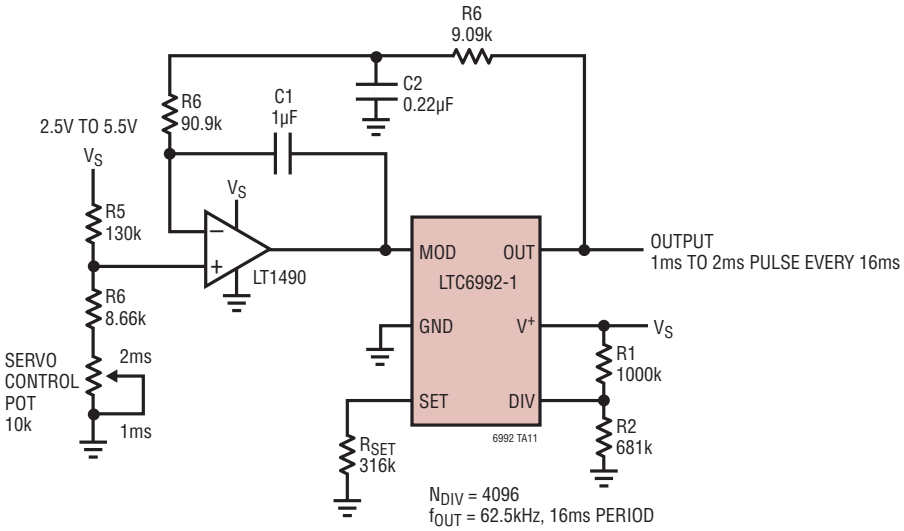


Ratiometric Sensor to Pulse Width, Inverting Response

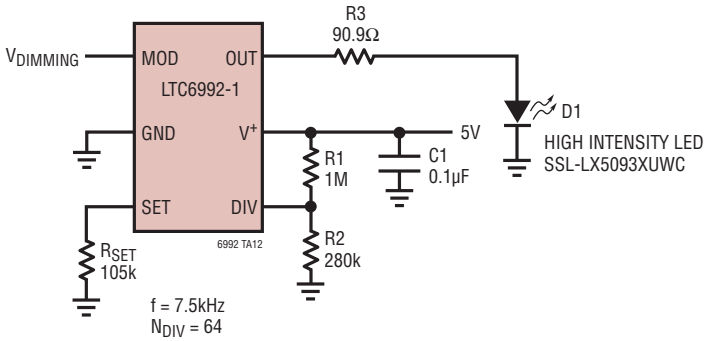


TYPICAL APPLICATIONS

Ratio Control Servo Pulse Generator

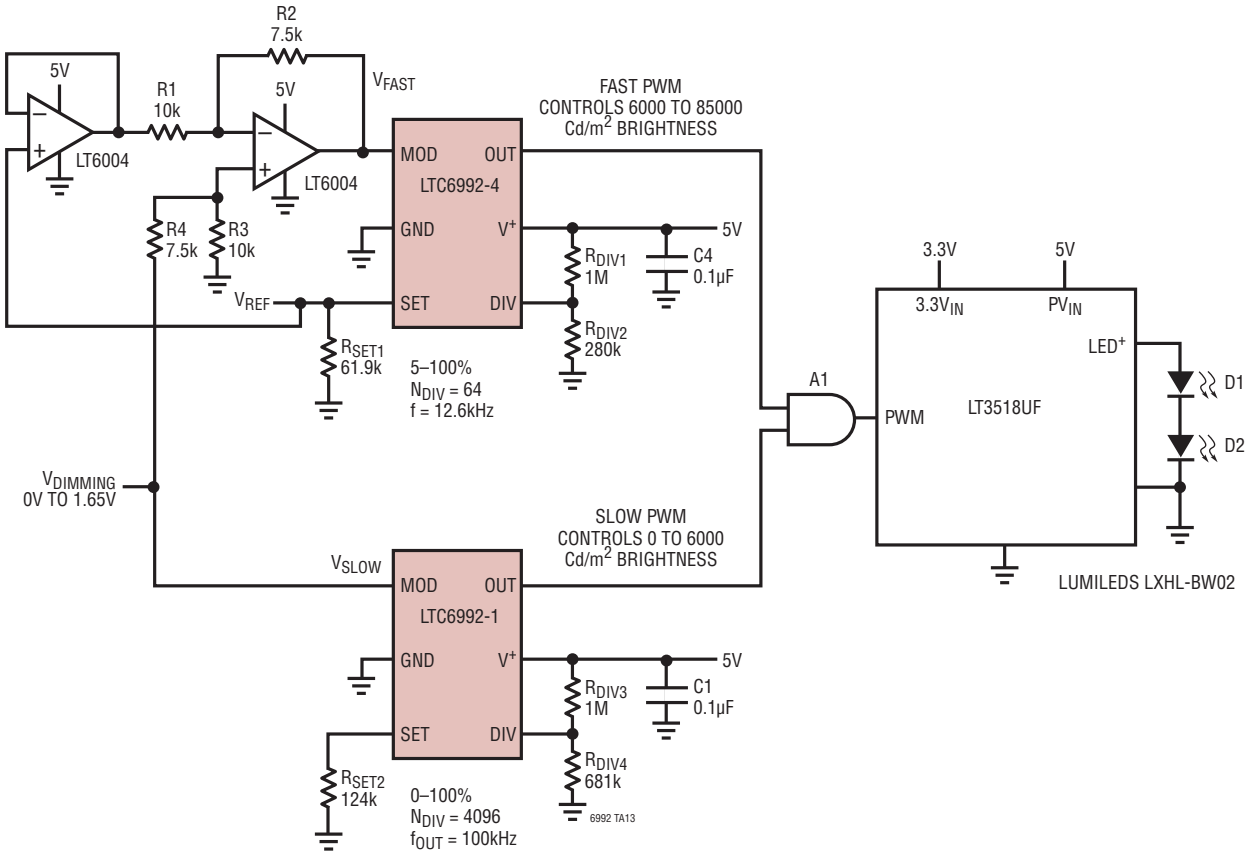


Direct Voltage Controlled PWM Dimming 0 to 15000 Cd/m^2 Intensity



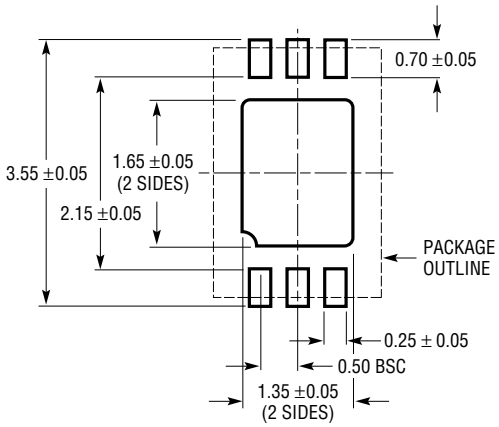
TYPICAL APPLICATIONS

Wide Range LED Dimming (0 to 85000 Cd/m^2 Brightness)

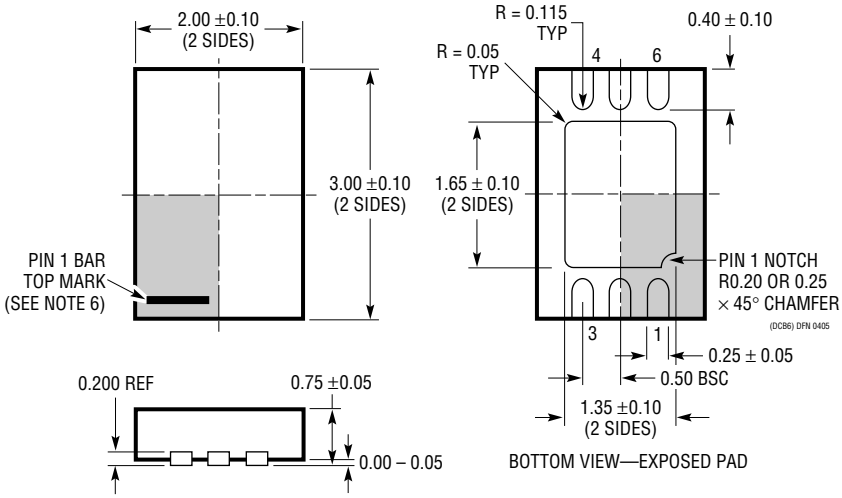


PACKAGE DESCRIPTION

DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

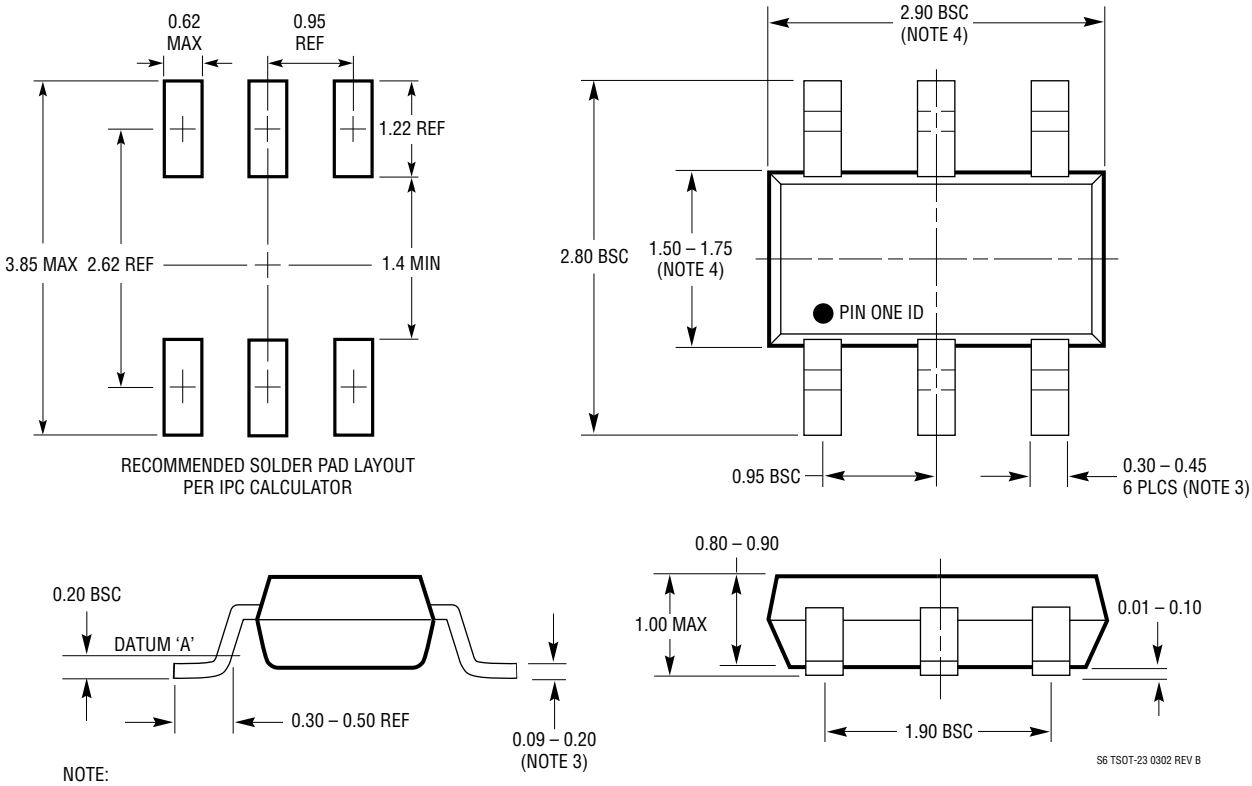


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636 Rev B)

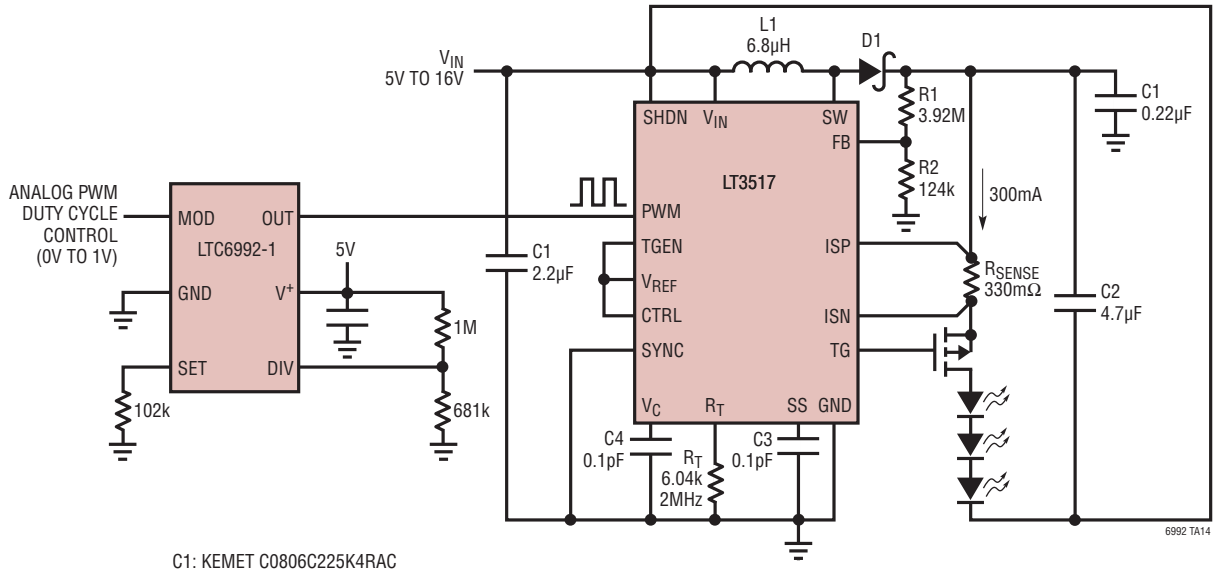


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

LED Driver with 5000:1 Dimming Range



C1: KEMET C0806C225K4RAC
C2: KEMET C1206C475K3RAC
C3, C4: MURATA GRM21BR71H104KA01B
C5: MURATA GRM21BR71H224KA01B
D1: DIODE DFL5160
L1: TOKO B992A5-6RBN
LEDS: LUXEON I (WHITE)
M1: ZETEX ZXMP6A13FTA

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1799	1MHz to 33MHz ThinSOT Silicon Oscillator	Wide Frequency Range
LTC6900	1MHz to 20MHz ThinSOT Silicon Oscillator	Low Power, Wide Frequency Range
LTC6906/LTC6907	10kHz to 1MHz or 40kHz ThinSOT Silicon Oscillator	Micropower, I_{SUPPLY} = 35µA at 400kHz
LTC6990	TimerBlox, Voltage Controlled Oscillator	Frequency from 488Hz to 1MHz, No Caps, 2% Accurate
LTC6991	TimerBlox, Very Low Frequency Clock with Reset	Cycle Time from 2ms to 9.5 Hours, No Caps, 2% Accurate
LTC6993-1	TimerBlox, Monostable Pulse Generator	Resistor Set Pulse Width from 1µs to 2ms, No Caps, 2% Accurate
LTC6993-2	TimerBlox, Retriggerable Monostable Pulse Generator	Resistor Set Pulse Width from 1µs to 2ms, No Caps, 2% Accurate
LTC6994-1	TimerBlox, Delay Block, First Edge Only Delayed	Resistor Set Delay from 1µs to 2ms, No Caps, 2% Accurate
LTC6994-2	TimerBlox, Delay Block/Debouncer, Both Edges Delayed	Resistor Set Delay from 1µs to 2ms, No Capacitors Required, 2% Accurate

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