- **Low Supply-Voltage Range, 1.8 V to 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 280 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 1.1 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Five Power Saving Modes**
- **Wake-Up From Standby Mode in 6 μs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **12-Bit A/D Converter With Internal Reference, Sample-and-Hold and Autoscan Feature**
- **16-Bit Timer With Three† or Seven‡ Capture/Compare-With-Shadow Registers, Timer_B**
- **16-Bit Timer With Three Capture/Compare Registers, Timer_A**
- **On-Chip Comparator**
- **Serial Communication Interface (USART), Select Asynchronous UART or Synchronous SPI by Software; Two USARTs (USART0, USART1) In MSP430x44x Devices One USART (USART0) In MSP430x43x Devices**
- **Brownout Detector**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Integrated LCD Driver for Up to 160 Segments**
- **Family Members Include:**
  - **MSP430F435: 16KB+256B Flash Memory, 512B RAM**
  - **MSP430F436: 24KB+256B Flash Memory, 1KB RAM**
  - **MSP430F437: 32KB+256B Flash Memory, 1KB RAM**
  - **MSP430F447: 32KB+256B Flash Memory, 1KB RAM**
  - **MSP430F448: 48KB+256B Flash Memory, 2KB RAM**
  - **MSP430F449: 60KB+256B Flash Memory, 2KB RAM**
- **For Complete Module Descriptions, See The MSP430x4xx Family User's Guide, Literature Number SLAU056**

† 'F435, 'F436, and 'F437 devices

‡ 'F447, 'F448, and 'F449 devices

description

The Texas Instruments MSP430 series is an ultralow-power microcontroller family consisting of several devices featuring different sets of modules targeted to various applications. The microcontroller is designed to be battery operated for use in extended-time applications. The MSP430 achieves maximum code efficiency with its 16-bit RISC architecture, 16-bit CPU-integrated registers, and a constant generator. The digitally-controlled oscillator provides wake-up from low-power mode to active mode in less than 6 μs. The MSP430x43x and the MSP430x44x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, one or two universal serial synchronous/asynchronous communication interfaces (USART), 48 I/O pins, and a liquid crystal driver (LCD) with up to 160 segments.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and process and transmit the data to a host system, or process this data and displays it on a LCD panel. The timers make the configurations ideal for industrial control applications such as ripple counters, digital motor control, EE-meters, hand-held meters, etc. The hardware multiplier enhances the performance and offers a broad code and hardware-compatible family solution.

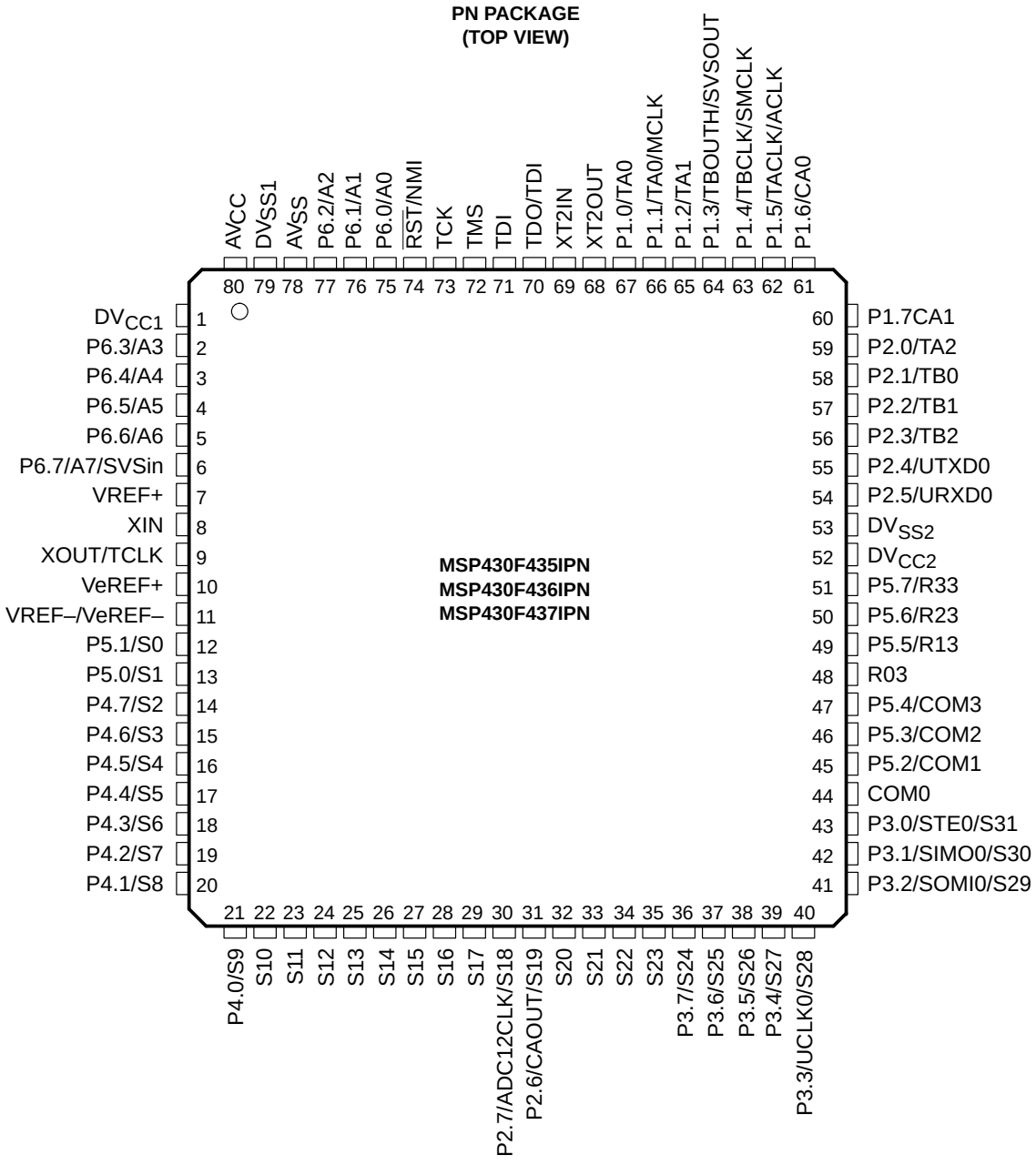
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC 80-PIN QFP (PN)	PLASTIC 100-PIN QFP (PZ)
–40°C to 85°C	MSP430F435IPN† MSP430F436IPN† MSP430F437IPN†	MSP430F435IPZ MSP430F436IPZ MSP430F437IPZ MSP430F447IPZ MSP430F448IPZ MSP430F449IPZ

† Advanced Information

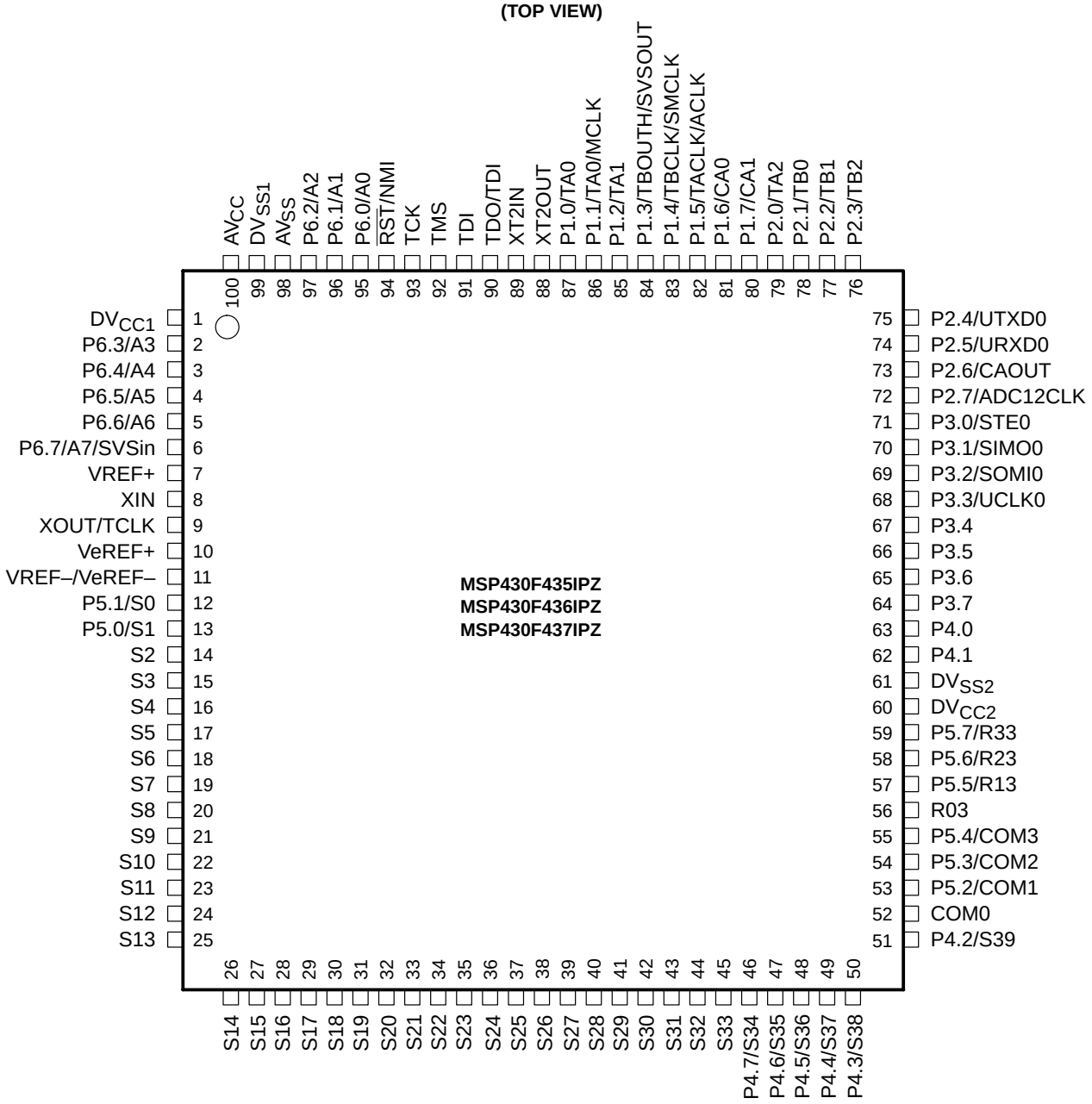
pin designation, MSP430x435IPN, MSP430x436IPN, MSP430x437IPN†

PN PACKAGE
(TOP VIEW)



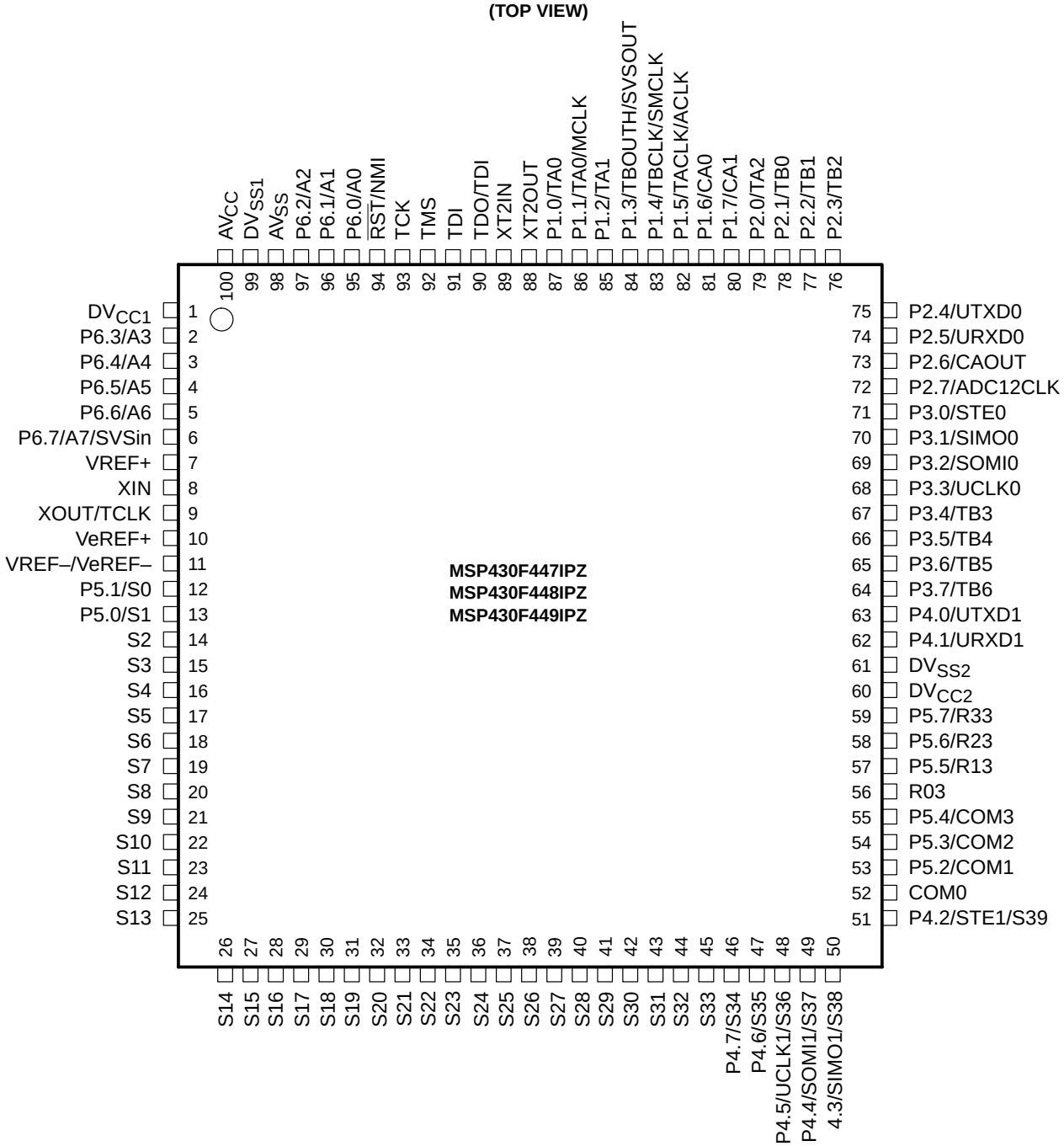
pin designation, MSP430x435IPZ, MSP430x436IPZ, MSP430x437IPZ

PZ PACKAGE
(TOP VIEW)

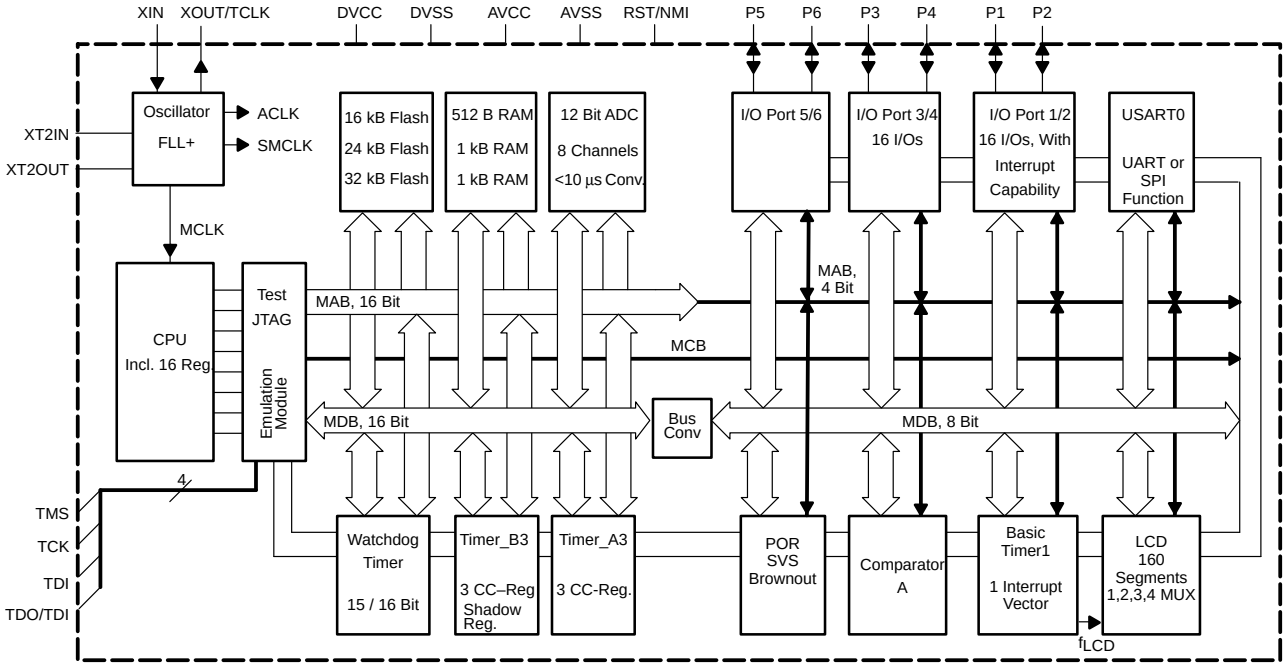


pin designation, MSP430x447IPZ, MSP430x448IPZ, MSP430x449IPZ

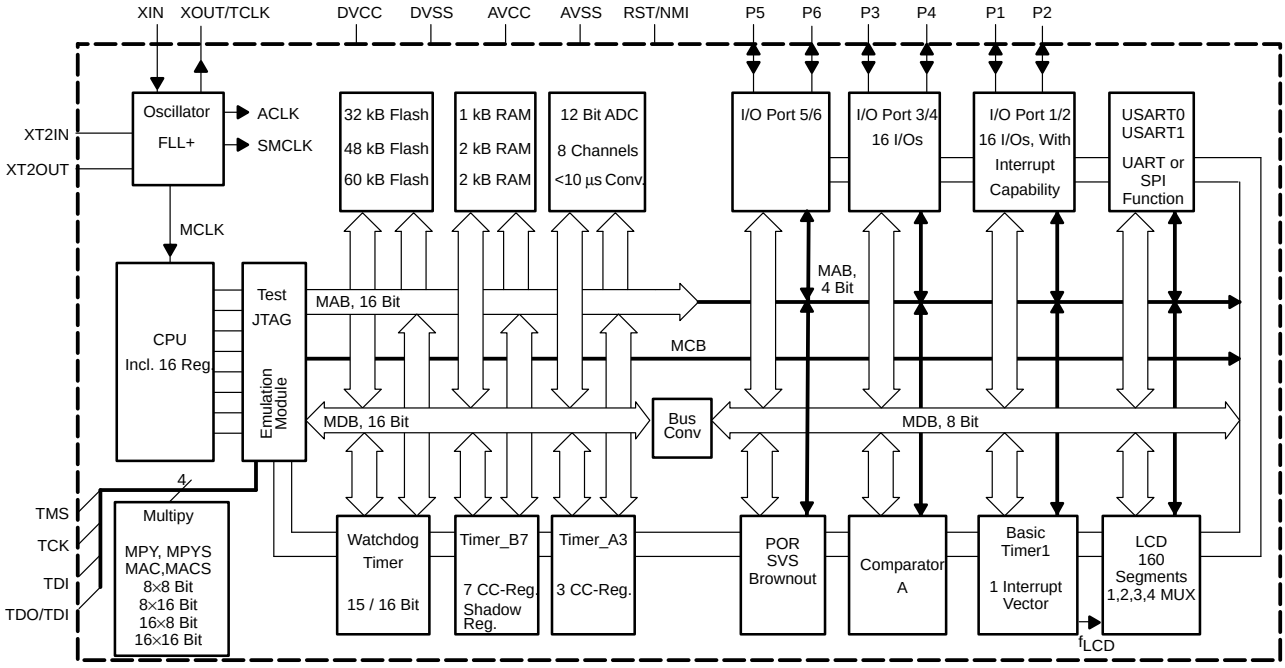
PZ PACKAGE
(TOP VIEW)



MSP430x43x functional block diagrams



MSP430x44x functional block diagrams



MSP430x43x Terminal Functions

TERMINAL					DESCRIPTION
PN		I/O	PZ		I/O	
NAME	NO.		NAME	NO.		
DV_{CC1}	1		DV_{CC1}	1		Digital supply voltage, positive terminal. Supplies all digital parts
P6.3/A3	2	I/O	P6.3/A3	2	I/O	General-purpose digital I/O, analog input a3—12-bit ADC
P6.4/A4	3	I/O	P6.4/A4	3	I/O	General-purpose digital I/O, analog input a4—12-bit ADC
P6.5/A5	4	I/O	P6.5/A5	4	I/O	General-purpose digital I/O, analog input a5—12-bit ADC
P6.6/A6	5	I/O	P6.6/A6	5	I/O	General-purpose digital I/O, analog input a6—12-bit ADC
P6.7/A7/SVSin	6	I/O	P6.7/A7/SVSin	6	I/O	General-purpose digital I/O, analog input a7—12-bit ADC, analog input to brownout, supply voltage supervisor
V_{REF+}	7	O	V_{REF+}	7	O	Output of positive terminal of the reference voltage in the ADC
XIN	8	I	XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT/TCLK	9	I/O	XOUT/TCLK	9	I/O	Output terminal of crystal oscillator XT1 or test clock input
Ve_{REF+}	10	I	Ve_{REF+}	10	I	Input for an external reference voltage to the ADC
V_{REF-}/Ve_{REF-}	11	I	V_{REF-}/Ve_{REF-}	11	I	Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage.
P5.1/S0	12	I/O	P5.1/S0	12	I/O	General-purpose I/O / LCD segment output 0
P5.0/S1	13	I/O	P5.0/S1	13	I/O	General-purpose I/O / LCD segment output 1
P4.7/S2	14	I/O	S2	14	O	General-purpose I/O / LCD segment output 2
P4.6/S3	15	I/O	S3	15	O	General-purpose I/O / LCD segment output 3
P4.5/S4	16	I/O	S4	16	O	General-purpose I/O / LCD segment output 4
P4.4/S5	17	I/O	S5	17	O	General-purpose I/O / LCD segment output 5
P4.3/S6	18	I/O	S6	18	O	General-purpose I/O / LCD segment output 6
P4.2/S7	19	I/O	S7	19	O	General-purpose I/O / LCD segment output 7
P4.1/S8	20	I/O	S8	20	O	General-purpose I/O / LCD segment output 8
P4.0/S9	21	I/O	S9	21	O	General-purpose I/O / LCD segment output 9
S10	22	O	S10	22	O	LCD segment output 10
S11	23	O	S11	23	O	LCD segment output 11
S12	24	O	S12	24	O	LCD segment output 12
S13	25	O	S13	25	O	LCD segment output 13
S14	26	O	S14	26	O	LCD segment output 14
S15	27	O	S15	27	O	LCD segment output 15
S16	28	O	S16	28	O	LCD segment output 16
S17	29	O	S17	29	O	LCD segment output 17
P2.7/ADC12CLK/ S18	30	I/O	S18	30	O	General-purpose digital I/O / conversion clock—12-bit ADC LCD segment output 18
P2.6/CAOUT/S19	31	I/O	S19	31	O	General-purpose digital I/O / Comparator_A output / LCD segment output 19
S20	32	O	S20	32	O	LCD segment output 20
S21	33	O	S21	33	O	LCD segment output 21
S22	34	O	S22	34	O	LCD segment output 22
S23	35	O	S23	35	O	LCD segment output 23
P3.7/S24	36	I/O	S24	36	O	General-purpose digital I/O / LCD segment output 24
P3.6/S25	37	I/O	S25	37	O	General-purpose digital I/O / LCD segment output 25
P3.5/S26	38	I/O	S26	38	O	General-purpose digital I/O / LCD segment output 26
P3.4/S27	39	I/O	S27	39	O	General-purpose digital I/O / LCD segment output 27

MSP430x43x Terminal Functions (Continued)

TERMINAL						DESCRIPTION
PN		I/O	PZ		I/O	
NAME	NO.		NAME	NO.		
P3.3/UCLK0/S28	40	I/O	S28	40	O	General-purpose digital I/O / ext. clock i/p—USART0/UART or SPI mode, clock o/p—USART0/SPI mode / LCD segment output 28
P3.2/SOMI0/S29	41	I/O	S29	41	O	General-purpose digital I/O / slave out/master in of USART0/SPI mode / LCD segment output 29
P3.1/SIMO0/S30	42	I/O	S30	42	O	General-purpose digital I/O / slave out/master out of USART0/SPI mode / LCD segment output 30
P3.0/STE0/S31	43	I/O	S31	43	O	General-purpose digital I/O / slave transmit enable-USART0/SPI mode / LCD segment output 31
			S32	44	O	LCD segment output 32
			S33	45	O	LCD segment output 33
			P4.7/S34	46	I/O	General-purpose digital I/O / LCD segment output 34
			P4.6/S35	47	I/O	General-purpose digital I/O / LCD segment output 35
			P4.5/S36	48	I/O	General-purpose digital I/O / LCD segment output 36
			P4.4/S37	49	I/O	General-purpose digital I/O / LCD segment output 37
			P4.3/S38	50	I/O	General-purpose digital I/O / LCD segment output 38
			P4.2/S39	51	I/O	General-purpose digital I/O / LCD segment output 39
COM0	44	O	COM0	52	O	COM0–3 are used for LCD backplanes.
P5.2/COM1	45	I/O	P5.2/COM1	53	I/O	General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.
P5.3/COM2	46	I/O	P5.3/COM2	54	I/O	General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.
P5.4/COM3	47	I/O	P5.4/COM3	55	I/O	General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.
R03	48	I	R03	56	I	Input port of fourth positive (lowest) analog LCD level (V5)
P5.5/R13	49	I/O	P5.5/R13	57	I/O	General-purpose digital I/O / input port of third most positive analog LCD level (V4 or V3)
P5.6/R23	50	I/O	P5.6/R23	58	I/O	General-purpose digital I/O / input port of second most positive analog LCD level (V2)
P5.7/R33	51	I/O	P5.7/R33	59	I/O	General-purpose digital I/O / output port of most positive analog LCD level (V1)
DV_{CC2}	52		DV_{CC2}	60		
DV_{SS2}	53		DV_{SS2}	61		
			P4.1	62	I/O	General-purpose digital I/O
			P4.0	63	I/O	General-purpose digital I/O
			P3.7	64	I/O	General-purpose digital I/O
			P3.6	65	I/O	General-purpose digital I/O
			P3.5	66	I/O	General-purpose digital I/O
			P3.4	67	I/O	General-purpose digital I/O
			P3.3/UCLK0	68	I/O	General-purpose digital I/O / external clock input—USART0/UART or SPI mode, clock output—USART0/SPI mode
			P3.2/SOMI0	69	I/O	General-purpose digital I/O / slave out/master in of USART0/SPI mode
			P3.1/SIMO0	70	I/O	General-purpose digital I/O / slave in/master out of USART0/SPI mode
			P3.0/STE0	71	I/O	General-purpose digital I/O / slave transmit enable USART0/SPI mode
			P2.7/ADC12CLK	72	I/O	General-purpose digital I/O / conversion clock—12-bit ADC
			P2.6/CAOUT	73	I/O	General-purpose digital I/O / Comparator_A output
P2.5/URXD0	54	I/O	P2.5/URXD0	74	I/O	General-purpose digital I/O / receive data in—USART0/UART mode

MSP430x43x Terminal Functions (Continued)

TERMINAL						DESCRIPTION
PN		I/O	PZ		I/O	
NAME	NO.		NAME	NO.		
P2.4/UTXD0	55	I/O	P2.4/UTXD0	75	I/O	General-purpose digital I/O / transmit data out—USART0/UART mode
P2.3/TB2	56	I/O	P2.3/TB2	76	I/O	General-purpose digital I/O / Timer_B3 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output
P2.2/TB1	57	I/O	P2.2/TB1	77	I/O	General-purpose digital I/O / Timer_B3 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output
P2.1/TB0	58	I/O	P2.1/TB0	78	I/O	General-purpose digital I/O / Timer_B3 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output
P2.0/TA2	59	I/O	P2.0/TA2	79	I/O	General-purpose digital I/O / Timer_A Capture: CCI2A input, compare: Out2 output
P1.7/CA1	60	I/O	P1.7/CA1	80	I/O	General-purpose digital I/O / Comparator_A input
P1.6/CA0	61	I/O	P1.6/CA0	81	I/O	General-purpose digital I/O / Comparator_A input
P1.5/TACLK/ ACLK	62	I/O	P1.5/TACLK/ ACLK	82	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8)
P1.4/TBCLK/ SMCLK	63	I/O	P1.4/TBCLK/ SMCLK	83	I/O	General-purpose digital I/O / input clock TBCLK—Timer_B3 / submain system clock SMCLK output
P1.3/TBOUTH/ SVSOUT	64	I/O	P1.3/TBOutH/ SVSOut	84	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance—Timer_B3 TB0 to TB2 / SVS: output of SVS comparator
P1.2/TA1	65	I/O	P1.2/TA1	85	I/O	General-purpose digital I/O / Timer_A, Capture: CCI1A, compare: Out1 output
P1.1/TA0/MCLK	66	I/O	P1.1/TA0/MCLK	86	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0B / MCLK output. Note: TA0 is only an input on this pin.
P1.0/TA0	67	I/O	P1.0/TA0	87	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output
XT2OUT	68	O	XT2OUT	88	O	Output terminal of crystal oscillator XT2
XT2IN	69	I	XT2IN	89	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
TDO/TDI	70	I/O	TDO/TDI	90	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TDI	71	I	TDI	91	I	Test data input. TDI is used as a data input port. The device protection fuse is connected to TDI.
TMS	72	I	TMS	92	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	73	I	TCK	93	I	Test clock. TCK is the clock input port for device programming and test.
$\overline{\text{RST}}$/NMI	74	I	$\overline{\text{RST}}$/NMI	94	I	General-purpose digital I/O / reset input or nonmaskable interrupt input port
P6.0/A0	75	I/O	P6.0/A0	95	I/O	General-purpose digital I/O / analog input a0 – 12-bit ADC
P6.1/A1	76	I/O	P6.1/A1	96	I/O	General-purpose digital I/O / analog input a1 – 12-bit ADC
P6.2/A2	77	I/O	P6.2/A2	97	I/O	General-purpose digital I/O / analog input a2 – 12-bit ADC
AV_{SS}	78		AV_{SS}	98		Negative terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1, and LCD resistive divider circuitry.
DV_{SS1}	79		DV_{SS1}	99		Digital supply voltage, negative terminal. Supplies all digital parts, except those which are supplied via AV_{CC}/AV_{SS}.
AV_{CC}	80		AV_{CC}	100		Positive terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DV_{CC1}/DV_{CC2}.

MSP430x44x Terminal Functions

TERMINAL PN NAME	NO.	I/O	DESCRIPTION
DV_{CC1}	1		Digital supply voltage, positive terminal. Supplies all digital parts
P6.3/A3	2	I/O	General-purpose digital I/O, analog input a3—12-bit ADC
P6.4/A4	3	I/O	General-purpose digital I/O, analog input a4—12-bit ADC
P6.5/A5	4	I/O	General-purpose digital I/O, analog input a5—12-bit ADC
P6.6/A6	5	I/O	General-purpose digital I/O, analog input a6—12-bit ADC
P6.7/A7/SVSin	6	I/O	General-purpose digital I/O, analog input a7—12-bit ADC, analog input to brownout, supply voltage supervisor
V_{REF+}	7	O	Output of positive terminal of the reference voltage in the ADC
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT/TCLK	9	I/O	Output terminal of crystal oscillator XT1 or test clock input
Ve_{REF+}	10	I	Input for an external reference voltage to the ADC
V_{REF-}/Ve_{REF-}	11	I	Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
P5.1/S0	12	O	General-purpose digital I/O, LCD segment output 0
P5.0/S1	13	O	General-purpose digital I/O, LCD segment output 1
S2	14	O	LCD segment output 2
S3	15	O	LCD segment output 3
S4	16	O	LCD segment output 4
S5	17	O	LCD segment output 5
S6	18	O	LCD segment output 6
S7	19	O	LCD segment output 7
S8	20	O	LCD segment output 8
S9	21	O	LCD segment output 9
S10	22	O	LCD segment output 10
S11	23	O	LCD segment output 11
S12	24	O	LCD segment output 12
S13	25	O	LCD segment output 13
S14	26	O	LCD segment output 14
S15	27	O	LCD segment output 15
S16	28	O	LCD segment output 16
S17	29	O	LCD segment output 17
S18	30	O	LCD segment output 18
S19	31	O	LCD segment output 19
S20	32	O	LCD segment output 20
S21	33	O	LCD segment output 21
S22	34	O	LCD segment output 22
S23	35	O	LCD segment output 23
S24	36	O	LCD segment output 24
S25	37	O	LCD segment output 25
S26	38	O	LCD segment output 26
S27	39	O	LCD segment output 27
S28	40	O	LCD segment output 28

MSP430x44x Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
PN NAME	NO.		
S29	41	O	LCD segment output 29
S30	42	O	LCD segment output 30
S31	43	O	LCD segment output 31
S32	44	O	LCD segment output 32
S33	45	O	LCD segment output 33
P4.7/S34	46	I/O	General-purpose digital I/O / LCD segment output 34
P4.6/S35	47	I/O	General-purpose digital I/O / LCD segment output 35
P4.5/UCLK1/S36	48	I/O	General-purpose digital I/O / external clock input—USART1/UART or SPI mode, clock output—USART1/SPI MODE / LCD segment output 36
P4.4/SOMI1/S37	49	I/O	General-purpose digital I/O / slave out/master in of USART1/SPI mode / LCD segment output 37
P4.3/SIMO1/S38	50	I/O	General-purpose digital I/O / slave in/master out of USART1/SPI mode / LCD segment output 38
P4.2/STE1/S39	51	I/O	General-purpose digital I/O / slave transmit enable—USART1/SPI mode / LCD segment output 39
COM0	52	O	COM0–3 are used for LCD backplanes.
P5.2/COM1	53	I/O	General-purpose digital I/O / Common output, COM0–3 are used for LCD backplanes.
P5.3/COM2	54	I/O	General-purpose digital I/O / Common output, COM0–3 are used for LCD backplanes.
P5.4/COM3	55	I/O	General-purpose digital I/O / Common output, COM0–3 are used for LCD backplanes.
R03	56	I	Input port of fourth positive (lowest) analog LCD level (V5)
P5.5/R13	57	I/O	General-purpose digital I/O / Input port of third most positive analog LCD level (V4 or V3)
P5.6/R23	58	I/O	General-purpose digital I/O / Input port of second most positive analog LCD level (V2)
P5.7/R33	59	I/O	General-purpose digital I/O / Output port of most positive analog LCD level (V1)
DV_{CC2}	60		
DV_{SS2}	61		
P4.1/URXD1	62	I/O	General-purpose digital I/O / receive data in—USART1/UART mode
P4.0/UTXD1	63	I/O	General-purpose digital I/O / transmit data out—USART1/UART mode
P3.7/TB6	64	I/O	General-purpose digital I/O / Timer_B7 CCR6 / Capture: CCI6A/CCI6B input, compare: Out6 output
P3.6/TB5	65	I/O	General-purpose digital I/O / Timer_B7 CCR5 / Capture: CCI5A/CCI5B input, compare: Out5 output
P3.5/TB4	66	I/O	General-purpose digital I/O / Timer_B7 CCR4 / Capture: CCI4A/CCI4B input, compare: Out4 output
P3.4/TB3	67	I/O	General-purpose digital I/O / Timer_B7 CCR3 / Capture: CCI3A/CCI3B input, compare: Out3 output
P3.3/UCLK0	68	I/O	General-purpose digital I/O / external clock input—USART0/UART or SPI mode, clock output—USART0/SPI mode
P3.2/SOMI0	69	I/O	General-purpose digital I/O / slave out/master in of USART0/SPI mode
P3.1/SIMO0	70	I/O	General-purpose digital I/O / slave in/master out of USART0/SPI mode
P3.0/STE0	71	I/O	General-purpose digital I/O / slave transmit enable—USART0/SPI mode
P2.7/ADC12CLK	72	I/O	General-purpose digital I/O / conversion clock—12-bit ADC
P2.6/CAOUT	73	I/O	General-purpose digital I/O / Comparator_A output
P2.5/URXD0	74	I/O	General-purpose digital I/O / receive data in—USART0/UART mode
P2.4/UTXD0	75	I/O	General-purpose digital I/O / transmit data out—USART0/UART mode
P2.3/TB2	76	I/O	General-purpose digital I/O / Timer_B7 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output
P2.2/TB1	77	I/O	General-purpose digital I/O / Timer_B7 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output
P2.1/TB0	78	I/O	General-purpose digital I/O / Timer_B7 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output
P2.0/TA2	79	I/O	General-purpose digital I/O / Timer_A Capture: CCI2A input, compare: Out2 output
P1.7/CA1	80	I/O	General-purpose digital I/O / Comparator_A input

MSP430x44x Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
PN NAME	NO.		
P1.6/CA0	81	I/O	General-purpose digital I/O / Comparator_A input
P1.5/TACLK/ ACLK	82	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8)
P1.4/TBCLK/ SMCLK	83	I/O	General-purpose digital I/O / input clock TBCLK—Timer_B7 / submain system clock SMCLK output
P1.3/TBOutH/ SVSOut	84	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance—Timer_B7 TB0 to TB6 / SVS: output of SVS comparator
P1.2/TA1	85	I/O	General-purpose digital I/O / Timer_A, Capture: CCI1A, compare: Out1 output
P1.1/TA0/MCLK	86	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0B / MCLK output. Note: TA0 is only an input on this pin.
P1.0/TA0	87	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output
XT2OUT	88	O	Output terminal of crystal oscillator XT2
XT2IN	89	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
TDO/TDI	90	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TDI	91	I	Test data input. TDI is used as a data input port. The device protection fuse is connected to TDI.
TMS	92	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	93	I	Test clock. TCK is the clock input port for device programming and test.
$\overline{\text{RST}}$/NMI	94	I	Reset input or nonmaskable interrupt input port
P6.0/A0	95	I/O	General-purpose digital I/O, analog input a0—12-bit ADC
P6.1/A1	96	I/O	General-purpose digital I/O, analog input a1—12-bit ADC
P6.2/A2	97	I/O	General-purpose digital I/O, analog input a2—12-bit ADC
AV_{SS}	98		Negative terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1, and LCD resistive divider circuitry.
DV_{SS1}	99		Digital supply voltage, negative terminal. Supplies all digital parts, except those which are supplied via AV_{CC}/AV_{SS}.
AV_{CC}	100		Positive terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DV_{CC1}/DV_{CC2}.

short-form description

processing unit

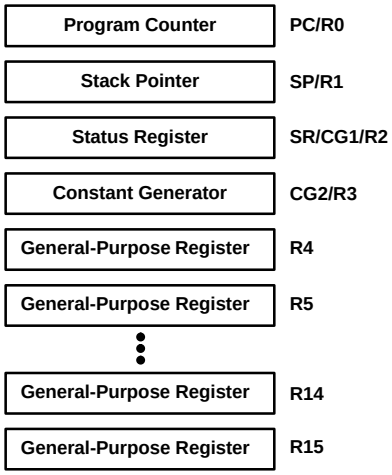
The processing unit is based on a consistent and orthogonal CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development and notable for its ease of programming. All operations, other than program-flow instructions, are consequently performed as register operations in conjunction with seven addressing modes for source and four modes for destination operand.

CPU

The CPU has 16 registers that provide reduced instruction execution time. This reduces the register-to-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as program counter, stack pointer, status register, and constant generator. The remaining registers are available as general-purpose registers.

Peripherals are connected to the CPU using a data address and control bus, and can be easily handled with all memory manipulation instructions.



instruction set

The instruction set for this register-to-register architecture constitutes a powerful and easy-to-use assembler language. The instruction set consists of 51 instructions with three formats and seven address modes. Table 1 provides a summary and example of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ——> R5
Single operands, destination only	e.g. CALL R8	PC —>(TOS), R8—> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Each instruction operating on word and byte data is identified by the suffix B.

Examples:	WORD INSTRUCTIONS		BYTE INSTRUCTIONS	
	MOV	EDE, TONI	MOV.B	EDE,TONI
	ADD	#235h, and MEM	ADD.B	#35h, and MEM
	PUSH	R5	PUSH.B	R5
	SWPB	R5	—	

instruction set (continued)

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	✓	✓	MOV and MEM,and TCDAT		M(MEM) —> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

Computed branches (BR) and subroutine call (CALL) instructions use the same address modes as other instructions. These address modes provide *indirect* addressing, which is ideally suited for computed branches and calls. The full use of this programming capability results in a program structure which is different from structures used with conventional 8- and 16-bit controllers. For example, numerous routines can be easily designed to deal with pointers and stacks instead of using flag-type programs for flow control.

operating modes

The MSP430 operating modes support various advanced requirements for ultralow power and ultralow energy consumption. The intelligent management of the operations during the different module operation modes and CPU states achieves this. The requirements are fully supported during interrupt event handling. An interrupt event awakens the system from each of the various operating modes and returns with the RETI instruction to the mode that was selected before the interrupt event. The clocks used are ACLK, SMCLK and MCLK.

ACLK is the crystal frequency, MCLK and SMCLK are either multiples of ACLK or come from the crystal oscillators. MCLK and SMCLK are used as the system clock and subsystem clock.

The software can configure six operating modes:

- Active mode AM; SCG1=0, SCG0=0, OscOff=0, CPUOff=0:
  CPU clocks are active
- Low-power mode 0 (LPM0); SCG1=0, SCG0=0, OscOff=0, CPUOff=1:
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
    FLL+ Loop control remains active
- Low-power mode 1 (LPM1); SCG1=0, SCG0=1, OscOff=0, CPUOff=1:
  - CPU is disabled
    FLL+ Loop control is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 2 (LPM2); SCG1=1, SCG0=0, OscOff=0, CPUOff=1:
  - CPU is disabled
    MCLK and FLL+ loop control and DCOCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active

operating modes (continued)

- Low-power mode 3 (LPM3); SCG1=1, SCG0=1, OscOff=0, CPUOff=1:
  - CPU is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4); SCG1=X, SCG0=X, OscOff=1, CPUOff=1:
  - CPU is disabled
    ACLK is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

SMCLK is disabled with SMCLKOFF bit in register FLL+CTL1 (054h). The selected clock source (DCOCLK or XT2CLK) can be switched off only if SMCLKOFF = 1.

NOTE:
Peripheral operation is not halted by CPUOff. Peripherals are controlled by their individual control registers.

The various operating modes are controlled by the software through control of the internal clock system operation. This clock system gives a large combination of hardware and software capabilities to run the application with the lowest power consumption and with optimized system costs:

- Use of the internal clock (DCO) generator without any external components
- Selection of an external crystal or ceramic resonator for lowest frequency and cost
- Application of an external clock source

The control bits that most influence the operation of the clock system and support fast turnon from low power operating modes are located in the status register SR. Four bits control the CPU and the system clock generator: SCG1, SCG0, OscOff, and CPUOff.

15 – 9	8	7							0
Reserved for Future Enhancements	V	SCG1	SCG0	OscOff	CPUOff	GIE	N	Z	C
rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0

CPUOff, SCG1, SCG0, and OscOff are the most important bits in low-power control when the basic function of the system clock generator is established. They are pushed to the stack whenever an interrupt is accepted and saved for returning to the operation before an interrupt request. They can be manipulated via indirect access to the data on the stack during execution of an interrupt handler so that program execution can resume in another power operating mode after return-from-interrupt.

CPUOff:	The CPUOff bit, when set, disables CPU (MCLK is disabled).
SCG0:	The SCG0 bit, when set, disables the FLL+ loop control.
SCG1:	The SCG1 bit, when set, disables the DCOCLK signal.
OscOff:	The OscOff bit, when set, disables the LFXT1 crystal oscillator.
DC generator:	When both SCG0 and SCG1 are set, the dc generator for the DCO is disabled.
XT2Off:	The XT2Off bit, when set, disables the XT2 crystal oscillator. XT2 is disabled only if it is unused for MCLK (SELM≠2 or CPUOff=1) and if it is unused for SMCLK (SELS=0 or SMCLKOFF=1). Both conditions prevent disabling of XT2 accidentially.
SMCLKOFF:	SMCLKOFF, when set, switches off clock SMCLK.

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 3. Interrupt Sources, Flags, and Vectors of 4xx Configurations

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash memory access violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1 and 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer_B7†	CCIFG0 (see Note 2)	Maskable	0FFFAh	13
Timer_B7†	CCIFG1 to CCIFG6 TBIFG (see Notes 1 and 2)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog Timer	WDTIFG	Maskable	0FFF4h	10
USART0 receive	URXIFG0	Maskable	0FFF2h	9
USART0 transmit	UTXIFG0	Maskable	0FFF0h	8
ADC	ADCIFG (see Notes 1 and 2)	Maskable	0FFEEh	7
Timer_A3	CCIFG0 (see Note 2)	Maskable	0FFECh	6
Timer_A3	CCIFG1, CCIFG2, TAIFG (see Notes 1 and 2)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 (see Notes 1 and 2) To P1IFG.7 (see Notes 1 and 2)	Maskable	0FFE8h	4
USART1 receive‡	URXIFG1	Maskable	0FFE6h	3
USART1 transmit‡	UTXIFG1	Maskable	0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 (see Notes 1 and 2) To P2IFG.7 (see Notes 1 and 2)	Maskable	0FFE2h	1
Basic Timer1	BTIFG	Maskable	0FFE0h	0, lowest

‡ ’43x uses Timer_B3 with CCIFG0, CCIFG1 to CCIFG2 flags, and TBIFG. ’44x uses Timer_B7 with CCIFG0, CCIFG1 to CCIFG6, and TBIFG
‡ USART1 is implemented in ’44x only.

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable can not disable it.

special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h	UTXIE0	URXIE0	ACCVIE	NMIIE			OFIE	WDTIE
	rw–0	rw–0	rw–0	rw–0			rw–0	rw–0

WDTIE: Watchdog-timer-interrupt enable signal

OFIE: Oscillator-fault-interrupt enable signal

NMIIE: Nonmaskable-interrupt enable signal

ACCVIE: (Non)maskable-interrupt enable signal, access violation if FLASH memory/module is busy

URXIE0: USART0, UART, and SPI receive-interrupt enable signal

UTXIE0: USART0, UART, and SPI transmit-interrupt enable signal

Address	7	6	5	4	3	2	1	0
01h	BTIE		UTXIE1	URXIE1				
	rw–0		rw–0	rw–0				

URXIE1: USART1, UART, and SPI receive-interrupt enable signal (MSP430F44x devices only)

UTXIE1: USART1, UART, and SPI transmit-interrupt enable signal (MSP430F44x devices only)

BTIE: Basic timer interrupt enable signal

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h	UTXIFG0	URXIFG0		NMIIFG			OFIFG	WDTIFG
	rw–1	rw–0		rw–0			rw–1	rw–0

WDTIFG: Set on overflow or security key violation or reset on VCC power-on or reset condition at $\overline{\text{RST}}$/NMI

OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{\text{RST}}$/NMI pin

URXIFG0: USART0, UART, and SPI receive flag

UTXIFG0: USART0, UART, and SPI transmit flag

Address	7	6	5	4	3	2	1	0
03h	BTIFG		UTXIFG1	URXIFG1				
	rw		rw–1	rw–0				

URXIFG1: USART1, UART, and SPI receive flag (MSP430F44x devices only)

UTXIFG1: USART1, UART, and SPI transmit flag (MSP430F44x devices only)

BTIFG: Basic timer flag

module enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h	UTXE0	URXE0 USPIE0						
	rw–0	rw–0						

URXE0: USART0, UART receive enable

UTXE0: USART0, UART transmit enable

USPIE0: USART0, SPI (synchronous peripheral interface) transmit and receive enable

Address	7	6	5	4	3	2	1	0
05h			UTXE1	URXE1 USPIE1				
			rw–0	rw–0				

URXE1: USART1, UART receive enable (MSP430F44x devices only)

UTXE1: USART1, UART transmit enable (MSP430F44x devices only)

USPIE1: USART1, SPI (synchronous peripheral interface) transmit and receive enable (MSP430F44x devices only)

Legend: rw: **Bit Can Be Read and Written**
rw–0: **Bit Can Be Read and Written. It Is Reset by PUC.**
SFR Bit Not Present in Device

memory organization

		MSP430F435	MSP430F436	MSP430F437 MSP430F447	MSP430F448	MSP430F449
Memory Main: interrupt vector Main: code memory	Size Flash Flash	16KB 0FFFFh – 0FFE0h 0FFFFh – 0C000h	24KB 0FFFFh – 0FFE0h 0FFFFh – 0A000h	32KB 0FFFFh – 0FFE0h 0FFFFh – 08000h	48KB 0FFFFh – 0FFE0h 0FFFFh – 04000h	60KB 0FFFFh – 0FFE0h 0FFFFh – 01100h
Information memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size ROM	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h
RAM	Size	512 Byte 03FFh – 0200h	1KB 05FFh – 0200h	1KB 05FFh – 0200h	2KB 09FFh – 0200h	2KB 09FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

boot ROM containing bootstrap loader

The intention of the bootstrap loader is to download data into the flash memory module. Various write, read, and erase operations are needed for a proper download environment.

functions of the bootstrap loader:

Definition of read: Apply data to pin P1.0/TA0 (BSLTX) and transmit peripheral registers or memory data to pin P1.0/TA0.

write: Read data from pin P1.1/TA0/MCLK (BSLRX) and write it to flash memory.

boot ROM containing bootstrap loader (continued)

unprotected functions

Mass erase, erase of the main memory (segment 0 to segment n)

Access to the MSP430 via the bootstrap loader is protected. It must be enabled before any protected function can be performed. The 256 bits in 0FFE0h to 0FFFFh provide the access key.

protected functions

All protected functions can be executed only if the access is enabled.

- Write/program byte into flash memory. The parameters passed are start address and number of bytes (the flash segment-write feature of the flash memory is not supported and not used with the UART protocol).
- Segment erase of segment 0 to segment n in main memory, and segment erase of segments A and B in the information memory
- Reading of all data in main memory and information memory
- Reading and writing to all peripheral modules and RAM
- Modifying PC and start program execution immediately

NOTE:
Unauthorized readout of code and data is prevented by the user's definition of the data in the interrupt memory locations.

features of the bootstrap loader are:

- UART communication protocol, fixed to 9600 baud
- Port pin P1.0/TA0 for transmit, P1.1/TA0/MCLK for receive
- TI standard serial protocol definition
- Loader implemented in flash memory version only
- Program execution starts with the user vector at 0FFFEh or with the bootstrap loader (address 0C00h)

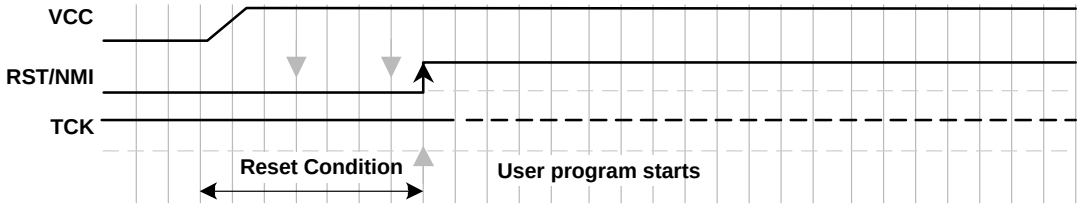
hardware resources used for serial input/output:

- Pins P1.0/TA0 and P1.1/TA0/MCLK for serial data transmission
- TCK and $\overline{\text{RST}}$/NMI to start program execution at the reset or bootstrap loader vector
- FLL+ module: SCFI0=0, SCFI1=098h, SCG0=1
- Timer_A: Timer_A operates in continuous mode with SMCLK source selected, input divider set to 1, and using CCR0 and polling CCIFG0.
- WDT: Watchdog Timer is halted
- Interrupt: GIE=0, NMIIE=0, OFIFG=0, ACCVIFG=0
- Using the stack depends on the start condition:
  Starting via RST/NMI and TCK pin: 6 bytes used, stack pointer initialized to 220h
  Start via SW (e.g., BR &0C02h): 6 bytes used, on top of the actual stack pointer
- RAM: 20 bytes used, start at address 0200h, last address used: 0219h

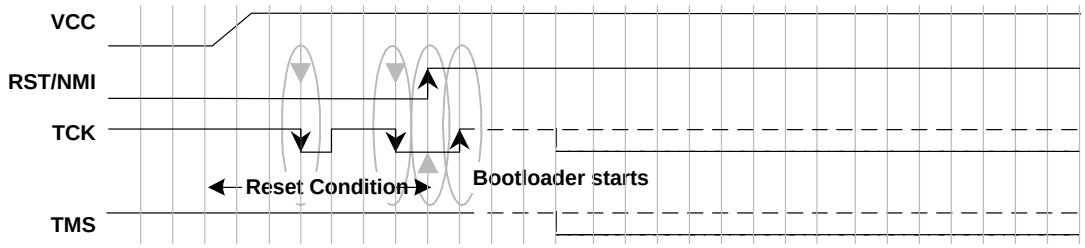
NOTE:
When writing RAM data via the bootstrap loader, make sure the stack is outside the range of data to be written.

Program execution begins with the user's reset vector at FFFEh (standard method) if TCK is held high while RST/NMI goes from low to high.

boot ROM containing bootstrap loader (continued)



Program execution begins with the bootstrap vector at 0C00h (boot ROM) if TCK has applied a minimum of two negative edges at signal/pin TCK, and if TCK is low while RST/NMI goes from low to high.



NOTES: 4. The default level of TCK is high. An active low has to be applied to enter the bootstrap loader. Other MSP430s which have a pin function used with a low default level can use an inverted signal.
5. The TMS signal must be high while TCK clocks are applied. This ensures that the JTAG controller function remains in its default mode.

The bootstrap loader does not start (via the vector in address 0C00h) if:

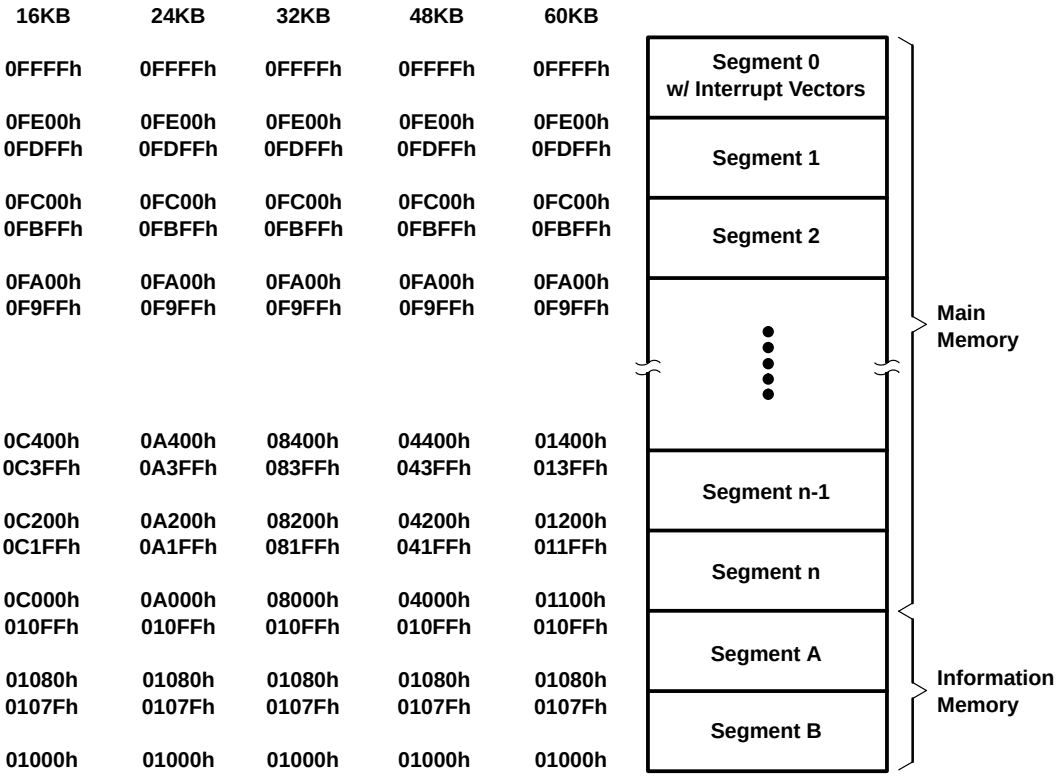
- There are less than two negative edges at TCK while RST/NMI is low
- TCK is high when RST/NMI goes from low to high
- JTAG has control over the MSP430 resources
- The supply voltage V_{CC} drops and a POR is executed
- RST/NMI pin is configured for NMI function (NMI bit is set)

flash memory

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n.
  Segments A and B are also called *information memory.*
- A security fuse burning is irreversible; no further access to JTAG is possible afterwards.
- Internal generation of the programming/erase voltage: no external V_{PP} has to be applied, but V_{CC} increases the supply current requirements.
- Program and erase timing is controlled by hardware in the flash memory – no software intervention is needed.
- The control hardware is called the flash-timing generator. The input frequency of the flash-timing generator should be in the proper range and should be maintained until the write/program or erase operation is completed.

flash memory (continued)

- During program or erase, no code can be executed from flash memory and all interrupts must be disabled by setting the GIE, NMIIE, ACCVIE, and OFIE bits to zero. If a user program requires execution concurrent with a flash program or erase operation, the program must be executed from memory other than the flash memory (e.g., boot ROM, RAM). In the event a flash program or erase operation is initiated while the program counter is pointing to the flash memory, the CPU will execute JMP $ instructions until the flash program or erase operation is completed. Normal execution of the previously running software then resumes.
- Unprogrammed, new devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



flash memory, control register FCTL1, FCTL2, and FCTL3

All control bits are reset during PUC. PUC is active after VCC is applied, a reset condition is applied to the RST/NMI pin or the Watchdog Timer expires, a watchdog access violation occurs, or an improper flash operation has been performed. Any write to control register FCTL1 during erase, mass erase, or write (programming) ends in an access violation with ACCVIFG=1. In an active segment write mode the control register may be written if wait mode is active (WAIT=1). Read access is possible at any time without restrictions.

The control bits of control register FCTL1 hold all bits that apply write (programming) or erase modes. Writing to the control register requires key word 0A5H in the *high-byte*. Any other data there generates a power-up clear (PUC) which resets the controller.

flash memory, control register FCTL1, FCTL2, and FCTL3 (continued)

FCTL1, 0128h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								SEG WRT	WRT	res.	res.	res.	MEras	Erase	res.
								rw–0	rw–0	r–0	r–0	r–0	rw–0	rw–0	r–0

FCTL1 Read: 096h
FCTL1 Write: 0A5h

The bits control erase or mass erase of the flash, write (WRT), programming, or segment write (SEGWRT).

The control register FCTL2 determines the operation of the timing generator that generates all the timing signals necessary for write, erase, and mass erase from the selected clock source. One of three different clock sources may be selected. The selected clock source must be divided to meet the frequency requirements specified in the recommended operating conditions.

NOTE:

The mass erase duration generated by the flash timing generator is at least 11.1 ms. The cumulative mass erase time needed is 200 ms. This can be achieved by repeating the mass erase operation until the cumulative mass erase time is met (a minimum of 19 cycles may be required).

FCTL2, 012Ah

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								SSEL1	SSEL0	FN5	FN4	FN3	FN2	FN1	FN0
								rw–0	rw–1	rw–0	rw–0	rw–0	rw–0	rw–1	rw–0

FCTL2 Read: 096h
FCTL2 Write: 0A5h

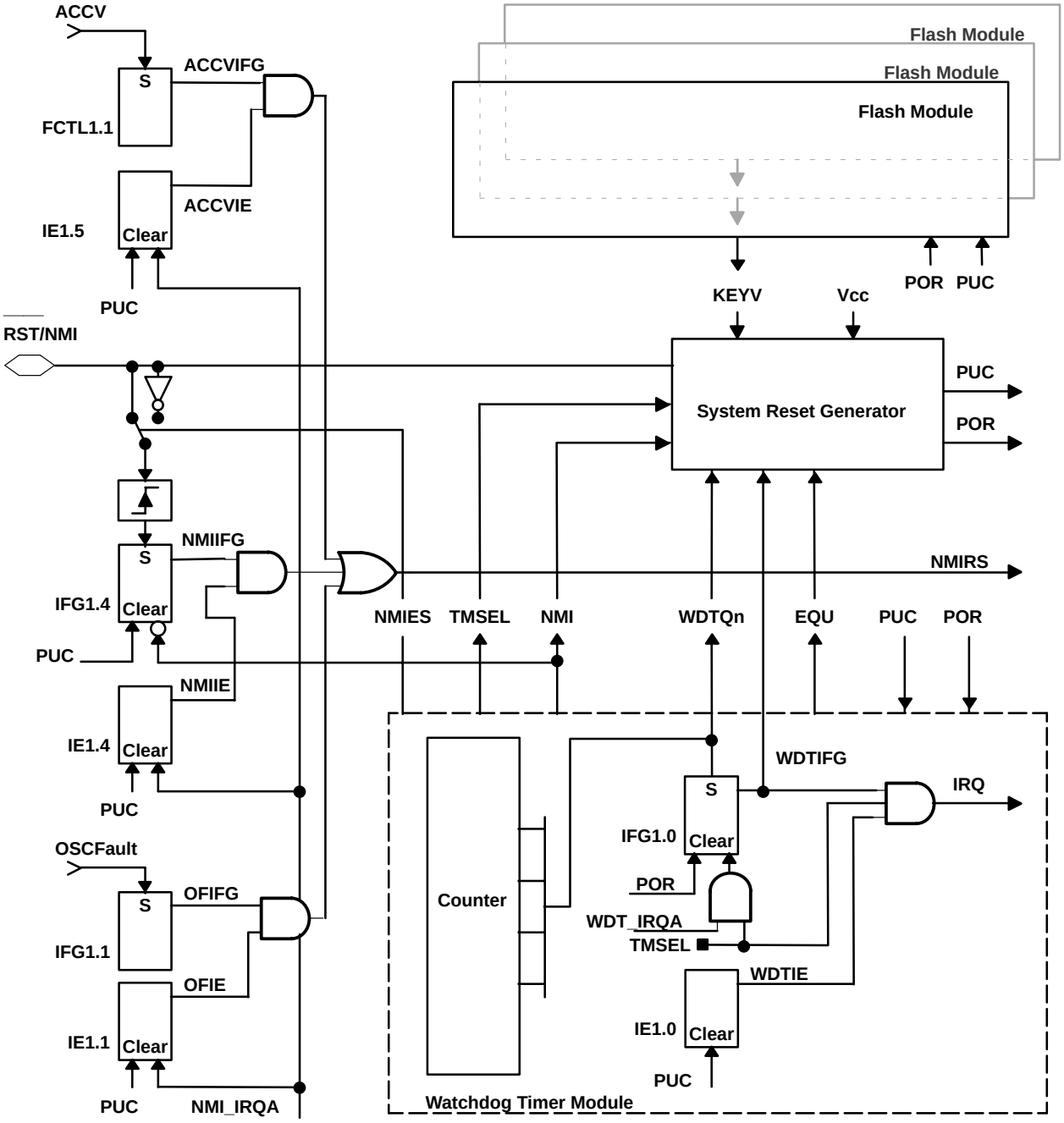
Control register FCTL3 determines the access and flags the status and error conditions of the flash operation. There are no restrictions to modify this control register. Control bits are reset or set (WAIT) with PUC but key violation bit KEYV is reset with POR.

FCTL3, 012Ch

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								res.	res.	EMEX	Lock	WAIT	ACCV IFG	KEYV	BUSY
								r–0	r–0	rw–0	rw–1	r–1	rw–0	rw–(0)	r(w)–0

FCTL3 Read: 096h
FCTL3 Write: 0A5h

flash memory, interrupt and security key violation



IRQA: Interrupt request accepted

Figure 1. Block Diagram of NMI Interrupt Sources

One NMI vector is used for three NMI events: RST/NMI (NMIIFG), oscillator fault (OFIFG), and flash memory access violation (ACCVIFG). The software can determine the source of the interrupt request since all flags remain set until they are reset by the software. The enable flag(s) must be set only within one instruction directly before the return-from-interrupt (RETI) instruction. This ensures that the stack remains under control. A pending NMI interrupt request does not increase stack demand unnecessarily.

peripherals

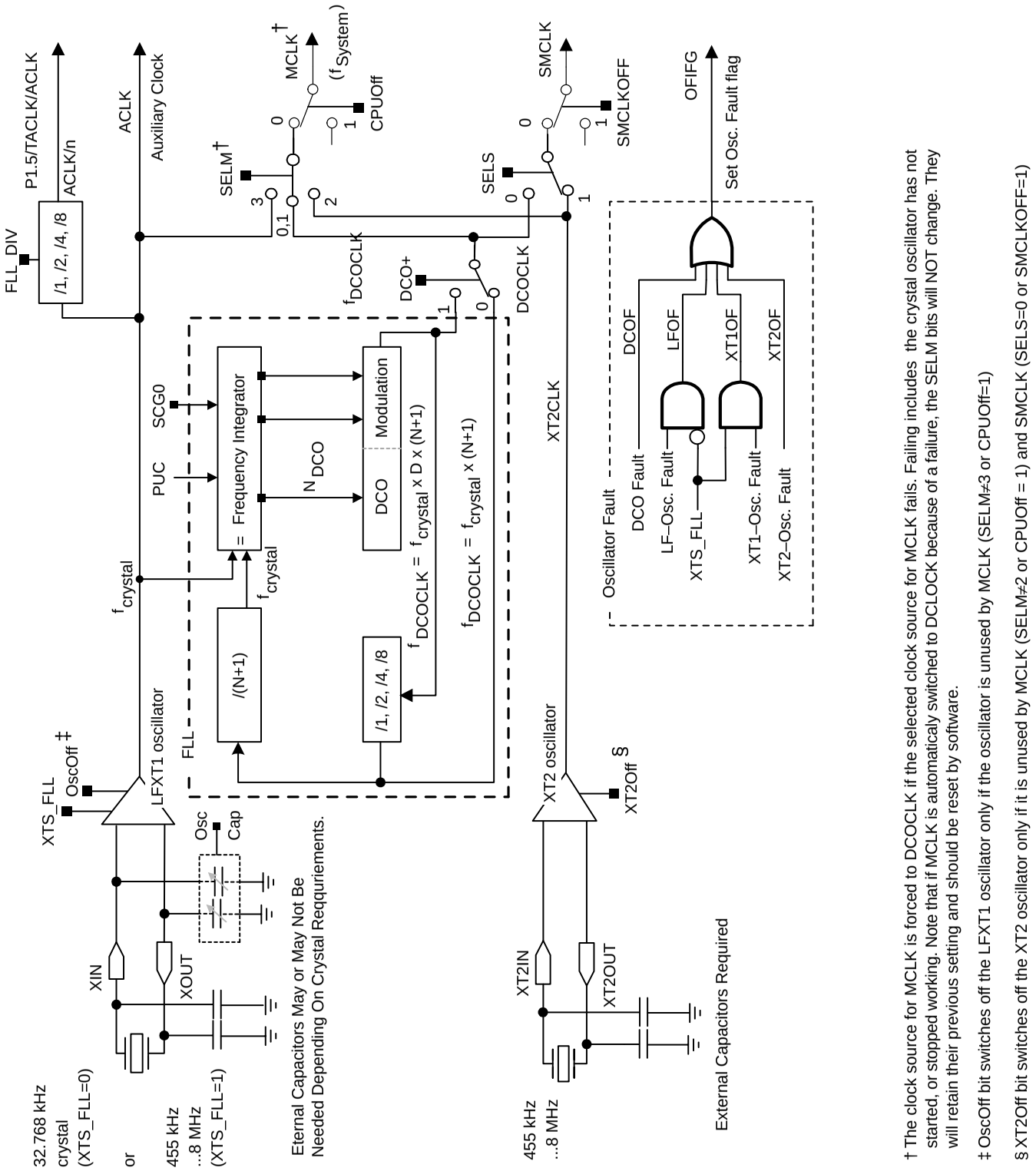
Peripherals, which are connected to the CPU through data, address, and control busses, can be easily handled using all memory-manipulation instructions.

oscillator and system clock

Three clocks are used in the system:

- Main system (master) clock (MCLK), used by the CPU and the system
- Subsystem (master) clock (SMCLK), used by the peripheral modules
- Auxiliary clock (ACLK), originated by LFXT1CLK (crystal frequency) and used by the peripheral modules

oscillator and system clock (continued)



† The clock source for MCLK is forced to DCOCLK if the selected clock source for MCLK fails. Failing includes the crystal oscillator has not started, or stopped working. Note that if MCLK is automaticaly switched to DCLOCK because of a failure, the SELM bits will NOT change. They will retain their previous setting and should be reset by software.

‡ OscOff bit switches off the LFXT1 oscillator only if the oscillator is unused by MCLK (SELM≠3 or CPUOff=1)

§ XT2Off bit switches off the XT2 oscillator only if it is unused by MCLK (SELM≠2 or CPUOff = 1) and SMCLK (SELS=0 or SMCLKOFF=1)

Figure 2. Block Diagram of FLL+ Oscillator and System Clock

oscillator and system clock (continued)

The ACLK is defined by connecting a low-power, low-frequency, or high-frequency crystal to the oscillator, or by applying an external clock source (XTS_FLL must be set). The crystal oscillator may be switched off when the ACLK oscillator is not needed for the present operation mode.

The software selects the DCOCLK frequency. The DCOCLK is active if SCG1 is reset and stopped if SCG1 is set. The dc generator can be stopped when SCG0 and SCG1 are set. The dc generator, which defines the basic DCO frequency, can be adjusted in five steps using control bits FN_2, FN_3, FN_4, and FN_8.

When the target frequency needs modification of the FN_x bits, increasing D or setting DCO+, the following sequence ensures that the maximum system frequency [$f_{(system)}$] is not exceeded:

1. Save FLL lock bit (SCG0 in status register) and set it; loop control goes off.
2. Load modulation control register SCFQCTL with new data (modulation bit M, multiply factor N).
3. Set DCO control bits and MSB's of modulator: SCFI1 = 0Fh to lowest possible frequency.
4. Select DCO+ control bit to be set or reset.
5. Load control register SCFI0 with new data.
6. Restore or set/reset the FLL control bit.

NOTE:

The system clock generator starts with the DCOCLK for MCLK (CPU clock) and program execution starts quickly. The software defines the ACLK clock generation through control bit manipulation.

The MCLK is selected from DCOCLK (SELM {0,1}), XT2CLK (SELM=2), or ACLK (SELM=3). The initial source for MCLK is DCOCLK. The SMCLK selects between two clock sources, the DCOCLK (SELS=0, initial state) and XT2CLK (SELS=1). The XT2CLK is defined by connecting a high-frequency crystal to the oscillator (XT2IN, XT2OUT), or by applying an external clock source to XT2IN. The crystal oscillator may be switched off when the XT2 oscillator is not needed for the present operation mode.

The start conditions for MCLK and SMCLK frequency are identical to the FLL in MSP430x3xx devices, but the correct capacitors at pin XIN and XOUT have to be selected with OscCap bits in register FLL+CTL0 at address 053h.

The ACLK, supplied for external use via port P1.5, may be divided by 1, 2, 4, or 8. This ensures clock signal compatibility to the MSP430x3xx and MSP430x4xx families.

oscillator and system clock (continued)

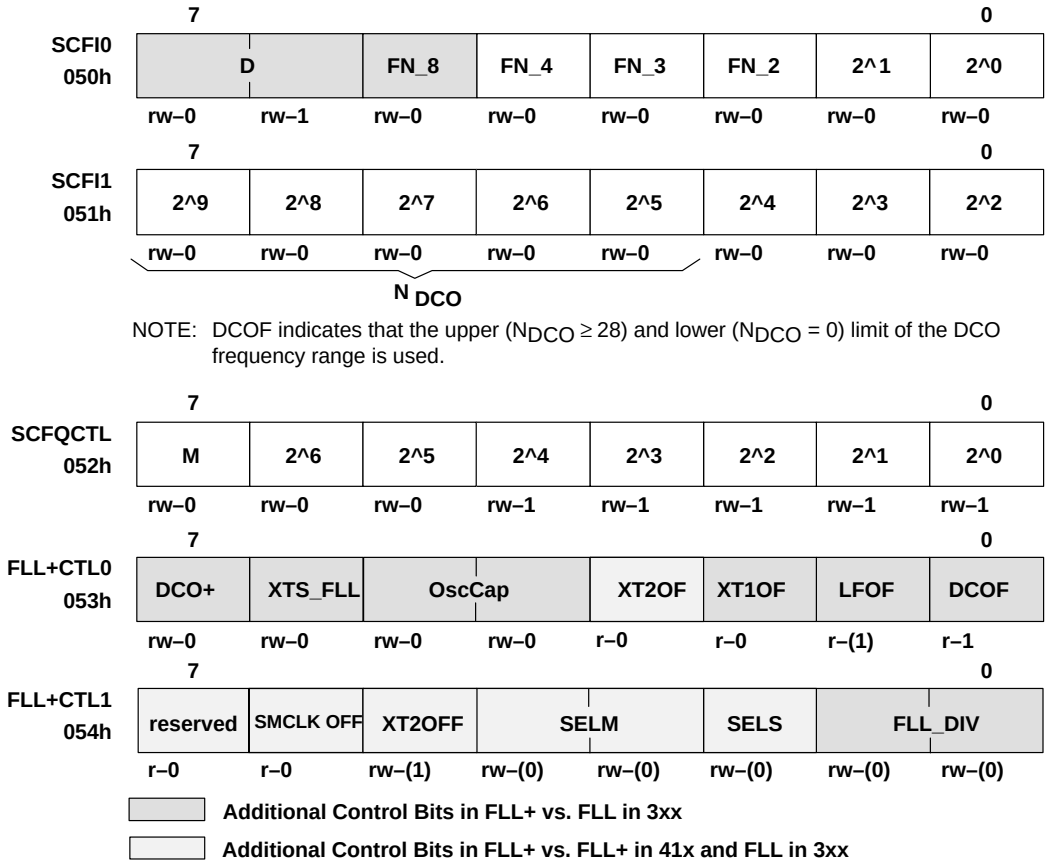


Figure 3. Registers and Control Bits of FLL+ Oscillator and System Clock

Four oscillator-fault bits, DCOF, XT1OF, LFOF, and XT2OF indicate if the DCO, LFXT1 oscillator-HF mode, LFXT1 oscillator-LF mode, and XT2 oscillator respectively, are operating properly. The oscillator fault XT1OF is applicable only if XTS_FLL=1, and LFOF is applicable only if XTS_FLL=0. If one of the four oscillator faults occurs, the OSCFault signal set the OFIFG flag. An NMI service is requested if the interrupt enable bit OFIE is set.

WARNING:

The oscillator fault flag is set if the oscillator is inactive. Inactivity can be caused by system failure such as crystal damage, broken leads, etc., but also if the oscillator is switched on or switched from nonselected to selected.

The clock signals ACLK, MCLK, and SMCLK can be used externally via port pins.

Different application requirements and system conditions dictate different system clock requirements. The FLL+ clock system supports the following conditions:

- High frequency for quick reaction to system hardware requests or events (DCO/FLL+XT1+XT2)
- Low frequency to minimize current consumption, EMI, etc. (LF)
- Stable peripheral clock for timer applications, such as real-time clock (RTC)
- Enabling of start-stop operation with minimum delay (DCO)

brownout, supply voltage supervisor

The brownout circuit detects if a supply voltage is applied to or removed from the VCC terminal and resets the device appropriately.

The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops to a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset). The SVS circuitry is shown in Figure 4. The initial condition for the SVS is off to conserve current consumption. The user's software should enable it when desired.

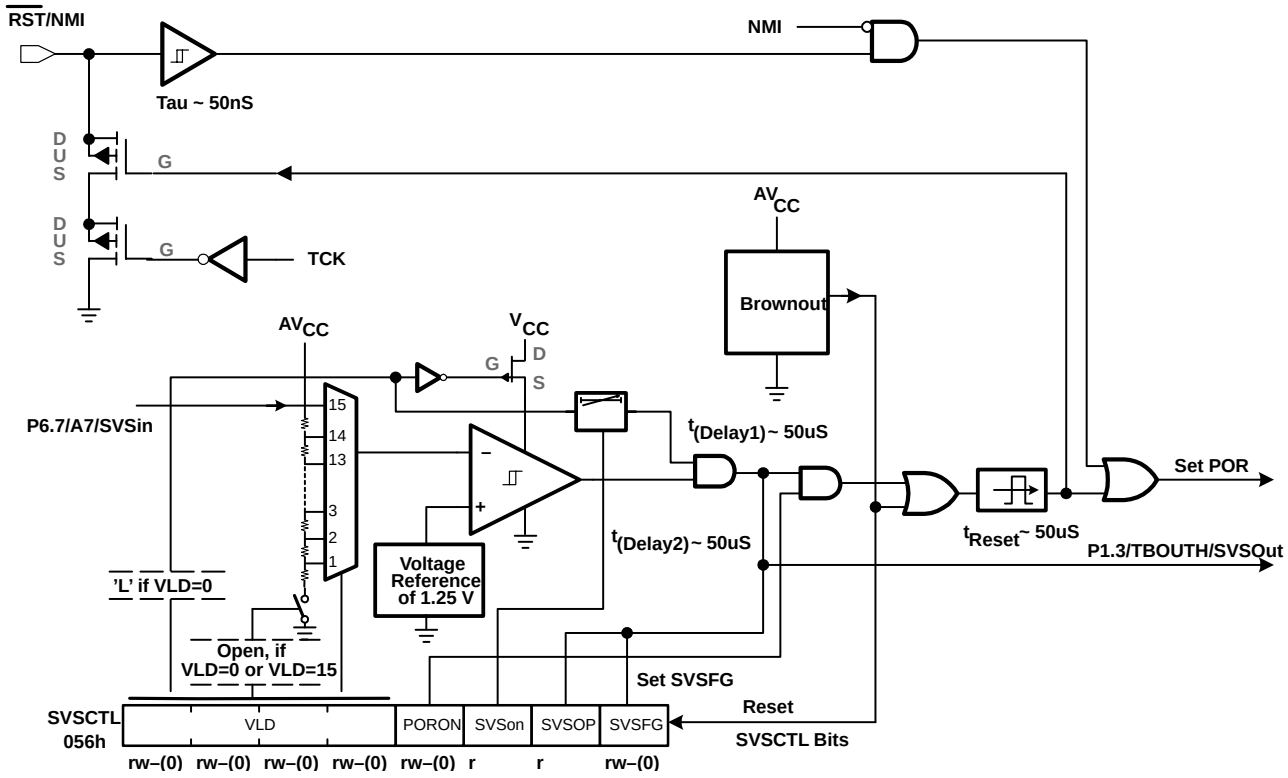


Figure 4. Block Diagram of Brownout and Supply Voltage Supervision

The VLD bits control the on/off state of the SVS circuitry. The SVS is off if VLD=0, and on if VLD=1. Bit PORON enables or disables the automatic reset of the MSP430 upon a low-voltage detection. If PORON=1, a low-voltage detection generates a POR signal and resets the MSP430. Bit SVSOP is used to watch the actual SVS comparator output. Bit SVSFG is set as long as a low-voltage situation is detected and remains set until no low voltage is detected and the software resets it. SVSFG latches such events, whereas SVSOP represents the actual output of the comparator.

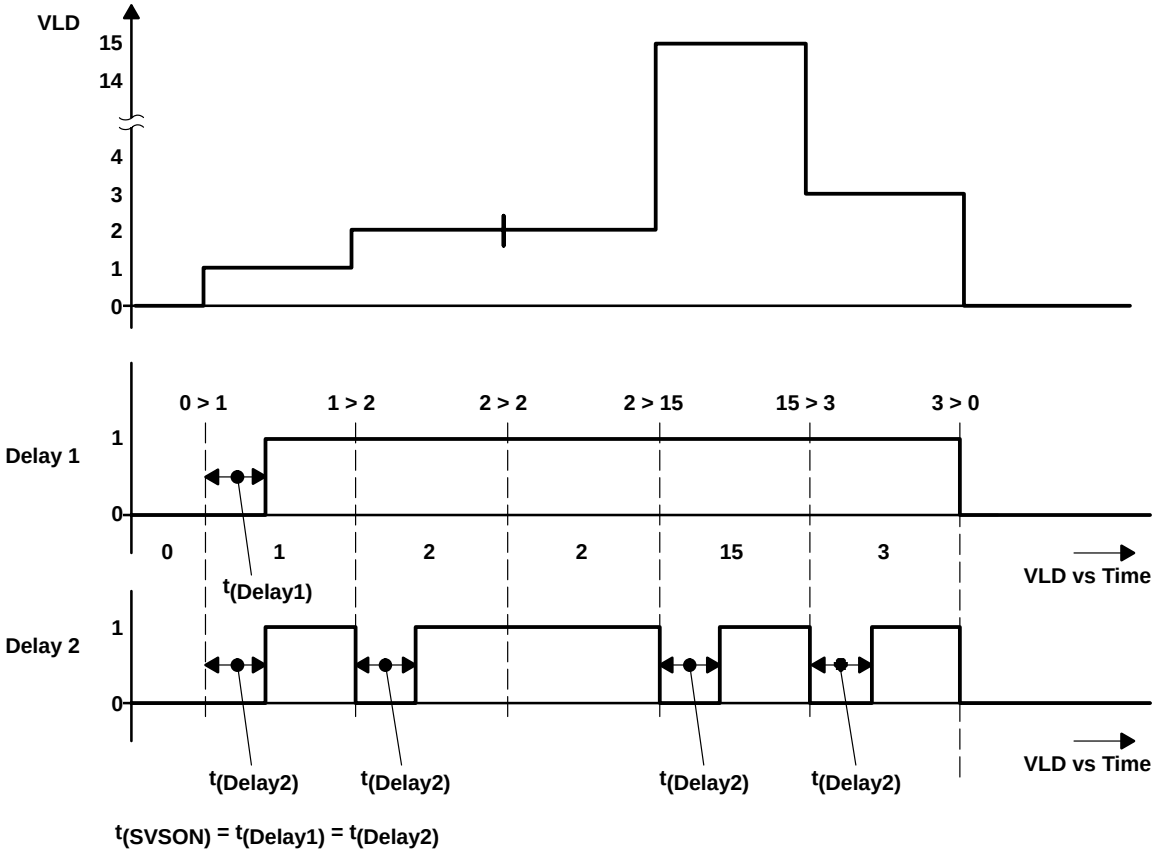
If it is desired to only monitor the supply voltage, but not reset the device if it dips below the determined level, the user simply resets the PORON bit and sets the level normally. This provides the SVM function. The SVM function is useful for example, when performing A/D conversions and the user wants to know if the supply voltage dipped below the minimum operating voltage while the conversion took place.

The SVS circuitry uses hysteresis to reduce sensitivity on voltage drops when the VCC is close to the threshold level. The hystersis for each SVS level is shown in the table below.

The SVS/SVM has some delay as shown below. The Delay1 is used to avoid erroneous SVS/SVM operation if it is enabled (VLD changes from 0 to > 0). SVSon bit is L for $t_{(Delay2)}$ whenever the value of VLD (register SVSCTL) is changed. It is L if VLD = 0.

brownout, supply voltage supervisor (continued)

The SVS level is user programmable as shown in the table below. In addition, any other voltage can be monitored if it is applied to A7.



$t_{(SVSON)} = t_{(Delay1)} = t_{(Delay2)}$

Figure 5. Timing of $t_{(Delay1)}$ and $t_{(Delay2)}$ Triggered by VLD

brownout, supply voltage supervisor (continued)

The levels for monitoring and supervision are defined by the control bits VLD:

VLD				$V_{CC(min)}$ [V]	COMMENT
0	0	0	0	NA	SVS/SVM function is off
0	0	0	1	1.9	SVS/SVM on. Hysteresis is typ 110 mV.
0	0	1	0	2.1	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
0	0	1	1	2.2	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
0	1	0	0	2.3	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
0	1	0	1	2.4	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
0	1	1	0	2.5	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
0	1	1	1	2.65	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	0	0	0	2.8	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	0	0	1	2.9	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	0	1	0	3.05	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	0	1	1	3.2	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	1	0	0	3.35	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	1	0	1	3.5	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	1	1	0	3.7†	SVS/SVM on. Hysteresis is 8 mV to 30 mV.
1	1	1	1	(1.2)	External analog input is used (input comes from the P6.7/A7/SVSin pin) and internally compared with 1.2 V.

† The recommended operation voltage range is limited to 3.6 V.

multiplication

The multiplication operation is supported by a dedicated peripheral module. The module performs 16x16, 16x8, 8x16, and 8x8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6. Ports P1 and P2 use seven control registers, while ports P3, P4, P5, and P6 use only four of the control registers to provide maximum digital input/output flexibility to the application:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Interrupt processing of external events is fully implemented for all eight bits of ports P1 and P2.
- Read/write access to all registers using all instructions is possible.

digital I/O (continued)

The seven control registers are:

- Input register 8 bits at ports P1 through P6
- Output register 8 bits at ports P1 through P6
- Direction register 8 bits at ports P1 through P6
- Interrupt edge select 8 bits at ports P1 and P2
- Interrupt flags 8 bits at ports P1 and P2
- Interrupt enable 8 bits at ports P1 and P2
- Selection (port or module) 8 bits at ports P1 through P6

Each of these registers contains eight bits. Two interrupt vectors are implemented: one commonly used for any interrupt event on ports P1.0 to P1.7, and another commonly used for any interrupt event on ports P2.0 to P2.7.

Ports P3, P4, P5, and P6 have no interrupt capability.

Basic Timer1

The Basic Timer1 (BT1) divides the frequency of SMCLK or ACLK, as selected with the SSEL bit, to provide low-frequency control signals. This is done within the system by one central divider, the Basic Timer1, to support low-current applications. The BTCTL control register contains the flags that control or select the different operational functions. When the supply voltage is applied or when a device is reset (RST/NMI pin), a watchdog overflow or a watchdog security key violation occurs; all bits in the register hold undefined or unchanged status. The user software usually configures the operational conditions on the BT during initialization. The Basic Timer1 has two eight-bit timers which can be cascaded to a sixteen-bit timer. Both timers can be read and written by software. Two bits in the SFR address range handle the system control interaction according to the function implemented in the Basic Timer1. These two bits are the Basic Timer1 interrupt flag (BTIFG) and the Basic Timer1 interrupt enable (BTIE) bit.

LCD drive

The liquid crystal displays (LCDs) for static, 2-MUX, 3-MUX, and 4-MUX operation can be driven directly. The operation of the controller LCD logic is defined by software through memory-bit manipulation. The LCD memory is part of the LCD module, not part of data memory. Eight mode and control bits define the operation and current consumption of the LCD drive. The information for the individual digits can be easily obtained using table programming techniques combined with the proper addressing mode. The segment information is stored into LCD memory using instructions for memory manipulation.

The drive capability is defined by the external resistor divider that supports analog levels for 2-, 3-, and 4-MUX operation. Groups of the digital I/O-LCD segment lines can be selected to have either digital I/O or LCD function. Digital I/Os are selected by default after POR and PUC. The LCD provides four common lines and four terminals for adjusting the analog levels. The configuration for MSP430x44x and MSP430x43x with 100 pins has 40 segment lines and the configuration for MSP430x43x with 80 pins has 32 segment lines.

Table 4. MSP430x43xIPN Terminal Function, Selected by Bits 5/6/7 in LCD Mode Control Register LCDM

TERMINAL		I/O	BITS 5/6/7 IN LCD MODE CONTROL REGISTER LCDM							
NAME	NO		000X XXXX	001X XXXX	010X XXX	011X XXXX	100X XXXX	101X XXXX	110X XXX	111X XXXX
P5.1/S0	12	I/O	P5.1	S0						
P5.0/S1	13	I/O	P5.0	S1						
P4.7/S2	14	I/O	P4.7	S2						
P4.6/S3	15	I/O	P4.6	S3						
P4.5/S4	16	I/O	P4.5	S4						
P4.4/S5	17	I/O	P4.4	S5						
P4.3/S6	18	I/O	P4.3	S6						
P4.2/S7	19	I/O	P4.2	S7						
P4.1/S8	20	I/O	P4.1	S8						
P4.0/S9	21	I/O	P4.0	S9						
S10–S17	22–29	O	S10–S17							
P2.7/ADC10CLK/S18	30	I/O	P2.7/ADC10CLK	P2.7/ADC10CLK	S18					
P2.6/CAOUT/S19	31	I/O	P2.6/CAOUT	P2.6/CAOUT	S19					
S20–S23	32–35	O	S20–S23							
P3.7/S24	36	I/O	P3.7	P3.7	P3.7	P3.7	S24			
P3.6/S25	37	I/O	P3.6	P3.6	P3.6	P3.6	S25			
P3.5/S26	38	I/O	P3.5	P3.5	P3.5	P3.5	S26			
P3.4/S27	39	I/O	P3.4	P3.4	P3.4	P3.4	S27			
P3.3/UCLK0/S28	40	I/O	P3.3/UCLK0	P3.3/UCLK0	P3.3/UCLK0	P3.3/UCLK0	P3.3/UCLK0	S28		
P3.2/SOMI0/S29	41	I/O	P3.2/SOMI0	P3.2/SOMI0	P3.2/SOMI0	P3.2/SOMI0	P3.2/SOMI0	S29		
P3.1/SIMO0/S30	42	I/O	P3.1/SIMO0	P3.1/SIMO0	P3.1/SIMO0	P3.1/SIMO0	P3.1/SIMO0	S30		
P3.0/STE0/S31	43	I/O	P3.0/STE0	P3.0/STE0	P3.0/STE0	P3.0/STE0	P3.0/STE0	S31		

Table 5. MSP430x43xIPZ Terminal Functions, Selected by Bits 5/6/7 in LCD Mode Control Register LCDM

TERMINAL		I/O	BITS 5/6/7 IN LCD MODE CONTROL REGISTER LCDM							
NAME	NO		000X XXXX	001X XXXX	010X XXX	011X XXXX	100X XXXX	101X XXXX	110X XXXX	111X XXXX
P5.1/S0	12	I/O	P5.1	S0						
P5.0/S1	13	I/O	P5.0	S1						
S2–S33	14–45	O	S2–S33							
P4.7/S34	46	I/O	P4.7	P4.7	P4.7	P4.7	P4.7	P4.7	S34	
P4.6/S35	47	I/O	P4.6	P4.6	P4.6	P4.6	P4.6	P4.6	S35	
P4.5/S36	48	I/O	P4.5	P4.5	P4.5	P4.5	P4.5	P4.5	P4.5	S36
P4.4/S36	48	I/O	P4.4	P4.4	P4.4	P4.4	P4.4	P4.4	P4.4	S37
P4.3/S36	48	I/O	P4.3	P4.3	P4.3	P4.3	P4.3	P4.3	P4.3	S38
P4.2/S36	48	I/O	P4.2	P4.2	P4.2	P4.2	P4.2	P4.2	P4.2	S39

Table 6. MSP430x44xIPZ Terminal Functions, Selected by Bits 5/6/7 in LCD Mode Control Register LCDM

TERMINAL		I/O	BITS 5/6/7 IN LCD MODE CONTROL REGISTER LCDM							
NAME	NO		000X XXXX	001X XXXX	010X XXX	011X XXXX	100X XXXX	101X XXXX	110X XXXX	111X XXXX
P5.1/S0	12	I/O	P5.1	S0						
P5.0/S1	13	I/O	P5.0	S1						
S2–S33	14–45	O	S2–S33							
P4.7/S34	46	I/O	P4.7	P4.7	P4.7	P4.7	P4.7	P4.7	S34	
P4.6/S35	47	I/O	P4.6	P4.6	P4.6	P4.6	P4.6	P4.6	S35	
P4.5/UCLK1/S36	48	I/O	P4.5/UCLK1	P4.5UCLK1	P4.5/UCLK1	P4.5/UCLK1	P4.5/UCLK1	P4.5/UCLK1	P4.5/UCLK1	S36
P4.4/SOMI1/S37	49	I/O	P4.4/SOMI1	P4.4/SOMI1	P4.4/SOMI1	P4.4/SOMI1	P4.4/SOMI1	P4.4/SOMI1	P4.4/SOMI1	S37
P4.3/SIMO1/S38	50	I/O	P4.3/SIMO1	P4.3/SIMO1	P4.3/SIMO1	P4.3/SIMO1	P4.3/SIMO1	P4.3/SIMO1	P4.3/SIMO1	S38
P4.2/STE1/S39	51	I/O	P4.2/STE1	P4.2/STE1	P4.2/STE1	P4.2/STE1	P4.2/STE1	P4.2/STE1	P4.2/STE1	S39

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watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software upset has occurred. A system reset is generated if the selected time interval expires. If an application does not require this watchdog function, the module can work as an interval timer, which generates an interrupt after a selected time interval.

The watchdog timer counter (WDTCNT) is a 15/16-bit up-counter not directly accessible by software. The WDTCNT is controlled using the watchdog timer control register (WDTCTL), which is an 8-bit read/write register. Writing to WDTCTL in either operating mode (watchdog or timer) is only possible when using the correct password (05Ah) in the high byte. If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated. The password is read as 069h to minimize accidental write operations to the WDTCTL register. The low byte stores data written to the WDTCTL. In addition to the watchdog timer control bits, there are two bits included in the WDTCTL that configure the NMI pin.

USART0 and USART1

There are two USART peripherals implemented in the MSP430x44x: USART0 and USART1; but only one in the MSP430x43x configuration: USART0. Both have an identical function as described in the applicable chapters of the *MSP430x4xx User's Guide*. They use different pins to communicate, and different registers for module control. Registers with identical functions have different addresses.

The universal synchronous/asynchronous interface is a dedicated peripheral module used in serial communications. The USART supports synchronous SPI (3- or 4-pin), and asynchronous UART communication protocols, using double-buffered transmit and receive channels. Data streams of 7 or 8 bits in length can be transferred at a rate determined by the program, or by an external clock. Low-power applications are optimized by UART mode options which allow for the reception of only the first byte of a complete frame. The application software should then decide if the succeeding data is to be processed. This option reduces power consumption.

Two dedicated interrupt vectors are assigned to each USART module—one for the receive and one for the transmit channels.

timer_A (three capture/compare registers)

The timer module offers one 16-bit counter and three capture/compare registers. The timer clock source can be selected from the external source TACLK (noninverted via SSEL=0 or inverted via SSEL=3), or from two internal sources—ACLK (SSEL=1) or SMCLK (SSEL=2)). The clock source can be divided by one, two, four, or eight. The timer can be fully controlled (in word mode)—it can be halted, read, and written. It can be stopped, run continuously, or made to count up or up/down using one compare block to determine the period. The three capture/compare blocks are configured by the application to run in capture or compare mode.

The capture mode is mostly used to individually measure internal or external events from any combination of positive, negative, or positive and negative edges. It can also be stopped by software. Three different external events (TA0, TA1, and TA2) can be selected. In the capture/compare register CCR2, ACLK is the capture signal if CCI2B is selected. Software capture is chosen if CCISx=2 or CCISx=3.

The compare mode is mostly used to generate timing for the software or application hardware, or to generate pulse-width modulated output signals for various purposes such as D/A conversion functions or motor control. An individual output module is assigned to each of the three capture/compare registers. This module can run independently of the compare function or can be triggered in several ways.

timer_A (three capture/compare registers) (continued)

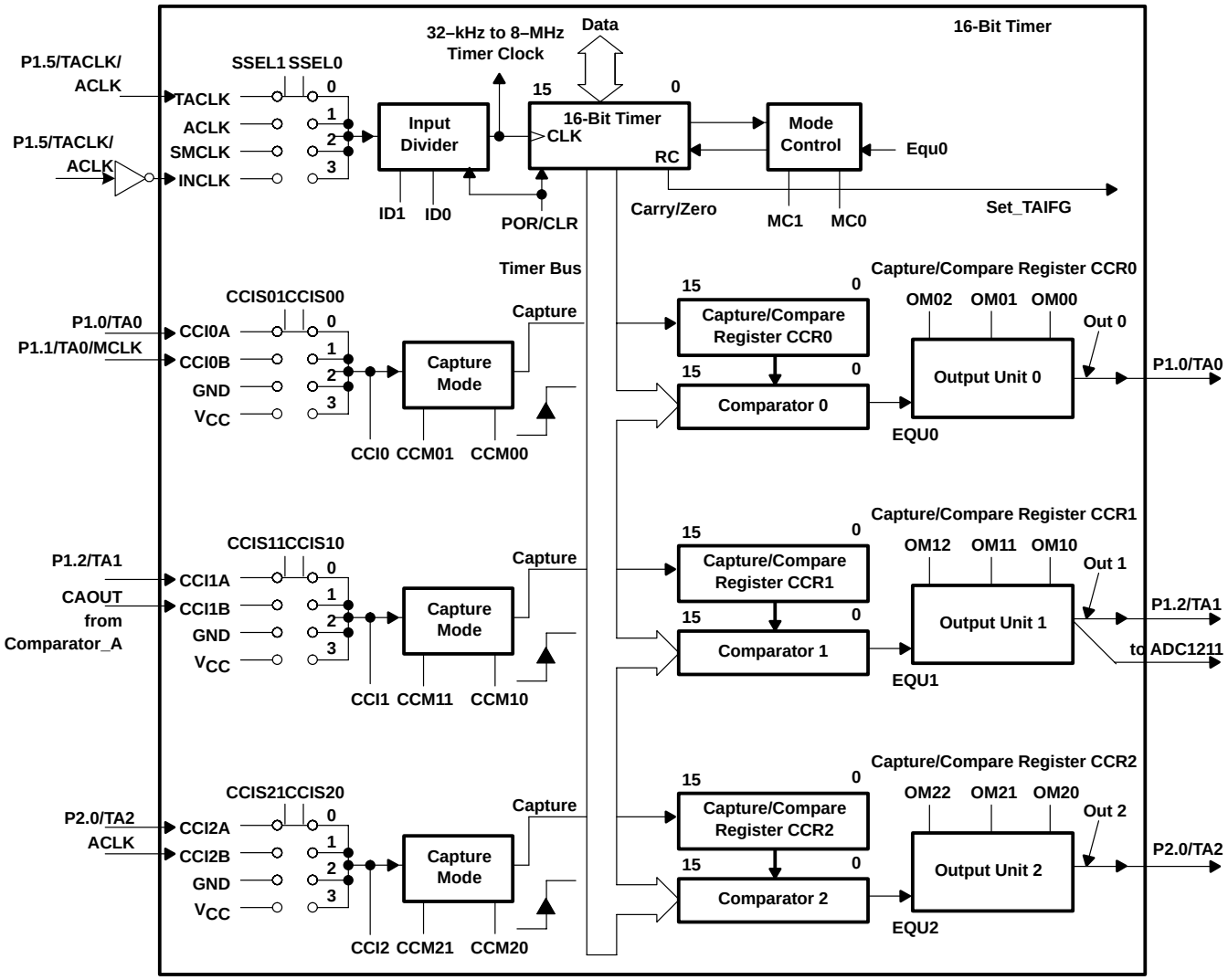


Figure 6. Timer_A Configuration With Three Capture/Compare Registers (CCRs)

The module uses two interrupt vectors. One individual vector is assigned to capture/compare block CCR0 and one common interrupt vector is implemented for the timer and the other two capture/compare blocks. The three interrupt events using the same vector are identified by an individual interrupt vector word. The interrupt vector word is used to add an offset to the program counter to continue the interrupt handler software on the corresponding program location. This simplifies the interrupt handler and gives each interrupt event the same overhead of five cycles in the interrupt handler.

timer_B (7 capture/compare registers in ’x44x and three capture/compare registers in ’x43x)

Timer_B7 is identical to Timer_A3, except for the following:

- The timer counter can be configured to operate in 8-, 10-, 12-, or 16-bit mode.
- The function of the capture/compare registers is slightly different when in compare mode. In Timer_B, the compare data is written to the capture/compare register, but is then transferred to the associated compare latch for the comparison.
- All output level Outx can be set to Hi-Z from the TboutH external signal.
- The SCCI bit is not implemented in Timer_B
- Timer_B7 has seven capture compare registers

The timer module has one 16-bit counter and seven capture/compare registers. The timer clock source can be selected from an external source TBCLK (SSEL=0) or $\overline{\text{TBCLK}}$ (SSEL=3), or from two internal sources: ACLK (SSEL=1) and SMCLK (SSEL=2)). The clock source can be divided by one, two, four, or eight. The timer can be fully controlled (in word mode): it can be halted, read, and written; it can be stopped, run continuously, or made to count up or up/down using one compare block to determine the period. The seven capture/compare blocks are configured by the application to run in capture or in compare mode.

The capture mode is mostly used to measure external or internal events from any combination of positive, negative, or positive and negative edges. It can also be stopped by software. Any of seven different external events TB0 to TB6 can be selected. In the capture/compare register CCR6, ACLK is the capture signal if CCI6B is selected. Software capture is chosen if CCISx=2 or CCISx=3.

The compare mode is mostly used to generate timing for the software or application hardware, or to generate pulse-width modulated output signals for various purposes such as D/A conversion functions or motor control. An individual output module is assigned to each of the seven capture/compare registers. This module can run independently of the compare function, or can be triggered in several ways. The comparison is made from the data in the compare latches (TBCLx) and not from the compare register.

Two interrupt vectors are used by the module. One vector is assigned to capture/compare block CCR0, and one common interrupt vector is implemented for the timer and the other six capture/compare blocks. The seven interrupt events using the same vector are identified by an individual interrupt vector word. The interrupt vector word is used to add an offset to the program counter so that the interrupt handler software continues at the corresponding program location. This simplifies the interrupt handler and assigns each interrupt event the same 5-cycle overhead.

compare latches (TBCLx)

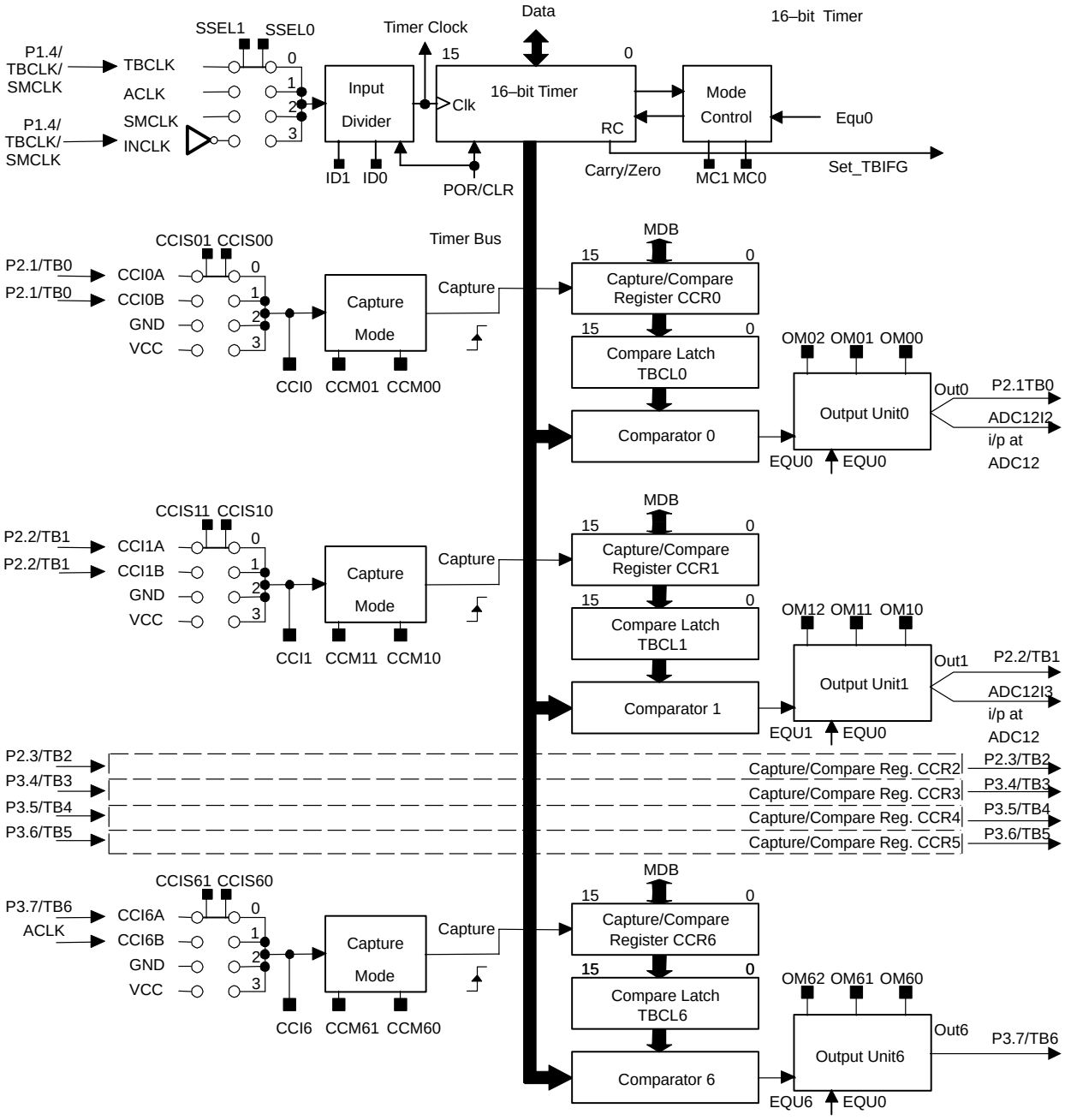
The compare latches can be loaded directly by software or via selected conditions triggered by the PWM function and they are reset by the POR signal.

Load TBCLx immediate, CLLD=0:	Capture/compare register CCRx and the corresponding compare latch are loaded simultaneously.
Load TBCLx at Zero, CLLD=1:	The data in capture/compare register CCRx is loaded to the corresponding compare latch when the 16-bit timer TBR counts to zero.
Load TBCLx at Zero + Period, CLLD=2:	The data in capture/compare register CCRx is loaded to the corresponding compare latch when the 16-bit timer TBR counts to zero or when the next period starts (in UP/DOWN mode).
Load TBCLx at EQUx, CLLD=3:	The data in capture/compare register CCRx is loaded when CCRx is equal to TBR.

Loading the compare latches can be done individually or in groups. Individually means that whenever the selected load condition (see above) is true, the CCRx data is loaded into TBCLx.

Load TBCLx individually, TBCLGRP=0:	Compare latch TBCLx is loaded when the selected load condition (CLLD) is true.
Dual load TBCLx mode, TBCLGRP=1:	Two compare latches TBCLx are loaded when data are written to both CCRx registers of the same group and the load condition (CLLD) is true. Three groups are defined: CCR1+CCR2, CCR3+CCR4, and CCR5+CCR6.
Triple load TBCLx mode, TBCLGRP=2:	Three compare latches TBCLx are loaded when data are written to all CCRx registers of the same group and then the selected load condition (CLLD) is true. Two groups are defined: CCR1+CCR2+CCR3 and CR4+CCR5+CCR6.
Full load TBCLx mode, TBCLGRP=3:	All seven compare latches TBCLx are loaded when data are written to all seven CCRx registers and then the selected load condition (CLLD) is true. All CCRx data, CCR0+CCR1+CCR2+CCR3+CCR4+CCR5+CCR6, are simultaneously loaded to the corresponding SHRx compare latches.

compare latches (TBCLx) (continued)



comparator_A

The primary functions of the comparator module are: support of precision slope conversion in A/D applications, battery voltage supervision, and external analog signal monitoring. The comparator is connected to port pins P1.6/CA0 (+ terminal) and P1.7/CA1 (– terminal). It is controlled by eight control bits in the CACTL register. A block diagram of comparator_A is shown in Figure 7.

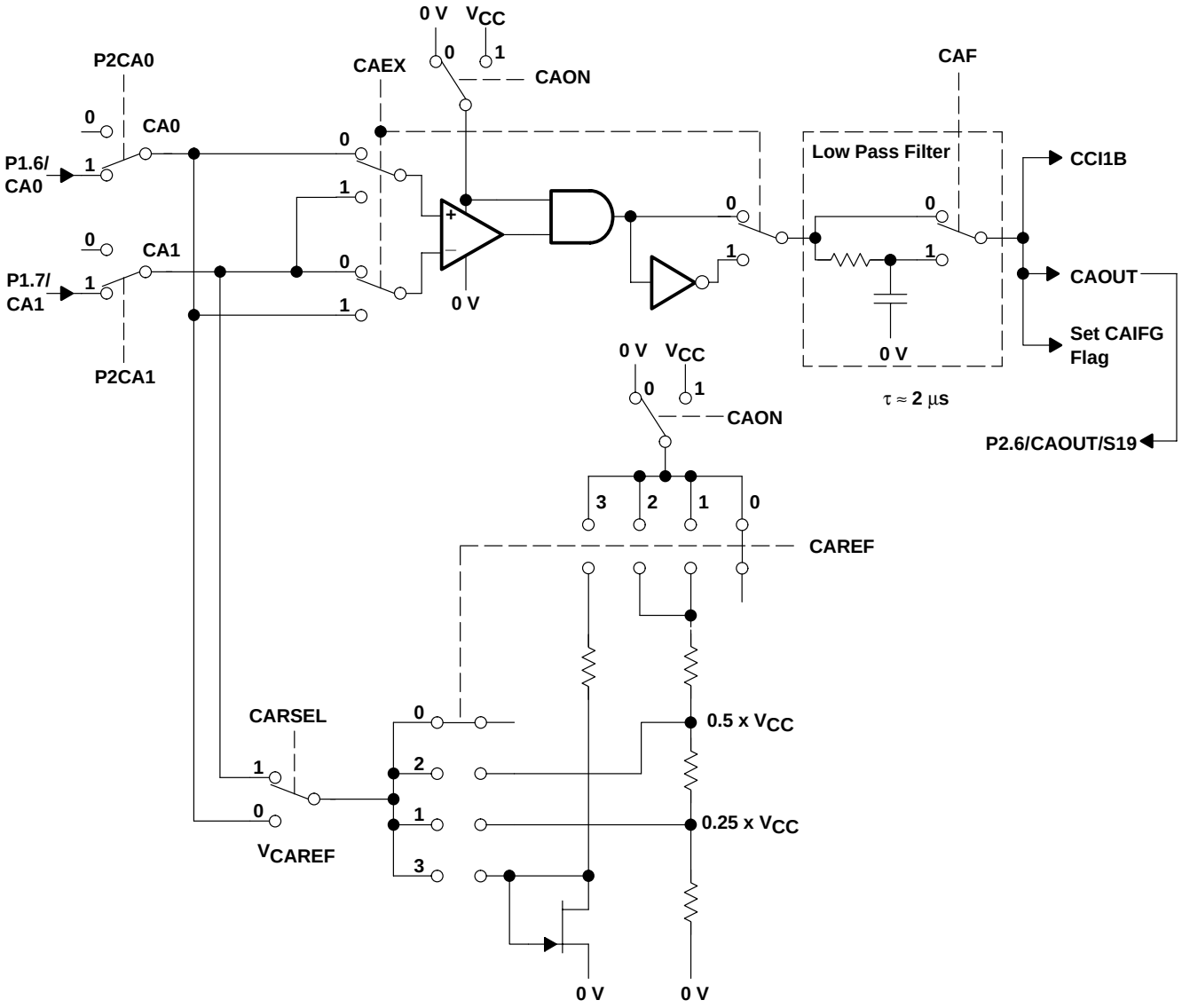


Figure 7. Block Diagram of Comparator_A

The eight control bits are used to connect the comparator to the supply voltage, apply external or internal signals to the + terminal and – terminal, and select the comparator output, including a small filter.

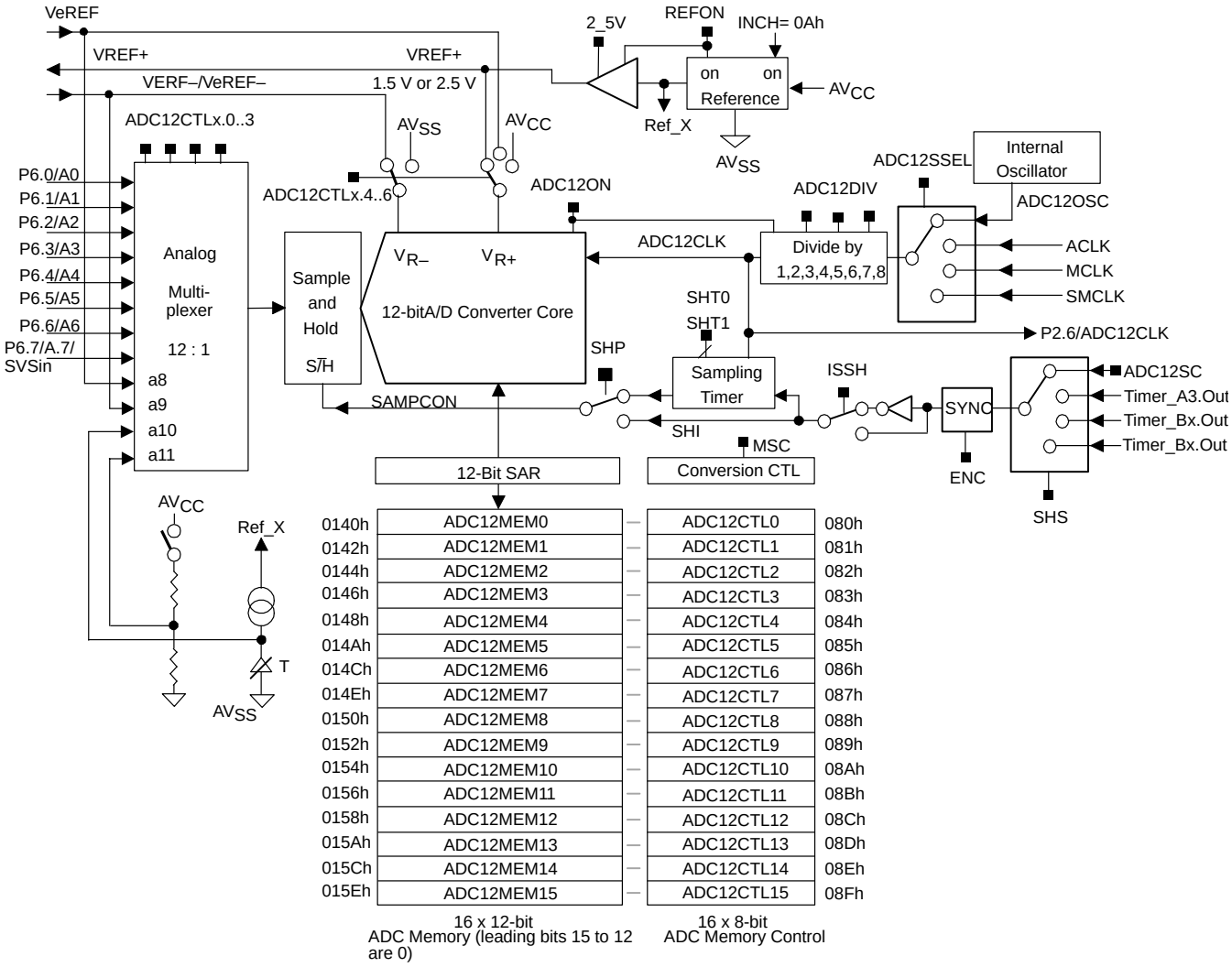
Eight additional bits in register CAPD are implemented into the Comparator_A module and enable the SW to switch off the input buffer of Port P1. A CMOS input buffer dissipates supply current when the input is not near V_{SS} or V_{CC}. Control bits CAPI0 to CAPI7 are initially reset and the port input buffer is active. The port input buffer is inactive if the corresponding control bit is set.

A/D converter

The 12-bit analog-to-digital converter (ADC) uses a 10-bit weighted capacitor array plus a 2-bit resistor string. The CMOS threshold detector in the successive-approximation conversion technique determines each bit by examining the charge on a series of binary-weighted capacitors. The features of the ADC are:

- 12-bit converter with ±1-LSB linearity
- Built-in sample-and-hold
- Eight external and four internal analog channels. The external ADC input terminals are shared with digital port I/O pins.
- Internal reference voltage V_{REF+} of 1.5 V or 2.5 V, software-selectable by control bit 2_5V
- Internal-temperature sensor for temperature measurement:
  - T = [V_SENSOR(T) – V_SENSOR(0°C)] / TC_SENSOR in °C
- Battery-voltage measurement: $N = 0.5 \times (AV_{CC} - AV_{SS}) \times 4096/1.5$ V; $V_{REF}+$ is selected for 1.5 V.
- Source of positive reference voltage level (V_{R+}) can be selected as internal (1.5 V or 2.5 V), external, or AV_{CC}. The source is selected individually for each channel.
- Source of negative reference voltage level (V_{R-}) can be selected as external or AV_{SS}. The source is selected individually for each channel.
- Conversion time can be selected from various clock sources: ACLK, MCLK, SMCLK, or the internal ADC12CLK oscillator. The clock source is divided by an integer from 1 to 8, as selected by software.
- Channel conversion: individual channels, a group of channels, or repeated conversion of a group of channels. If conversion of a group of channels is selected, the sequence, the channels, and the number of channels in the group can be defined by software. For example, a1-a2-a5-a2-a2-….
- The conversion is enabled by the ENC bit, and can be triggered by software via sample and conversion control bit ADC12SC, Timer_A3, or Timer_Bx. Most of the control bits can be modified only if the ENC control bit is low. This prevents unpredictable results caused by unintended modification.
- Sampling time can be $4 \times n0 \times$ ADC12CLK or $4 \times n1 \times$ ADC12CLK. It can be selected to sample as long as the sample signal is high (ISSH=0) or low (ISSH=1). SHT0 defines n0 and SHT1 defines n1.
- The conversion result is stored in one of 16 registers. The 16 registers have individual addresses and can be accessed via software. Each of the 16 registers is linked to an 8-bit register that defines the positive and negative reference source and the channel assigned.

A/D converter (continued)



A/D converter (continued)

Table 7. Reference Voltage Configurations

SREF	VOLTAGE AT V_{R+}	VOLTAGE AT V_{R-}
0	AV_{CC}	AV_{SS}
1	VREF+ (internal)	AV_{SS}
2, 3	VeREF+ (external)	AV_{SS}
4	AV_{CC}	VREF–/VeREF– (internal or external)
5	VREF+ (internal)	VREF–/VeREF– (internal or external)
6, 7	VeREF+ (external)	VREF–/VeREF– (internal or external)

control registers ADC12CTL0 and ADC12CTL1

All control bits are reset during POR. POR is active after V_{CC} or a reset condition is applied to pin RST/NMI. A more detailed description of the control bit functions is found in the ADC12 module description (in the user's guide). Most of the control bits in registers ADC12CTL0, ADC12CTL1, and ADC12MCTLx can only be modified if ENC is low.

The following illustration highlights these bits. Six bits are excluded and can be unrestrictedly modified: ADC12SC, ENC, ADC12TOVIE, ADC12OVIE, and CONSEQ.

The control bits of control registers ADC12CTL0 and ADC12CTL1 are:

ADC12CTL0

01A0h

15								8	7							0
SHT1								SHT0	MSC	2_5 V	REF ON	ADC12 ON	ADC12 OVIE	ADC12 TOVIE	ENC	ADC12 SC
rw–(0)								rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

ADC12SC
01A0h, bit0

Sample and convert. The ADC12SC bit is used to control the conversion by software. It is recommended that ISSH=0.

SHP=1: Changing the ADC12SC bit from 0 to 1 starts the sample and conversion operation. Bit ADC12SC is automatically reset when the conversion is complete (BUSY=0).

SHP=0: A high level of bit ADC12SC determines the sample time. Conversion starts once it is reset (by software). The conversion takes 13 ADC12CLK cycles.

ENC
01A0h, bit1

Enable conversion. A conversion can be started by software (via ADC12SC) or by external signals, only if the enable conversion bit ENC is high. Most of the control bits in ADC12CTL0 and ADC12CTL1, and all the bits in ADCMCTL.x can only be changed if ENC is low.

0: No conversion can be started. This is the initial state.

1: The first sample and conversion starts with the first rising edge of the sampling signal. The operation selected proceeds as long as ENC is set.

control registers ADC12CTL0 and ADC12CTL1 (continued)

ADC12TOVIE
01A0h, bit2

Conversion time overflow interrupt enable.
The timing overflow takes place and a timing overflow vector is generated if another start of sample and conversion is requested while the current conversion or sequence of conversions is still active. The timing overflow enable, if set, may request an interrupt.

ADC12OVIE
01A0h, bit3

Overflow interrupt enables the individual enable for the overflow-interrupt vector.
The overflow takes place if the next conversion result is written into ADC memory ADC12MEMx but the previous result was not read. If an overflow vector is generated, the overflow-interrupt enable flag ADC12OVIE and the general-interrupt enable GIE are set and an interrupt service is requested.

ADC12ON
01A0h, bit4

Switch on the 12-bit ADC core. Make sure that the settling timing constraints are met if ADC core is powered up.

0: Power consumption of the core is off. No conversion is started.

1: ADC core is supplied with power. If no A/D conversion is required, ADC12ON can be reset to conserve power.

REFON
01A0h, bit5

Reference voltage on

0: The internal reference voltage is switched off. No power is consumed by the reference voltage generator.

1: The internal reference voltage is switched on and consumes additional power. The settling time of the reference voltage should be over before the first sample and conversion is started.

2_5V
01A0h, bit6

Reference voltage level

0: The internal-reference voltage is 1.5 V if REFON = 1.

1: The internal-reference voltage is 2.5 V if REFON = 1.

MSC
01A0h, bit7

Multiple sample and conversion. Works only when the sample timer is selected to generate the sample signal and to repeat single channel, sequence of channel, or when repeat sequence of channel (CONSEQ≠0) is selected.

0: Only one sample is taken.

1: If SHP is set and CONSEQ = {1, 2, or 3}, then the rising edge of the sample timer's input signal starts the repeat and/or the sequence of channel mode. Then the second and all further conversions are immediately started after the current conversion is completed.

SHT0
01A0h, bit8–11

Sample-and-hold Time0

SHT1
01A0h, bit12–15

Sample-and-hold Time1

The sample time is a multiple of the ADC12CLK × 4:

$$t_{sample} = 4 \times ADC12CLK \times n$$

SHT0/1	0	1	2	3	4	5	6	7	8	9	10	11	12–15
n	1	2	4	8	16	24	32	48	64	96	128	192	256

The sampling time defined by SHT0 is used when ADC12MEM0 through ADC12MEM7 are used during conversion. The sampling time defined by SHT1 is used when ADC12MEM8 through ADC12MEM15 are used during conversion.

control registers ADC12CTL0 and ADC12CTL1 (continued)

ADC12CTL1

01A2h

15				8	7							0
CSStartAdd				SHS	SHP	ISSH	ADC12DIV			ADC12SSEL	CONSEQ	ADC12 BUSY
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	r–(0)

ADC12BUSY
01A2h, bit0

The BUSY signal indicates an active sample and conversion operation.

0: No conversion is active. The enable conversion bit ENC can be reset normally.

1: A sample period. Conversion or conversion sequence is active.

CONSEQ
01A2h, bit1/2

Select the conversion mode. Repeat mode is on if CONSEQ.1 (bit 1) is set.

0: One single channel is converted
1: One single sequence of channels is converted
2: Repeating conversion of one single channel
3: Repeating conversion of a sequence of channels

ADC12SSEL
01A2h, bit3/4

Selects the clock source for the converter core

0: Internal oscillator embedded in the ADC12 module
1: ACLK
2: MCLK
3: SMCLK

ADC12DIV
01A2h, bit5,6,7

Selects the division rate for the clock source selected by ADC12SSEL. The clock-operation signal ADC12CLK is used in the converter core. The conversion, without sampling time, requires 13 ADC12CLK clocks.

0 to 7: Divide the selected clock source by an integer from 1 to 8.

ISSH
01A2h, bit8

Invert source for the sample signal

0: The source for the sample signal is not inverted.

1: The source for the sample signal is inverted.

SHP
01A2h, bit9

Sample-and-hold pulse, programmable length of sample pulse

0: The sample operation lasts as long as the sample-and-hold signal is 1. The conversion operation starts if the sample-and-hold signal goes from 1 to 0.

1: The sample time (sample signal is high) is defined by $nx4x(1/f_{ADC12CLK})$. SHTx holds the data for n. The conversion starts when the sample signal goes from 1 to 0.

SHS
01A2h, bit10/11

Source for sample-and-hold

0: Control bit ADC12SC triggers sample-and-hold followed by the A/D conversion.

1: The trigger signal for sample-and-hold and conversion comes from Timer_A3.EQU1.

2: The trigger signal for sample-and-hold and conversion comes from Timer_B.EQU0.

3: The trigger signal for sample-and-hold and conversion comes from Timer_B.EQU1.

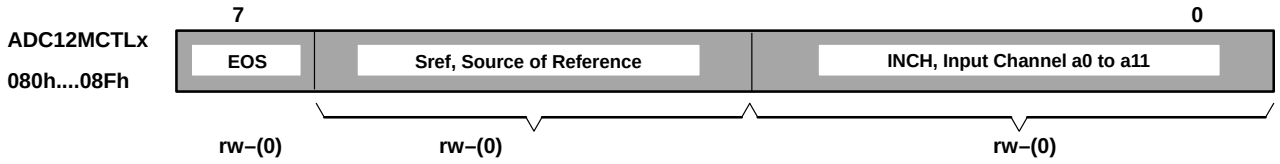
CStartAdd
01A2h, bit12 to bit15

Conversion start address CstartAdd is used to define which ADC12 control memory is used to start a (first) conversion. The value of CstartAdd ranges from 0 to 0Fh, corresponding to ADC12MEM0 to ADC12MEM15 and the associated control registers ADC12MCTL0 to ADC12MCTL15.

control register ADC12MCTLx and conversion memory ADC12MEMx

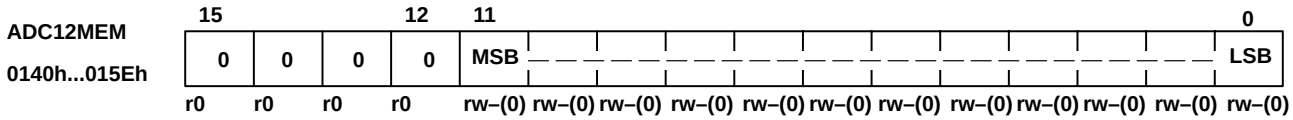
All control bits are reset during POR. POR is active after application of V_{CC}, or after a reset condition is applied to pin RST/NMI. Control registers ADC12MCTL.x can be modified only if enable conversion control bit ENC is reset. Any instruction that writes to an ADC12MCTLx register while the ENC bit is reset has no effect. A more detailed description of the control bit functions is found in the ADC12 module description (in the *MSP430x3xx User's Guide*).

There are 16 ADC12MCTLx 8-bit memory control registers and 16 ADC12MEMx 16-bit registers. Each of the memory control registers is associated with one ADC12MEMx register; for example, ADC12MEM0 is associated with ADC12MCTL0, ADC12MEM1 is associated with ADC12MCTL1, etc.



The control register bits are used to select the analog channel, the reference voltage sources for V_{R+} and V_{R-}, and a control signal which marks the last channel in a group of channels. The sixteen 16-bit registers ADC12MEMx are used to hold the conversion results.

The following illustration shows the conversion-result registers ADC12MEM0 to ADC12MEM15:



ADC12MEM0 to ADC12MEM15	0140h, bit0, 015Eh, bit15	The 12 bits of the conversion result are stored in 16 control registers ADC12MEM0 to ADC12MEM15. The 12 bits are right-justified and the upper four bits are always read as 0.

ADC12 interrupt flags ADC12IFG.x and enable registers ADC12IEN.x

There are 16 ADC12IFG.x interrupt flags, 16 ADC12IE.x interrupt-enable bits, and one interrupt-vector word. The 16 interrupt flags and enable bits are associated with the 16 ADC12MEMx registers. For example, register ADC12MEM0, interrupt flag ADC12IFG.0, and interrupt-enable bit ADC12IE.0 form one conversion-result block.

ADC12IFG.0 has the highest priority and ADC12IFG.15 has the lowest priority.

All interrupt flags and interrupt-enable bits are reset during POR. POR is active after application of V_{CC} or after a reset condition is applied to the RST/NMI pin.

ADC12 interrupt vector register

The 12-bit ADC has one interrupt vector for the overflow flag, the timing overflow flag, and 16 interrupt flags. This vector indicates that a conversion result is stored into registers ADC12MEMx. Handling of the 18 flags is assisted by the interrupt-vector word. The 16-bit vector word ADC12IV indicates the highest pending interrupt. The interrupt-vector word is used to add an offset to the program counter so that the interrupt-handler software continues at the corresponding program location according to the interrupt event. This simplifies the interrupt-handler operation and assigns each interrupt event the same 5-cycle overhead.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog Timer control	WDTCTL	0120h
Timer_B7 Timer_B3 (see Note 6)	Capture/compare register 6	CCR6	019Eh
	Capture/compare register 5	CCR5	019Ch
	Capture/compare register 4	CCR4	019Ah
	Capture/compare register 3	CCR3	0198h
	Capture/compare register 2	CCR2	0196h
	Capture/compare register 1	CCR1	0194h
	Capture/compare register 0	CCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 6	CCTL6	018Eh
	Capture/compare control 5	CCTL5	018Ch
	Capture/compare control 4	CCTL4	018Ah
	Capture/compare control 3	CCTL3	0188h
	Capture/compare control 2	CCTL2	0186h
	Capture/compare control 1	CCTL1	0184h
	Capture/compare control 0	CCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Reserved		017Eh
	Reserved		017Ch
	Reserved		017Ah
	Reserved		0178h
	Capture/compare register 2	CCR2	0176h
	Capture/compare register 1	CCR1	0174h
	Capture/compare register 0	CCR0	0172h
	Timer_A register	TAR	0170h
	Reserved		016Eh
	Reserved		016Ch
	Reserved		016Ah
	Reserved		0168h
	Capture/compare control 2	CCTL2	0166h
	Capture/compare control 1	CCTL1	0164h
	Capture/compare control 0	CCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Multiply In MSP430x44x only	Sum extend	SumExt	013Eh
	Result high word	ResHi	013Ch
	Result low word	ResLo	013Ah
	Second operand	OP_2	0138h
	Multiply signed + accumulate/operand1	MACS	0136h
	Multiply + accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
	Multiply unsigned/operand1	MPY	0130h

NOTE 6: Timer_B7 in the MSP430x44x family has seven CCRs; Timer_B3 in the MSP430x43x family has three CCRs.

peripheral file map (continued)

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
ADC12 See also *Peripherals with Byte Access*	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
ADC12 (Memory control registers require byte access)	ADC memory-control register15	ADC12MCTL15	08Fh
	ADC memory-control register14	ADC12MCTL14	08Eh
	ADC memory-control register13	ADC12MCTL13	08Dh
	ADC memory-control register12	ADC12MCTL12	08Ch
	ADC memory-control register11	ADC12MCTL11	08Bh
	ADC memory-control register10	ADC12MCTL10	08Ah
	ADC memory-control register9	ADC12MCTL9	089h
	ADC memory-control register8	ADC12MCTL8	088h
	ADC memory-control register7	ADC12MCTL7	087h
	ADC memory-control register6	ADC12MCTL6	086h
	ADC memory-control register5	ADC12MCTL5	085h
	ADC memory-control register4	ADC12MCTL4	084h
	ADC memory-control register3	ADC12MCTL3	083h
	ADC memory-control register2	ADC12MCTL2	082h
	ADC memory-control register1	ADC12MCTL1	081h
	ADC memory-control register0	ADC12MCTL0	080h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
LCD	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDCTL	090h
UART1 (Only in ‘x44x)	Transmit buffer	UTXBUF1	07Fh
	Receive buffer	URXBUF1	07Eh
	Baud rate	UBR11	07Dh
	Baud rate	UBR01	07Ch
	Modulation control	UMCTL1	07Bh
	Receive control	URCTL1	07Ah
	Transmit control	UTCTL1	079h
	UART control	UCTL1	078h
UART0	Transmit buffer	UTXBUF0	077h
	Receive buffer	URXBUF0	076h
	Baud rate	UBR10	075h
	Baud rate	UBR00	074h
	Modulation control	UMCTL0	073h
	Receive control	URCTL0	072h
	Transmit control	UTCTL0	071h
	UART control	UCTL0	070h
Comparator_A	Comp._A port disable	CAPD	05Bh
	Comp._A control2	CACTL2	05Ah
	Comp._A control1	CACTL1	059h
BrownOUT, SVS	SVS control register (Reset by brownout signal)	SVSCTL	056h
System clock FLL+	FLL+ Control1	FLL+CTL1	054h
	FLL+ Control0	FLL+CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
Basic Timer1	BT counter2	BTCNT2	047h
	BT counter1	BTCNT1	046h
	BT control	BTCTL	040h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special functions	SFR module enable2	ME2	005h
	SFR module enable1	ME1	004h
	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to 4.1 V
Voltage applied to any pin (referenced to V_{SS}) . . . . . –0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg}: (unprogrammed device) . . . . . –55°C to 150°C
(programmed device) . . . . . –40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (AV_{CC} = DV_{CC2} = V_{CC})		MSP430F43x, MSP430F44x	1.8		3.6	V
Supply voltage during flash memory programming, V_{CC} (AV_{CC} = DV_{CC2} = V_{CC})		MSP430F43x, MSP430F44x	2.7		3.6	V
Supply voltage during program execution, SVS enabled (see Note 1), V_{CC} (V_{CC} = DV_{CC} = V_{CC})		MSP430F43x, MSP430F44x	2		3.6	V
Supply voltage, V_{SS}			0		0	V
Operating free-air temperature range, T_A		MSP430x43x MSP430x44x	–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 2)	LF selected, XTS_FLL=0	Watch crystal		32.768		kHz
	XT1 selected, XTS_FLL=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS_FLL=1	Crystal	1000		8000	kHz
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	
Flash-timing-generator frequency, $f_{(FTG)}$		MSP430F43x, MSP430F44x	257		476	kHz
Cumulative program time, $t_{(CPT)}$ (see Note 3)		V_{CC} = 2.7 V/3.6 V MSP430F43x MSP430F44x			3	ms
Mass erase time, t(MEras) (See also the *flash memory, timing generator, control register FCTL2* section, see Note 4)		V_{CC} = 2.7 V/3.6 V	200			ms
Low-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IL} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	V_{SS}		V_{SS} + 0.6	V
High-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IH} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	$0.8 \times V_{CC}$		V_{CC}	V
Input levels at Xin and Xout	$V_{IL(Xin, Xout)}$	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{SS}$	V
	$V_{IH(Xin, Xout)}$		$0.8 \times V_{CC}$		V_{CC}	

NOTES: 1. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the supply voltage is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.
2. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.
3. The cumulative program time must not be exceeded during a segment-write operation. This parameter is only relevant if segment write option is used.
4. The mass erase duration generated by the flash timing generator is at least 11.1 ms. The cumulative mass erase time needed is 200 ms. This can be achieved by repeating the mass erase operation until the cumulative mass erase time is met (a minimum of 19 cycles may be required).

typical characteristics

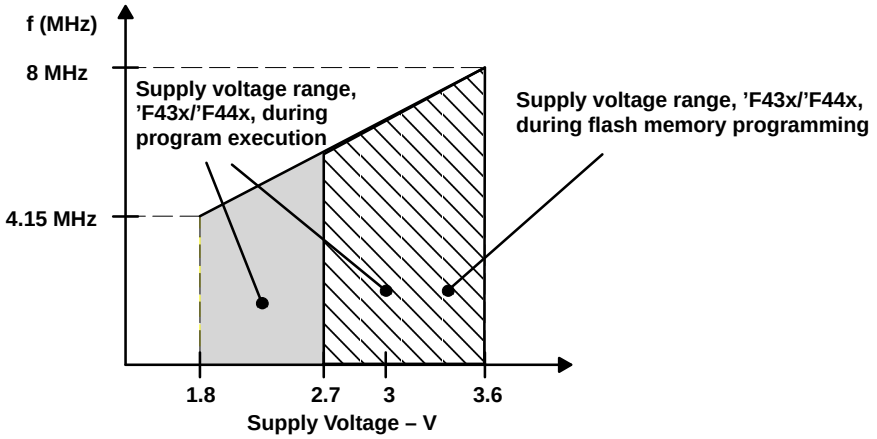


Figure 8. Frequency vs Supply Voltage, MSP430F43x or MSP430F44x

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current, $f_{(System)}$ = 1 MHz

PARAMETER			TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1)	F43x, F44x	T_A = –40°C to 85°C	V_{CC} = 2.2 V		280	350	µA
				V_{CC} = 3 V		420	560	
$I_{(LPM0)}$	Low-power mode, (LPM0) (see Note 1)	F43x, F44x	T_A = –40°C to 85°C	V_{CC} = 2.2 V		32	45	µA
				V_{CC} = 3 V		55	70	
$I_{(LPM2)}$	Low-power mode, (LPM2), f(MCLK) = f (SMCLK) = 0 MHz, f(ACLK) = 32.768 Hz, SCG0 = 0 (see Note 2)		T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
				V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 (see Note 3)		T_A = –40°C	V_{CC} = 2.2 V		1	1.5	µA
			T_A = 25°C			1.1	1.5	
			T_A = 60°C			2	3	
			T_A = 85°C			3.5	6	
			T_A = –40°C	V_{CC} = 3 V		1.8	2.2	µA
			T_A = 25°C			1.6	1.9	
			T_A = 60°C			2.5	3.5	
			T_A = 85°C			4.2	7.5	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1 (see Note 2)		T_A = –40°C	V_{CC} = 2.2 V		0.1	0.5	µA
			T_A = 25°C			0.1	0.5	
			T_A = 60°C			0.7	1.1	
			T_A = 85°C			1.7	3	
			T_A = –40°C	V_{CC} = 3 V		0.1	0.5	µA
			T_A = 25°C			0.1	0.5	
			T_A = 60°C			0.8	1.2	
			T_A = 85°C			1.9	3.5	

NOTES: 1. Timer_B is clocked by $f_{(DCOCLK)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
3. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The current consumption in LPM3 is measured with active Basic Timer1 and LCD (ACLK selected). The current consumption of the Comparator_A and the SVS module are specified in the respective sections. The LPM3 currents are characterized with a KDS Daishinku DT–38 (6 pF) crystal and OscCap=1.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Current consumption of active mode versus system frequency, F-version:

$I_{(AM)} = I_{(AM)}\ [1\ MHz] \times f_{(System)}\ [MHz]$

Current consumption of active mode versus supply voltage, F-version:

$I_{(AM)} = I_{(AM)\ [3\ V]} + 175\ \mu A/V \times (V_{CC} - 3\ V)$

SCHMITT-trigger inputs – ports P1, P2, P3, P4, P5, and P6; $\overline{RST}$/NMI; JTAG: TCK, TMS, TDI, TDO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.9	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

outputs – ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}–0.25		V_{CC}	V
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}–0.6		V_{CC}	
		$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}–0.25		V_{CC}	
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

typical characteristics

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

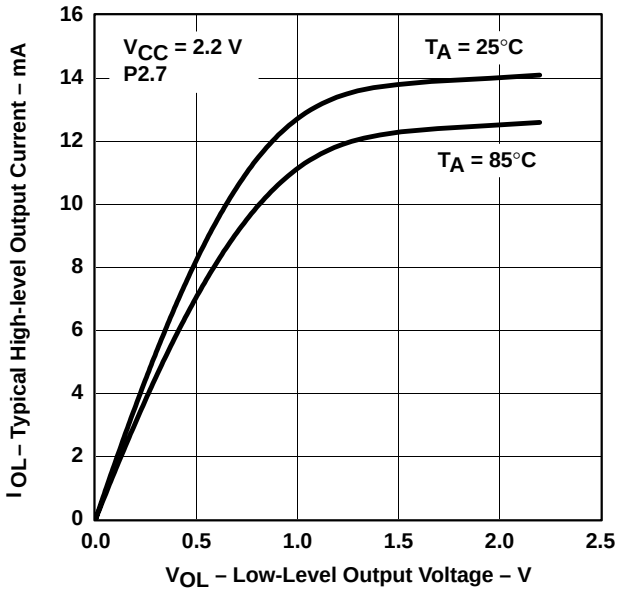


Figure 9

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

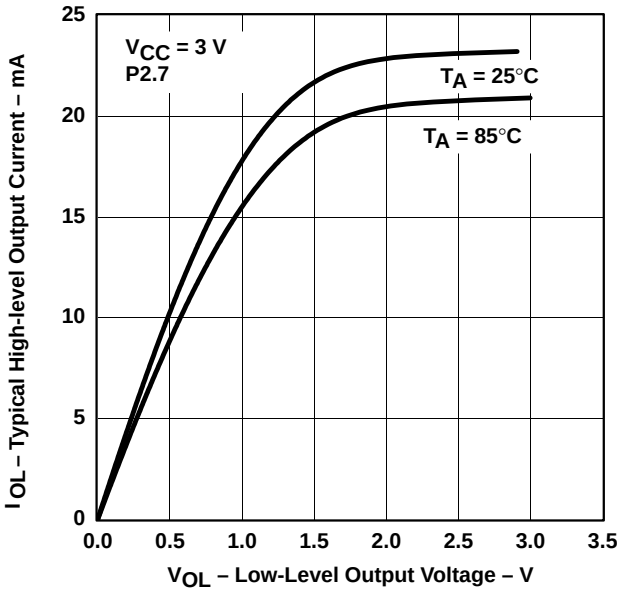


Figure 10

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

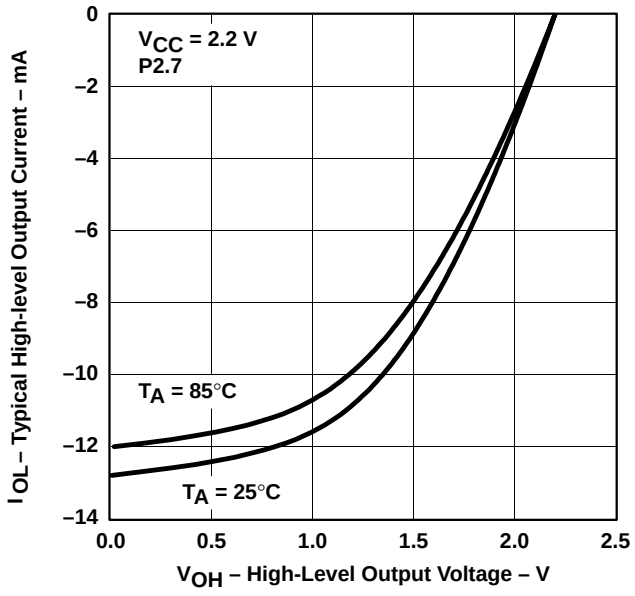


Figure 11

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

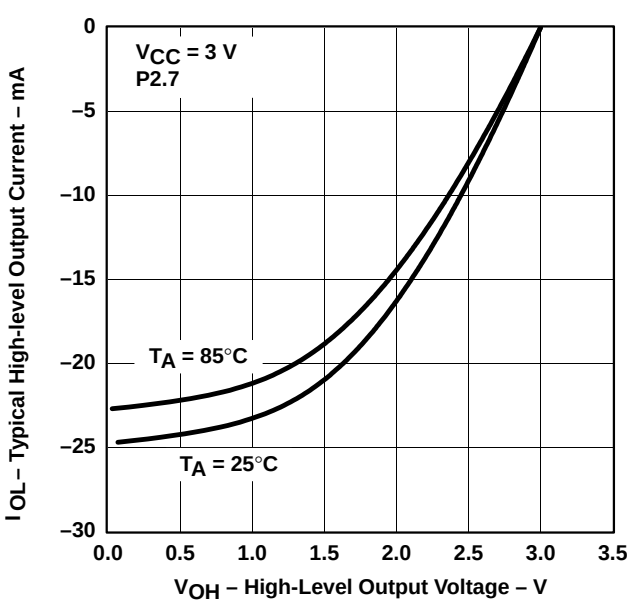


Figure 12

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

input frequency – ports P1, P2, P3, P4, P5, and P6

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(IN)}$	$t_{(h)} = t_{(L)}$	V_{CC} = 2.2 V			8	MHz
		V_{CC} = 3 V			10	

capture timing _ Timer_A3: TA0, TA1, TA2; Timer_B7: TB0 to TB6

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(int)}$	Ports P2, P4: External trigger signal for the interrupt flag (see Note 1 and Note 2)	V_{CC} = 2.2 V/3 V	1.5			Cycle
		V_{CC} = 2.2 V	62			ns
		V_{CC} = 3 V	50			

NOTES: 1. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently of this timing constraint. $t_{(int)}$ is defined in MCLK cycles.
2. The external signal needs additional timing because of the maximum input-frequency constraint.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	$(1 \le x \le 6,\ 0 \le y \le 7)$	C_L = 20 pF, I_L = ±1.5mA	V_{CC} = 2.2 V	DC		5	MHz
			V_{CC} = 3 V	DC		7.5	
$f_{(ACLK)}$ $f_{(MCLK)}$ $f_{(SMCLK)}$	P1.1/TA0/MCLK, P1.5/TACLK/ ACLK P1.4/TBCLK/SMCLK	C_L = 20 pF				$f_{(System)}$	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.5/TACLK/ACLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(ACLK)} = f_{(LFXT1)} = f_{(XT1)}$	40%		60%	
			$f_{(ACLK)} = f_{(LFXT1)} = f_{(LF)}$	30%		70%	
			$f_{(ACLK)} = f_{(LFXT1)}$		50%		
		P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50%– 15 ns	50%	50%+ 15 ns	
		P1.4/TBCLK/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(SMCLK)} = f_{(XT2)}$	40%		60%	
			$f_{(SMCLK)} = f_{(DCOCLK)}$	50%– 15 ns	50%	50%+ 15 ns	

external interrupt timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(int)}$	Ports P1, P2: External trigger signal for the interrupt flag (see Note 3 and Note 4)	V_{CC} = 2.2 V/3 V	1.5			Cycle
		V_{CC} = 2.2 V	62			ns
		V_{CC} = 3 V	50			

NOTES: 3. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently of this timing constraint. $t_{(int)}$ is defined in MCLK cycles.
4. The external signal needs additional timing because of the maximum input-frequency constraint.

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V			6	µs
		f = 2 MHz				6	
		f = 3 MHz				6	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

leakage current (see Notes 1 and 2)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current	Port P1	Port 1: $V_{(P1.x)}$	V_{CC} = 2.2 V/3 V			±50	nA
$I_{lkg(P6.x)}$		Port P6	Port 6: $V_{(P6.x)}$				±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input and there must be no optional pullup or pulldown resistor.

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU halted (see Note 3)	1.6			V

NOTE 3: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

LCD

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(33)}$	Analog voltage	Voltage at P5.7/R33	V_{CC} = 3 V	2.5		V_{CC} + 0.2	V
$V_{(23)}$		Voltage at P5.6/R23			$[V_{(33)}–V_{(03)}] \times 2/3 + V_{(03)}$		
$V_{(13)}$		Voltage at P5.5/R13			$[V_{(33)}–V_{(03)}] \times 1/3 + V_{(03)}$		
$V_{(33)} – V_{(03)}$		Voltage at R33 to R03		2.5		V_{CC} + 0.2	
$I_{(R03)}$	Input leakage	R03 = V_{SS}	No load at all segment and common lines, V_{CC} = 3 V			±20	nA
$I_{(R13)}$		P5.5/R13 = $V_{CC}/3$				±20	
$I_{(R23)}$		P5.6/R23 = $2 \times V_{CC}/3$				±20	
$V_{(Sxx0)}$	Segment line voltage	$I_{(Sxx)}$ = –3 µA,	V_{CC} = 3 V	$V_{(03)}$		$V_{(03)}$ – 0.1	V
$V_{(Sxx1)}$				$V_{(13)}$		$V_{(13)}$ – 0.1	
$V_{(Sxx2)}$				$V_{(23)}$		$V_{(23)}$ – 0.1	
$V_{(Sxx3)}$				$V_{(33)}$		$V_{(33)}$ + 0.1	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		25	40	µA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=0, CARSEL=0, CAREF=1/2/3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(Ref025)}$	Voltage @ 0.25 V_{CC} node / V_{CC}	PCA0=1, CARSEL=1, CAREF=1, No load at P2.3/CA0 and P2.4/CA1	V_{CC} = 2.2 V / 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	Voltage @ 0.5 V_{CC} node / V_{CC}	PCA0=1, CARSEL=1, CAREF=2, No load at P2.3/CA0 and P2.4/CA1	V_{CC} = 2.2V / 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$		PCA0=1, CARSEL=1, CAREF=3, No load at P2.3/CA0 and P2.4/CA1; T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
V_{IC}	Common-mode input voltage range	CAON=1	V_{CC} = 2.2 V / 3 V	0		V_{CC}–1	V
V_p–V_S	Offset voltage	See Note 2	VCC = 2.2 V / 3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	V_{CC} = 2.2 V / 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	160	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

typical characteristics

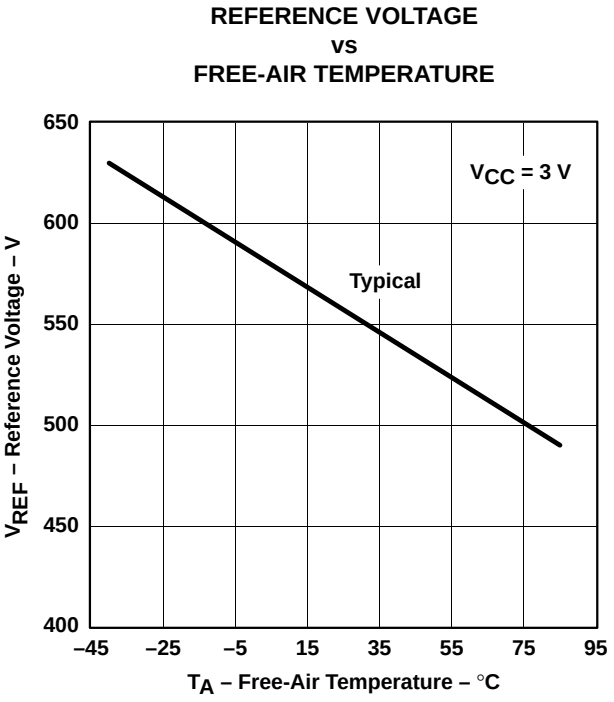


Figure 13. $V_{(RefVT)}$ vs Temperature

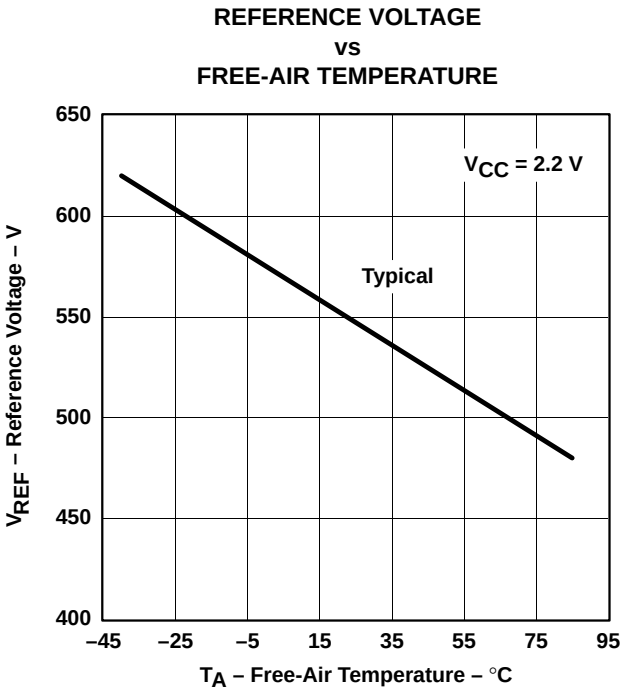


Figure 14. $V_{(RefVT)}$ vs Temperature

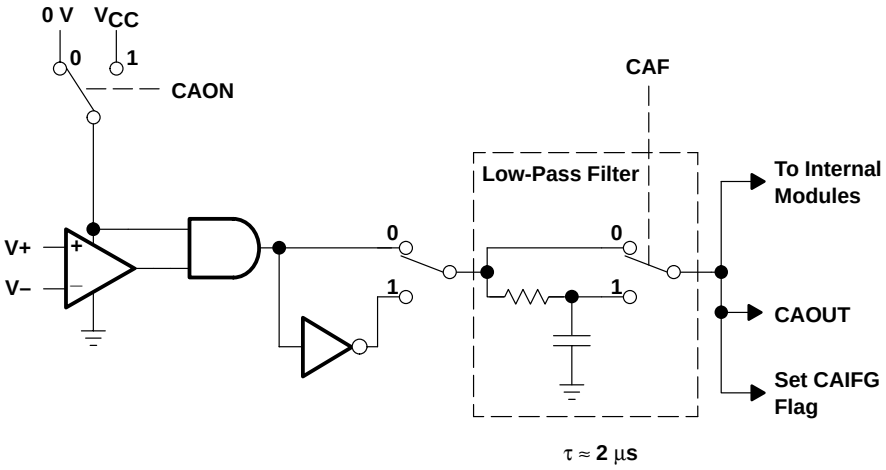


Figure 15. Block Diagram of Comparator_A Module

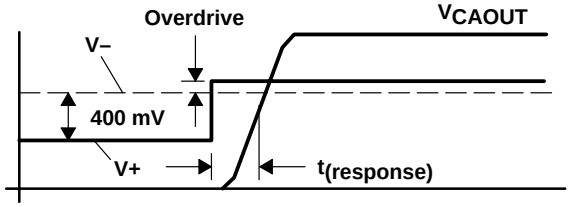


Figure 16. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

POR/brownout reset (BOR) (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout	$dV_{CC}/dt \geq 30$ V/ms (see Note 2)	5		150	µs
		$dV_{CC}/dt \leq 30$ V/ms (see Note 2)			2000	
$V_{CC(start)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 17)	$0.7 \times V_{(B\_IT-)}$			V
$V_{(B\_IT-)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 17 through Figure 19)	0.9	1.35	1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 17)	70	130	180	mV
$t_{(reset)}$		Pulse length needed at RST/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.
2. This parameter is not production tested, assured by design.

typical characteristics

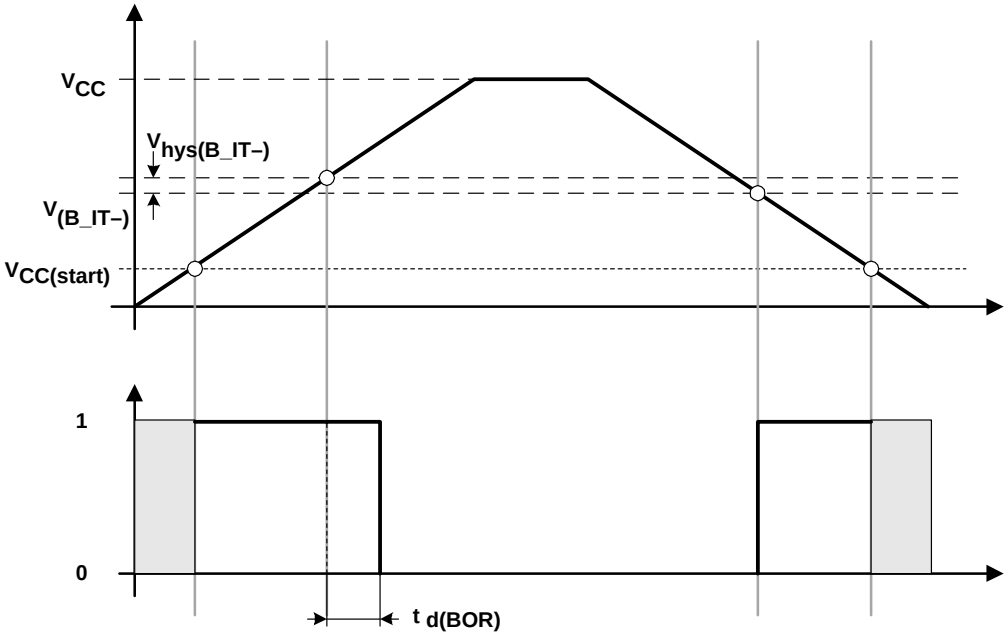


Figure 17. POR/Brownout Reset (BOR) vs Supply Voltage

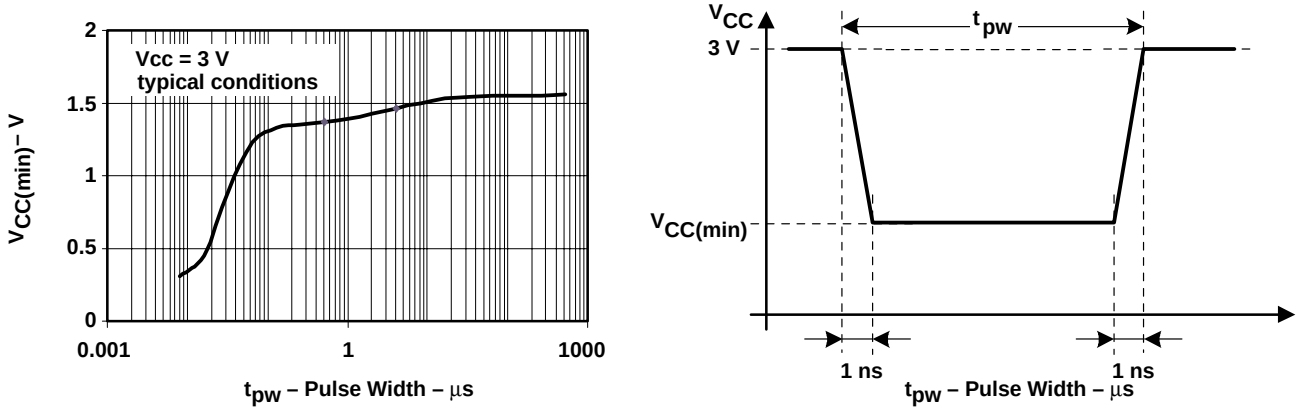


Figure 18. $V_{(CC)min}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

typical characteristics

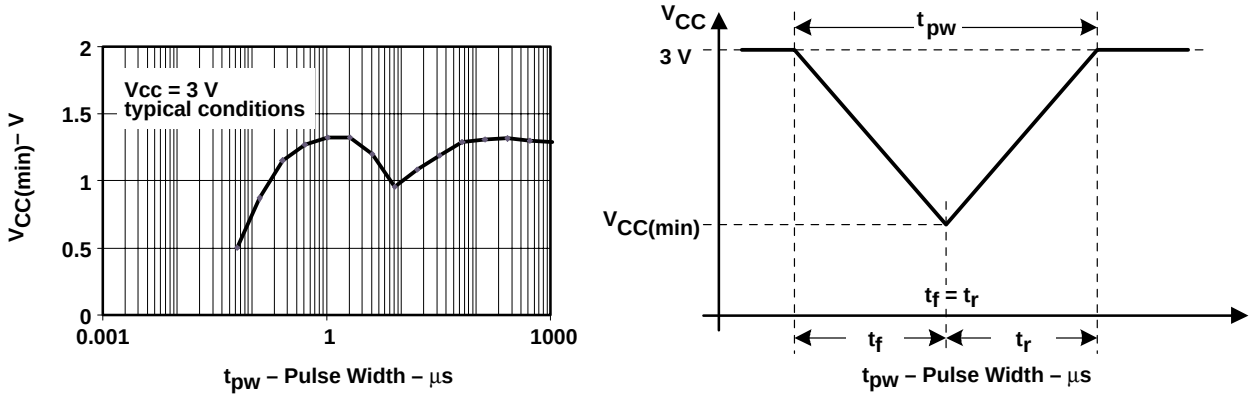


Figure 19. $V_{CC(min)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

SVS (supply voltage supervisor/monitor)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{(SVSR)}$	$dV_{CC}/dt \geq 30$ V/ms (see Figure 20)		5		150	μs
	$dV_{CC}/dt \leq 30$ V/ms				2000	μs
$t_{d(SVSon)}$	SVSon, switch from VLD=0 to VLD ≠ 0, V_{CC} = 3 V		20		150	μs
t_{settle}	VLD ≠ 0‡				12	μs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \leq 3$ V/s (see Figure 20)			1.55	1.7	V
$V_{hys(B\_IT-)}$	$V_{CC}/dt \leq 3$ V/s (see Figure 20)	VLD = 1	70	120	155	mV
		VLD = 2 .. 14	$V_{(SVS\_IT-)}$ x 0.004		$V_{(SVS\_IT-)}$ x 0.008	
	$V_{CC}/dt \leq 3$ V/s (see Figure 20), External voltage applied on A7	VLD = 15	4.4		10.4	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s (see Figure 20)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61†	
		VLD = 13	3.24	3.5	3.76†	
		VLD = 14	3.43	3.7†	3.99†	
	$V_{CC}/dt \leq 3$ V/s (see Figure 20), External voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	μA

† The recommended operating voltage range is limited to 3.6 V.

‡ t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTE 1: The current consumption of the SVS module is not included in the I_{CC} current consumption data.

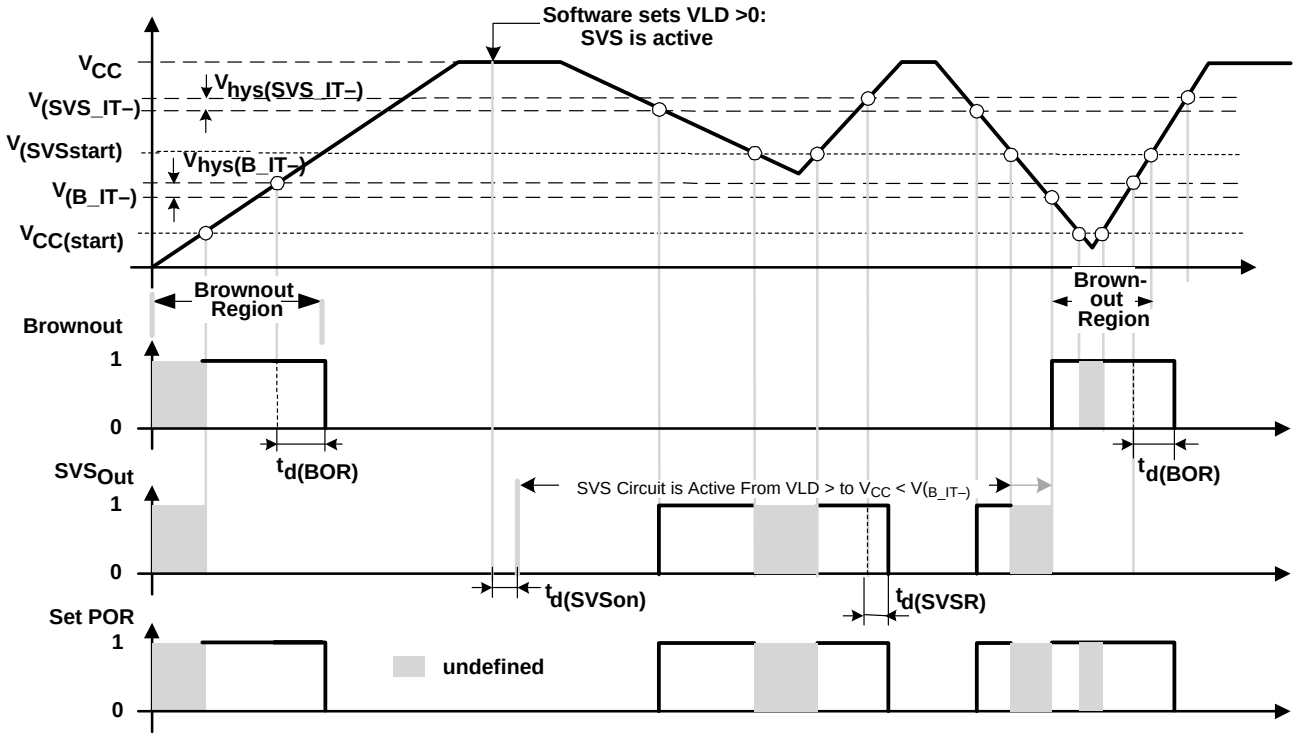


Figure 20. SVS Reset (SVSR) vs Supply Voltage

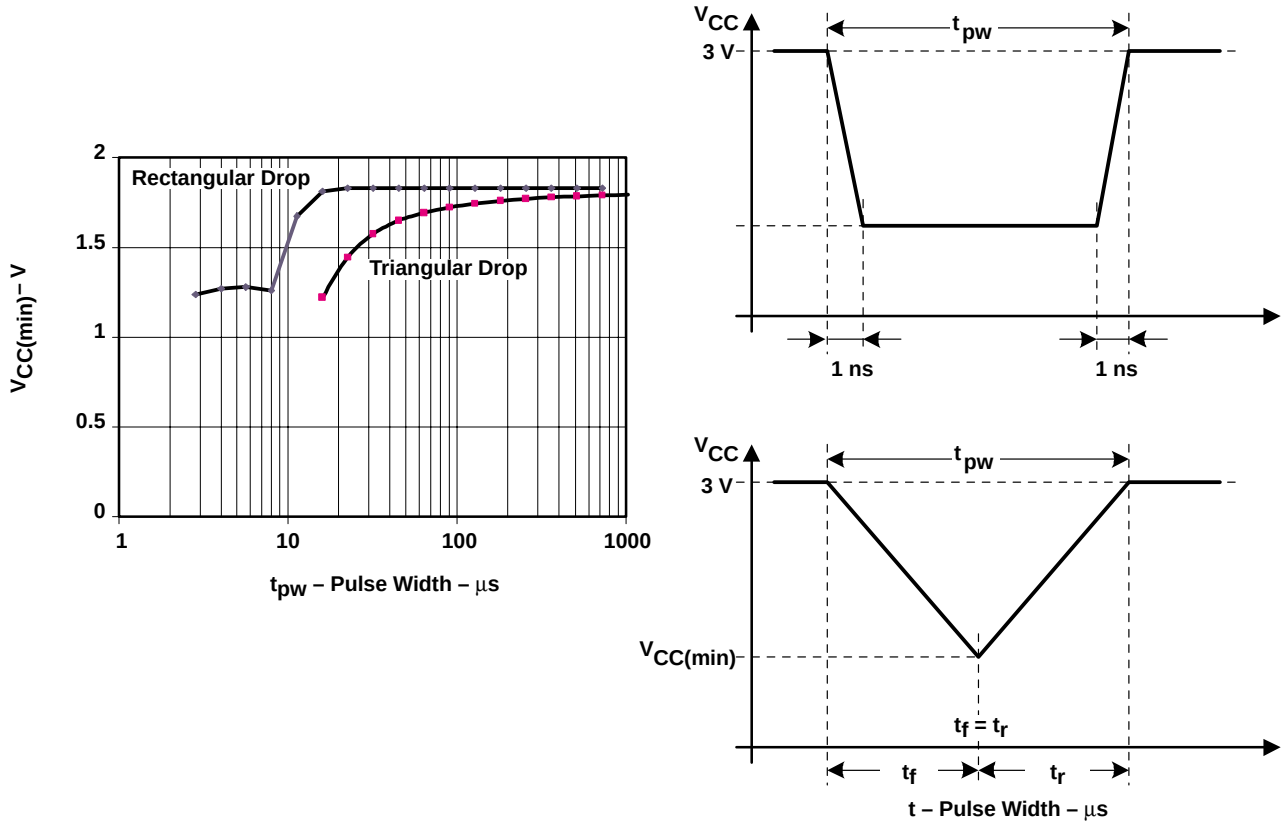


Figure 21. $V_{CC(min)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

DCO

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$=01E0h, FN_8=FN_4=FN_3=FN_2=0, D = 2, DCO+= 0	2.2 V/3 V		1		MHz
$f_{(DCO2)}$	FN_8=FN_4=FN_3=FN_2=0 , DCO+ = 1	2.2 V	0.23	0.41	0.82	MHz
		3 V	0.3	0.57	1.2	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=FN_2=0, DCO+ = 1, (see Note 1)	2.2 V	2.25	4	8	MHz
		3 V	3	5.6	11.2	
$f_{(DCO2)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCO+ = 1	2.2 V	0.45	0.85	1.75	MHz
		3 V	0.6	1.2	2.4	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCO+ = 1, (see Note 1)	2.2 V	4.4	8	16.5	MHz
		3 V	6	11	22.5	
$f_{(DCO2)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCO+ = 1	2.2 V	0.73	1.3	2.7	MHz
		3 V	1	1.85	3.9	
$f_{(DCO27)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x;, DCO+ = 1, (see Note 1)	2.2 V	6.5	12	24	MHz
		3 V	9	16.5	34	
$f_{(DCO2)}$	FN_8=0, FN_4= 1, FN_3= FN_2=x; DCO+ = 1	2.2 V	1.1	2.1	4.3	MHz
		3 V	1.6	2.9	6	
$f_{(DCO27)}$	FN_8=0, FN_4=1, FN_3= FN_2=x; DCO+ = 1, (see Note 1)	2.2 V	9.5	18	38	MHz
		3 V	13	25	52	
$f_{(DCO2)}$	FN_8=1, FN_4=FN_3=FN_2=x; DCO+ = 1	2.2 V	2.2	4	8.2	MHz
		3 V	3	5.6	12	
$f_{(DCO27)}$	FN_8=1,FN_4=FN_3=FN_2=x,DCO+ = 1, (see Note 1)	2.2 V	17.5	32	65	MHz
		3 V	24	45	94	
S	$f_{(NDCO)+1} = f_{(NDCO)}$	2 < TAP ≤ 20	1.06		1.13	
		TAP > 20	1.1		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2, DCO+ = 0, (see Note 2)	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2, DCO+ = 0 (see Note 2)		0	5	15	%/V

NOTES: 1. Please do not exceed the maximum system frequency.
2. This parameter not production tested.

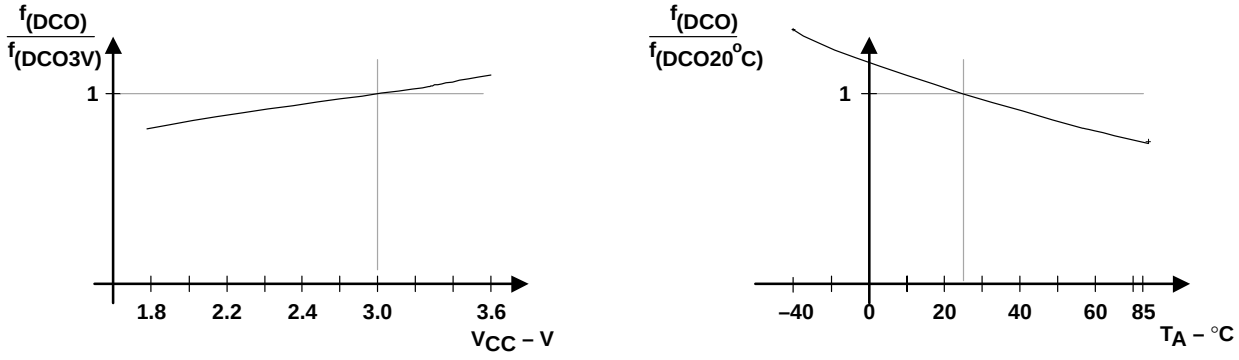


Figure 22. DCO Frequency vs Supply Voltage (V_{CC}) and vs Ambient Temperature

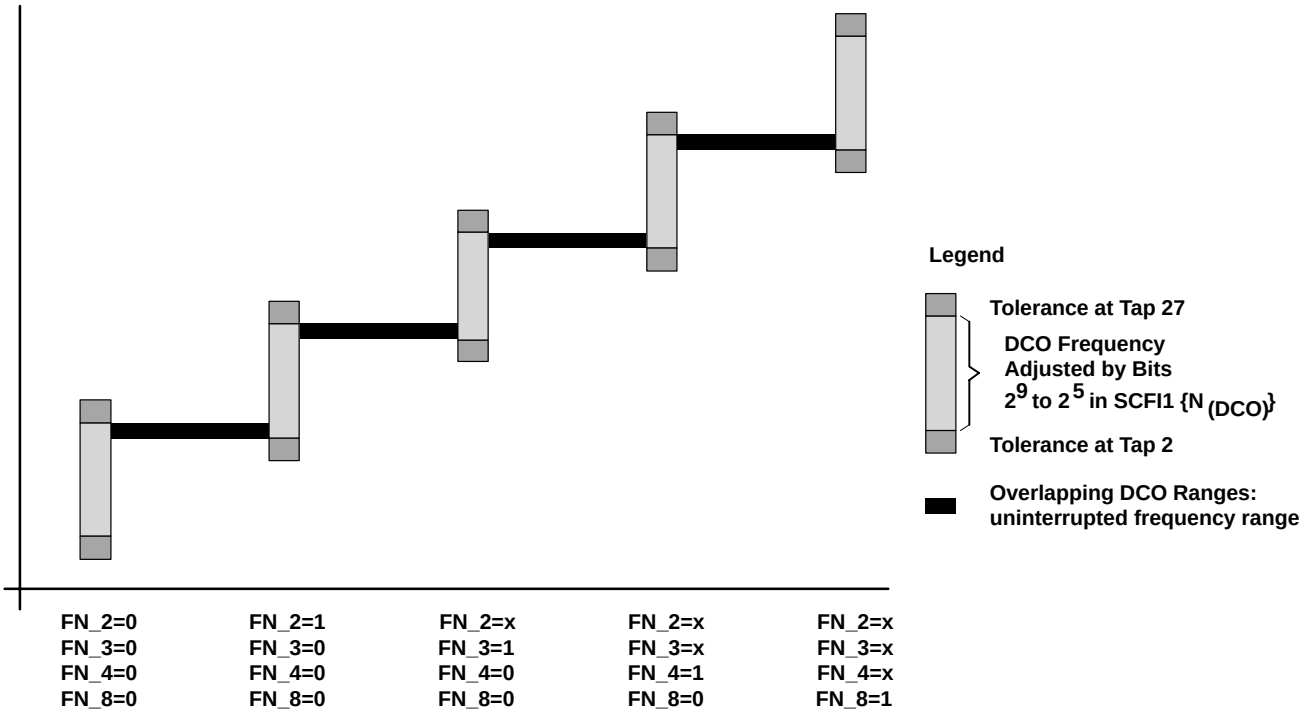


Figure 23. Five Overlapping DCO Ranges Controlled by FN_x Bits

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1 oscillator (see Note 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{(XIN)}$	Integrated input capacitance	OscCap = 0, V_{CC} = 2.2 V / 3 V		0		pF
		OscCap = 1, V_{CC} = 2.2 V / 3 V		10		
		OscCap = 2, V_{CC} = 2.2 V / 3 V		14		
		OscCap = 3, V_{CC} = 2.2 V / 3 V		18		
$C_{(XOUT)}$	Integrated output capacitance	OscCap = 0, V_{CC} = 2.2 V / 3 V		0		pF
		OscCap = 1, V_{CC} = 2.2 V / 3 V		10		
		OscCap = 2, V_{CC} = 2.2 V / 3 V		14		
		OscCap = 3, V_{CC} = 2.2 V / 3 V		18		

NOTES: 1. The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is $(X_{(CIN)} \times X_{(COUT)}) / (X_{(CIN)} + X_{(COUT)})$. This is independent of XST_FLL.

2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
   - Keep as short of a trace as possible between the F43x/44x and the crystal.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, XT2 oscillator (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
X_{CIN}	Integrated input capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{COUT}	Integrated output capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{INL}	Input levels at XIN, XOUT	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{CC}$	V
X_{INH}			$0.8 \times V_{CC}$		V_{CC}	V

NOTE 1: The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.

USART0, USART1 (see Note 2)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(\tau)}$	USART0/1: deglitch time	V_{CC} = 2.2 V	200	430	800	ns
		V_{CC} = 3 V	150	280	500	

NOTE 2: The signal applied to the USART0/1 receive signal/terminal (URXD0/1) should meet the timing requirements of $t_{(t)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(t)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0/1 line.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, power supply and input range conditions (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together AV_{SS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{CC(min)}$		0 mA ≤ $I_{(Load)}$ ≤ 0.5 mA		V_{REF+}		V_{REF+} + 150 mV	
		0.5 mA ≤ $I_{(Load)}$ ≤ 1.5 mA		V_{REF+}		V_{REF+} + 350 mV	
$V_{O(REF+)}$	Positive built-in reference voltage output	2_5 V = 1 for 2.5-V built-in reference 2_5 V = 0 for 1.5-V built-in reference $I_{(VREF+)}$ ≤ $I_{(VREF+\_max)}$	V_{CC} = 3 V	2.4	2.5	2.6	V
			V_{CC} = 2.2 V/3 V	1.44	1.5	1.56	
$I_{L(VREF+)}$	Load current out of VREF+ terminal		V_{CC} = 2.2 V	0.01		–0.5	mA
			V_{CC} = 3 V			–1	
$I_{L(VREF+)}$†	Load-current regulation VREF+ terminal	$I_{(VREF+)}$ = 500 µA ±100 µA Analog input voltage ~0.75 V; 2_5 V = 0	V_{CC} = 2.2 V			±2	LSB
			V_{CC} = 3 V			±2	
		$I_{(VREF+)}$ = 500 µA ± 100 µA Analog input voltage ~1.25 V; 2_5 V = 1	V_{CC} = 3 V			±2	LSB
$I_{L(VREF+)}$‡	Load current regulation VREF+ terminal	$I_{(VREF+)}$ =100 µA → 900 µA, VCC = 3 V, ax ~0.5 x VREF+ Error of conversion result ≤ 1 LSB	$C_{(VREF+)}$ = 5 µF			20	ns
$V_{ref(VREF+)}$	Positive external reference voltage input	VeREF+ > VeREF–/VeREF– (see Note 2)		1.4		$V_{(AVCC)}$	V
$V_{ref(VREF-/VeREF-)}$	Negative external reference voltage input	VeREF+ > VeREF–/VeREF– (see Note 3)		0		1.2	V

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 1. The leakage current is defined in the leakage current table with P6.x/Ax parameter.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
4. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

12-bit ADC, power supply and input range conditions (see Note 1) (continued)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
(V_{eREF+} – $V_{REF–}$/$V_{eREF–}$)	Differential external reference voltage input	VeREF+ > VeREF–/VeREF– (see Note 4)		1.4		$V_{(AVCC)}$	V
$V_{I(P6.x/Ax)}$	Analog input voltage range (see Note 5)	All P6.0/A0 to P6.7/A7/SVSin terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1 $0 \le x \le 7$; $V_{(AVSS)} \le V_{I(P6.x/Ax)} \le V_{(AVCC)}$		0		$V_{(AVCC)}$	V
$I_{DD(ADC12)}$	Operating supply current into AV_{CC} terminal (see Note 6)	$f_{(ADC12CLK)}$ = 5 MHz ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	V_{CC} = 2.2 V		0.65	1.3	mA
			V_{CC} = 3 V		0.8	1.6	
$I_{DD(REF+)}$	Operating supply current into AV_{CC} terminal (see Note 7)	$f_{(ADC12CLK)}$ = 5 MHz ADC12ON = 0, REFON = 1, 2_5V = 1	V_{CC} = 3 V		0.5	0.8	mA
	Operating supply current (see Note 7)	$f_{(ADC12CLK)}$ = 5 MHz ADC12ON = 0, REFON = 1, 2_5V = 0	V_{CC} = 2.2 V		0.5	0.8	
			V_{CC} = 3 V		0.5	0.8	

NOTES: 5. The analog input voltage range must be within the selected reference voltage range V_{R+} to $V_{R–}$ for valid conversion results.
6. The internal reference supply current is not included in current consumption parameter $I_{DD(ADC12)}$.
7. The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

12-bit ADC, built-in reference (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{DD(VeREF+)}$	Static input current (see Note 2)	0 V ≤ VeREF+ ≤ $V_{(AVCC)}$	V_{CC} = 2.2 V/3 V			±1	µA
$I_{DD(VREF–/VeREF–)}$	Static input current (see Note 2)	0 V ≤ VeREF– ≤ $V_{(AVCC)}$	V_{CC} = 2.2 V/3 V			±1	µA
$C_{(VREF+)}$	Capacitance at pin VREF+ (see Note 3)	REFON = 1, 0 mA ≤ $I_{(VREF+)}$ ≤ $I_{(VREF\_max)}$	V_{CC} = 2.2 V/3 V	5	10		µF
C_i‡	Input capacitance (see Note 4)	Only one terminal can be selected at one time, P6.x/Ax	V_{CC} = 2.2 V			40	pF
Z_i‡	Input MUX ON resistance (see Note 4)	0 V ≤ $V_{(Ax)}$ ≤ $V_{(AVCC)}$	V_{CC} = 3 V			2000	Ω
$T_{(REF+)}$†	Temperature coefficient of built-in reference	$I_{(VREF+)}$ is a constant in the range of 0 mA ≤ $I_{(VREF+)}$ ≤ 1 mA	V_{CC} = 2.2 V/3 V			±100	ppm/°C

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 1. The voltage source on VeREF+ and VREF–/VeREF– needs to have low-dynamic impedance for 12-bit accuracy to allow the charge to settle for this accuracy (See Figures 16 and 17).
2. The external reference is used during conversion to charge and discharge the capacitance array. The dynamic impedance should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
3. The internal buffer operational amplifier and the accuracy specifications require an external capacitor.
4. The input capacitance is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy. All INL and DNL tests uses two capacitors between pins VREF+ and AV_{SS} and VREF–/VeREF– and AV_{SS}: 10-µF tantalum and 100-nF ceramic.

timing requirements

12-bit ADC, timing parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{s(REF\_ON)}$†	Settle time of internal reference voltage (see Figure 24 and Note 1)	$I_{(VREF+)}$ = 0.5 mA, $C_{(VREF+)}$ = 10 µF, VREF+ = 1.5 V, $V_{(AVCC)}$ = 2.2 V				17	ms
$f_{(ADC12OSC)}$		ADC12DIV=0 [$f_{(ADC12CLK)}$ = $f_{(ADC12OSC)}$]	V_{CC} = 2.2 V/3 V	3.7		6.3	MHz
t_c	Conversion time	$AV_{CC(min)} \le V_{(AVCC)} \le AV_{CC(max)}$, $C_{(VREF+)} \ge 5$µF, internal oscillator, f_{OSC} = 3.7 MHz to 6.3 MHz	V_{CC} = 2.2 V/3 V	2.06		3.51	µs
		$AV_{CC(min)} \le V_{(AVCC)} \le AV_{CC(max)}$, External $f_{ADC12(CLK)}$ from ACLK or MCLK or SMCLK: ADC12SSEL ≠ 0			13×ADC12DIV× $1/f_{ADC12(CLK)}$		µs
$t_{s(ADC12ON)}$‡	Settle time of the ADC	$AV_{CC(min)} \le V_{(AVCC)} \le AV_{CC(max)}$ (see Note 2)				100	ns
$t_{(Sample)}$‡	Sampling time	$V_{(AVCC\_min)} \le V_{(AVCC)} \le V_{(AVCC\_max)}$ $R_{i(source)}$ = 400 Ω, Z_i = 1000 Ω, C_i = 30 pF $\tau = [R_{i(source)} + Z_i] \times C_i$, (see Note 3)	V_{CC} = 3 V	1220			ns
			V_{CC} = 2.2 V	1400			

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 1. The condition is that the error in a conversion started after $t_{s(REF\_ON)}$ is less than ±0.5 LSB. The settling time depends on the external capacitive load.
2. The condition is that the error in a conversion started after $t_{s(ADC12ON)}$ is less than ±0.5 LSB. The reference and input signal are already settled.
3. Ten Tau (τ) are needed to get an error of less than ±0.5 LSB. $t_{(Sample)} = 10 \times (R_i + Z_i) \times C_i + 800$ ns

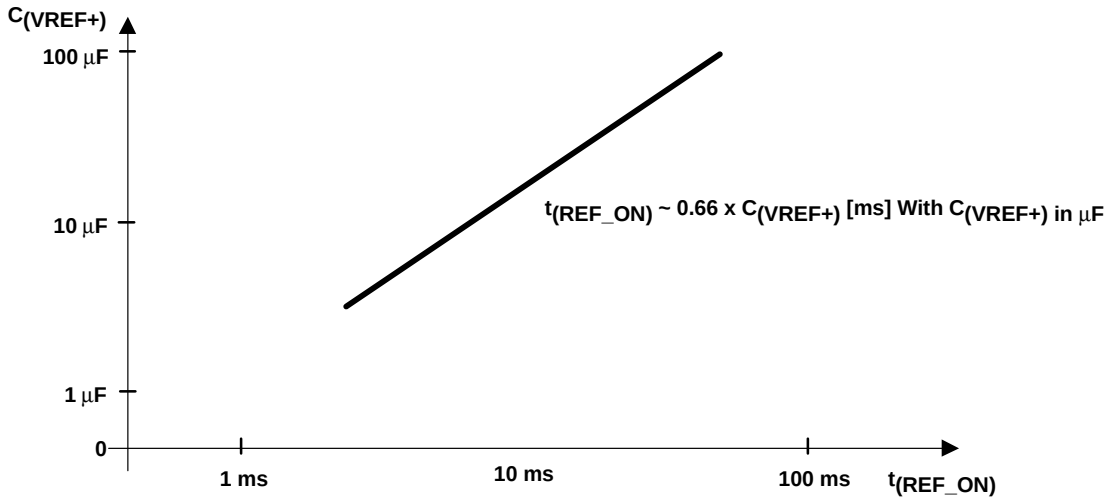


Figure 24. Typical Settling Time of Internal Reference $t_{(REF\_ON)}$ vs External Capacitor on VREF+

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

12-bit ADC, linearity parameters, V_{CC} = 2.2 V/3 V

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$E_{(I)}$	Integral linearity error	1.4 V ≤ (VeREF+ – VREF–/VeREF–) min ≤ 1.6 V			±2	LSB
		1.6 V < [V(eREF+) – V(REF–)/V(eREF–)] min ≤ [$V_{(AVCC)}$]			±1.7	
E_D	Differential linearity error	(VeREF+ – VREF–/VeREF–)min ≤ (VeREF+ – VREF–/VeREF–), $C_{(VREF+)}$ = 10 µF (tantalum) and 100 nF (ceramic)			±1	LSB
E_O	Offset error†	(VeREF+ – VREF–/VeREF–)min ≤ (VeREF+ – VREF–/VeREF–), Internal impedance of source R_i < 100 Ω, $C_{(VREF+)}$ = 10 µF (tantalum) and 100 nF (ceramic)		±2	±4	LSB
E_G	Gain error†	(VeREF+ – VREF–/VeREF–)min ≤ (VeREF+ – VREF–/VeREF–), $C_{(VREF+)}$ = 10 µF (tantalum) and 100 nF (ceramic)		±1.1	±2	LSB
$E_{(T)}$	Total unadjusted error†	(VeREF+ – VREF–/VeREF–)min ≤ (VeREF+ – VREF–/VeREF–), $C_{(VREF+)}$ = 10 µF (tantalum) and 100 nF (ceramic)		±2	±5	LSB

† Not production tested, limits characterized

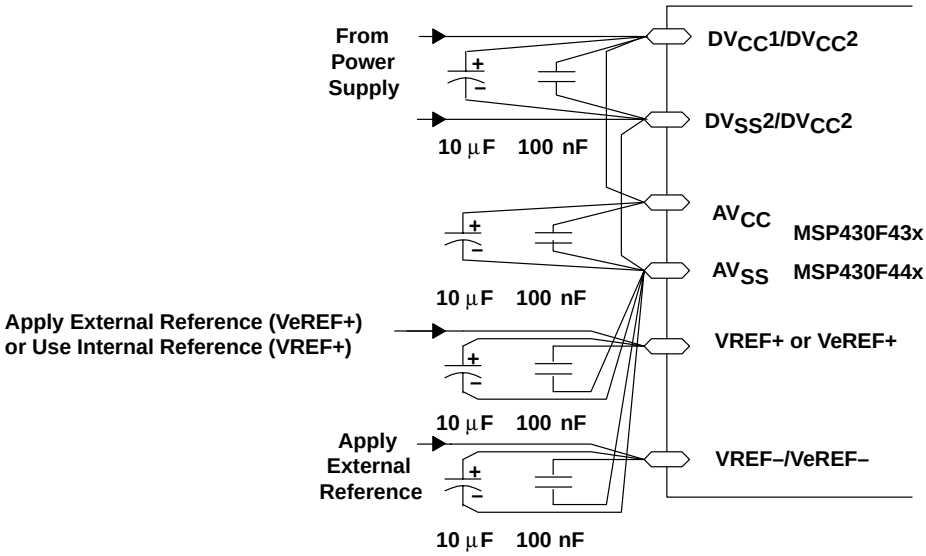


Figure 25. Supply Voltage and Reference Voltage Design VREF–/VeREF– External Supply

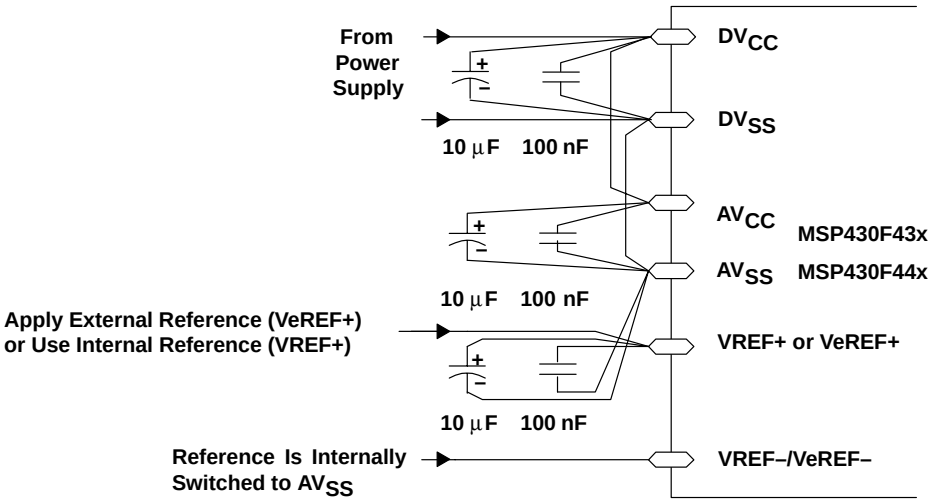


Figure 26. Supply Voltage and Reference Voltage Design VREF–/VeREF– = AV_{SS}, Internally Connected

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

12-bit ADC, temperature sensor and built-in Vmid

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{CC(SENSOR)}$	Operating supply current into AVCC terminal (see Note 1)	$V_{(REFON)}$ = 0, INCH = 0Ah, ADC12ON = NA, T_A = 25°C	V_{CC} = 2.2 V		40	120	µA
			V_{CC} = 3 V		60	160	
$V_{(SENSOR)}$†		ADC12ON = 1, INCH = 0Ah, T_A = 0°C	V_{CC} = 2.2 V/3 V		986	986±5%	mV
$TC_{(SENSOR)}$†		ADC12ON = 1, INCH = 0Ah	V_{CC} = 2.2 V/3 V		3.55	3.55±3%	mV/°C
$t_{s(SENSOR)}$†	Sample time required if channel 10 is selected (see Note 2)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	V_{CC} = 2.2 V/3 V	30			µs
$V_{(MID)}$	AVCC divider at channel 11	ADC12ON = 1, INCH = 0Bh, $V_{(MID)}$ is ~0.5 x $V_{(AVCC)}$	V_{CC} = 2.2 V		1.1	1.1±0.04	V
			V_{CC} = 3 V		1.5	1.5±0.04	
$t_{(ON\_VMID)}$	On-time if channel 11 is selected (see Note 3)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	V_{CC} = 2.2 V/3 V			NA	ns

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 1. The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and $V_{(REFON)}$ = 1), or (ADC12ON=1 AND INCH=0Ah and sample signal is high). Therefore it includes the constant current through the sensor and the reference.
2. The typical equivalent impedance of the sensor is 51 kΩ. The sample time needed is the sensor-on time $t_{(SENSOR\_ON)}$
3. The on-time $t_{(ON\_VMID)}$ is identical to sampling time $t_{(Sample)}$; no additional on time is needed.

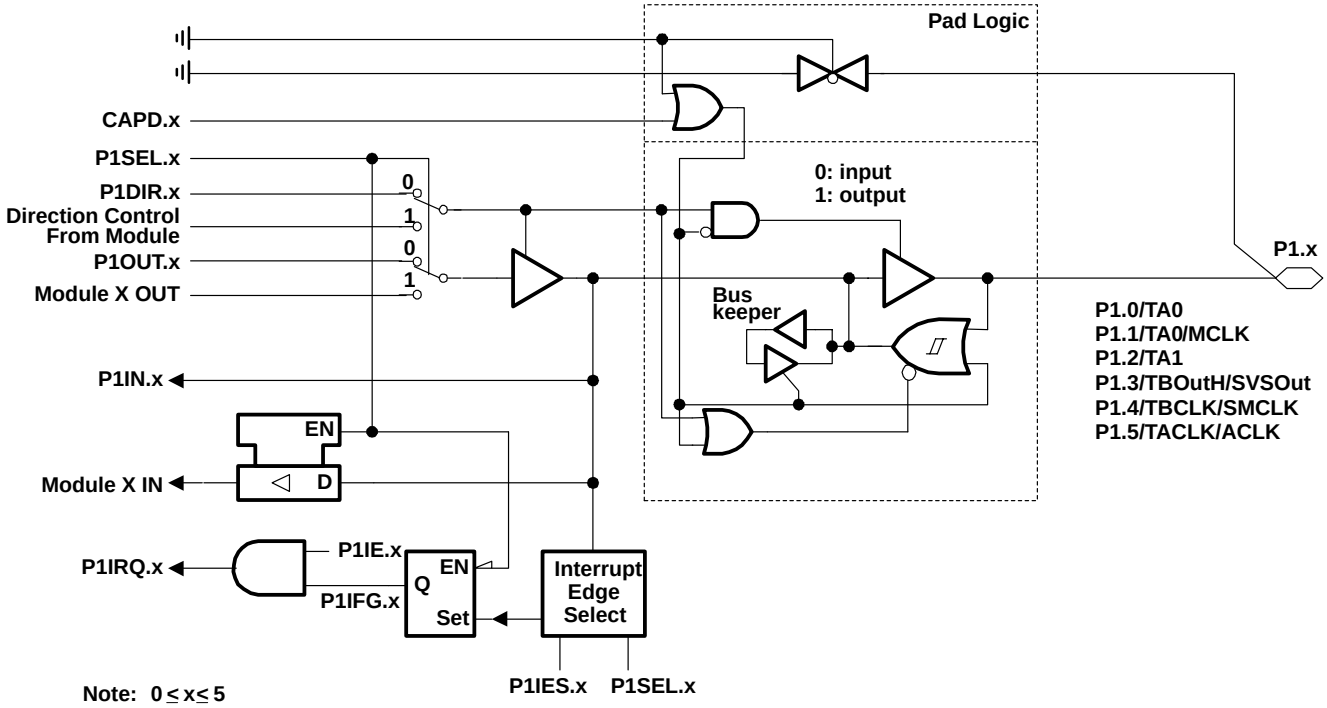
JTAG, program memory and fuse

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(TCK)}$	JTAG/Test (see Note 4)	TCK frequency	V_{CC} = 2.2 V	DC		5	MHz
			V_{CC} = 3 V	DC		10	
		Pull-up resistors on TMS, TCK, TDI (see Note 1)	V_{CC} = 2.2 V/3 V	25	60	90	kΩ
$V_{(FB)}$	JTAG/fuse (see Note 2)	Fuse-blow voltage, F versions (see Note 3)	V_{CC} = 2.2 V/3 V	6		7	V
$I_{(FB)}$		Supply current on TDI with fuse blown				100	mA
		Time to blow the fuse				1	ms
$I_{(DD-PGM)}$	F-versions only (see Note 4)	Current from DV_{CC} when programming is active	V_{CC} = 2.7 V/3.6 V		3	5	mA
$I_{(DD-Erase)}$		Current from DV_{CC} when erase is active	V_{CC} = 2.7 V/3.6 V		3	5	mA
$t_{(retention)}$	F-versions only	Write/erase cycles		10^4	10^5		cycles
		Data retention T_J = 25°C		100			years

NOTES: 1. TMS, TDI, and TCK pull-up resistors are implemented in all F versions.
2. Once the fuse is blown, no further access to the MSP430 JTAG/test feature is possible. The JTAG block is switched to bypass mode.
3. The supply voltage to blow the fuse is applied to the TDI pin.
4. $f_{(TCK)}$ may be restricted to meet the timing requirements of the module selected. Duration of the program/erase cycle is determined by $f_{(FTG)}$ applied to the flash timing controller. It can be calculated as follows:
   $t_{(word\ write)} = 33 \times 1/f_{(FTG)}$
   $t_{(segment\ write,\ byte\ 0)} = 30 \times 1/f_{(FTG)}$
   $t_{(segment\ write\ end\ sequence)} = 5 \times 1/f_{(FTG)}$
   $t_{(mass\ erase)} = 5296 \times 1/f_{(FTG)}$
   $t_{(segment\ erase)} = 4817 \times 1/f_{(FTG)}$

input/output schematic

Port P1, P1.0 to P1.5, input/output with Schmitt-trigger



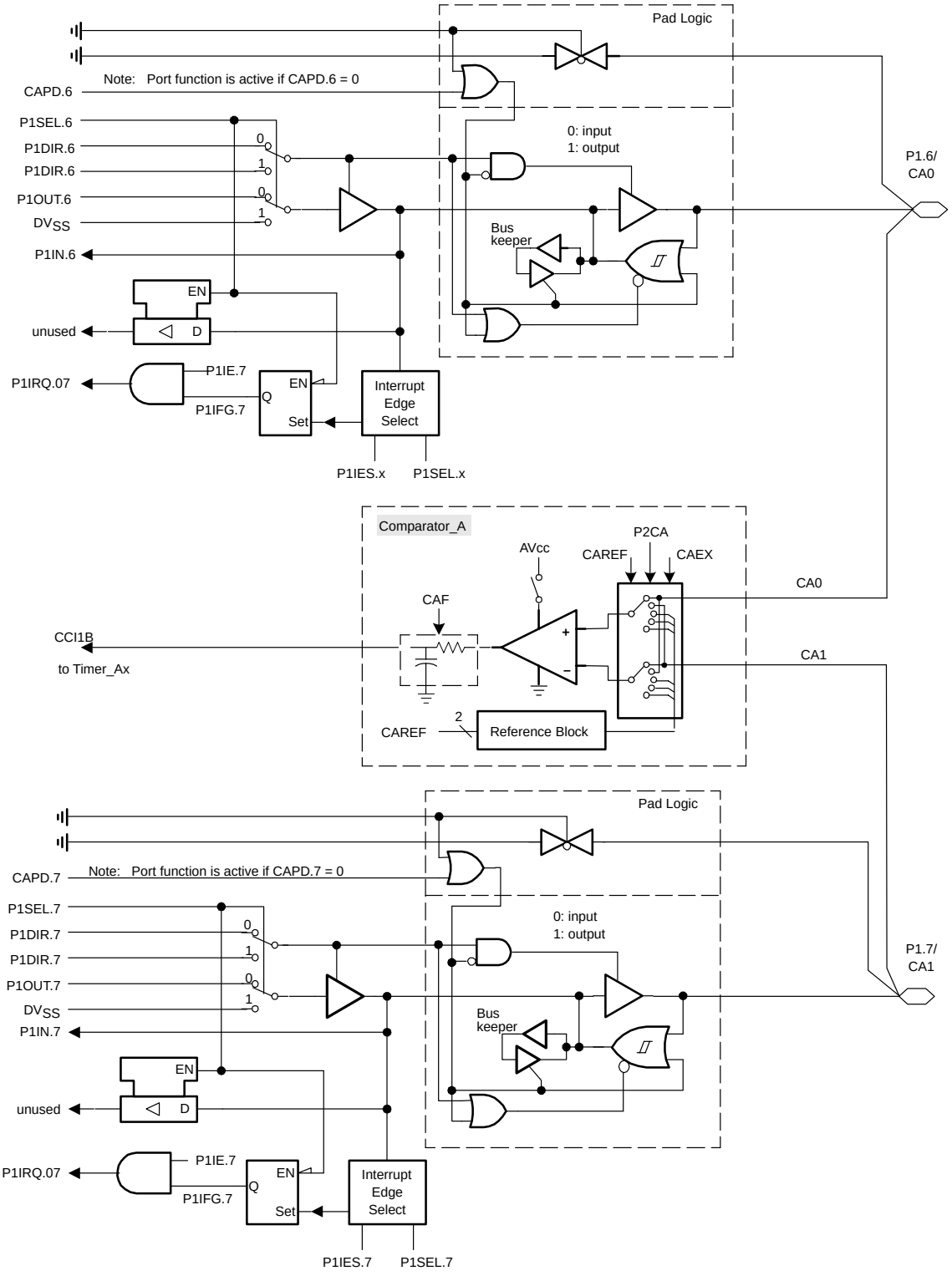
Note: $0 \le x \le 5$
Note: Port function is active if CAPD.x = 0

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	Out0 sig. †	P1IN.0	CCI0A †	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	MCLK	P1IN.1	CCI0B †	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 sig. †	P1IN.2	CCI1A †	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	SVSOut	P1IN.3	TBOutH ‡	P1IE.3	P1IFG.3	P1IES.3
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	TBCLK ‡	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	ACLK	P1IN.5	TACLK †	P1IE.5	P1IFG.5	P1IES.5

† Timer_A
‡ Timer_B

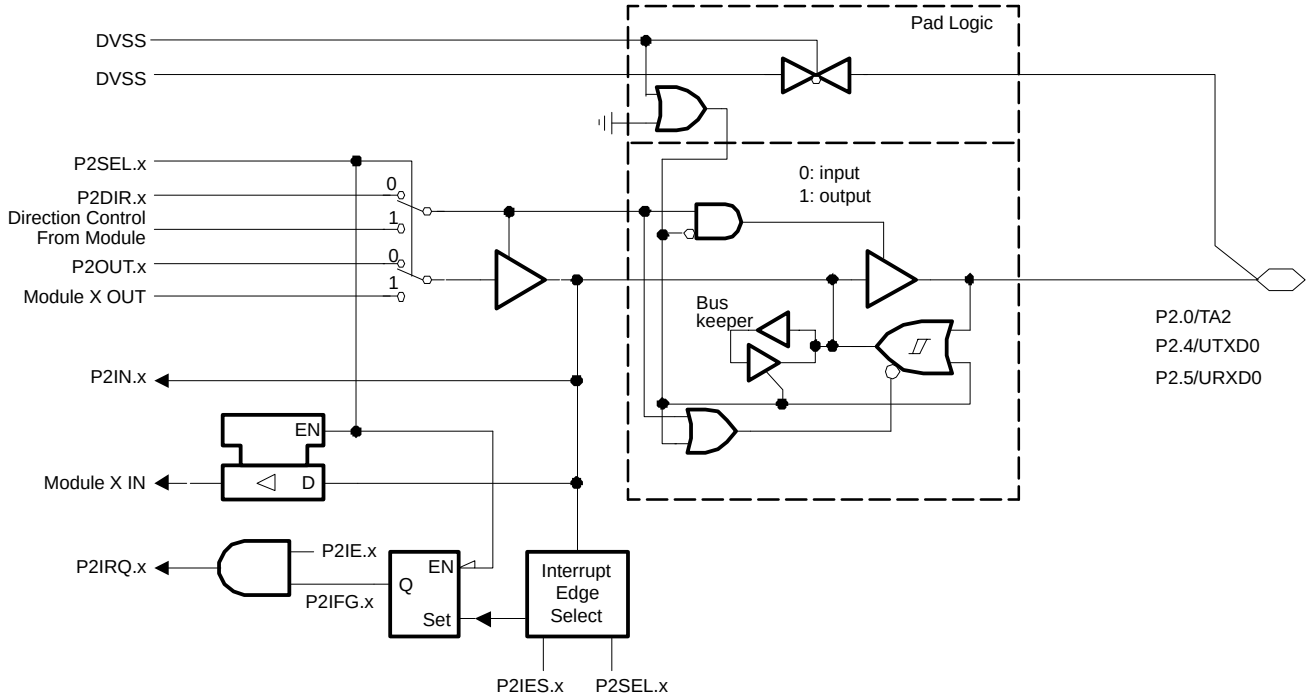
input/output schematic (continued)

Port P1, P1.6, P1.7, input/output with Schmitt-trigger



input/output schematic (continued)

port P2, P2.0, P2.4 to P2.5, input/output with Schmitt-trigger



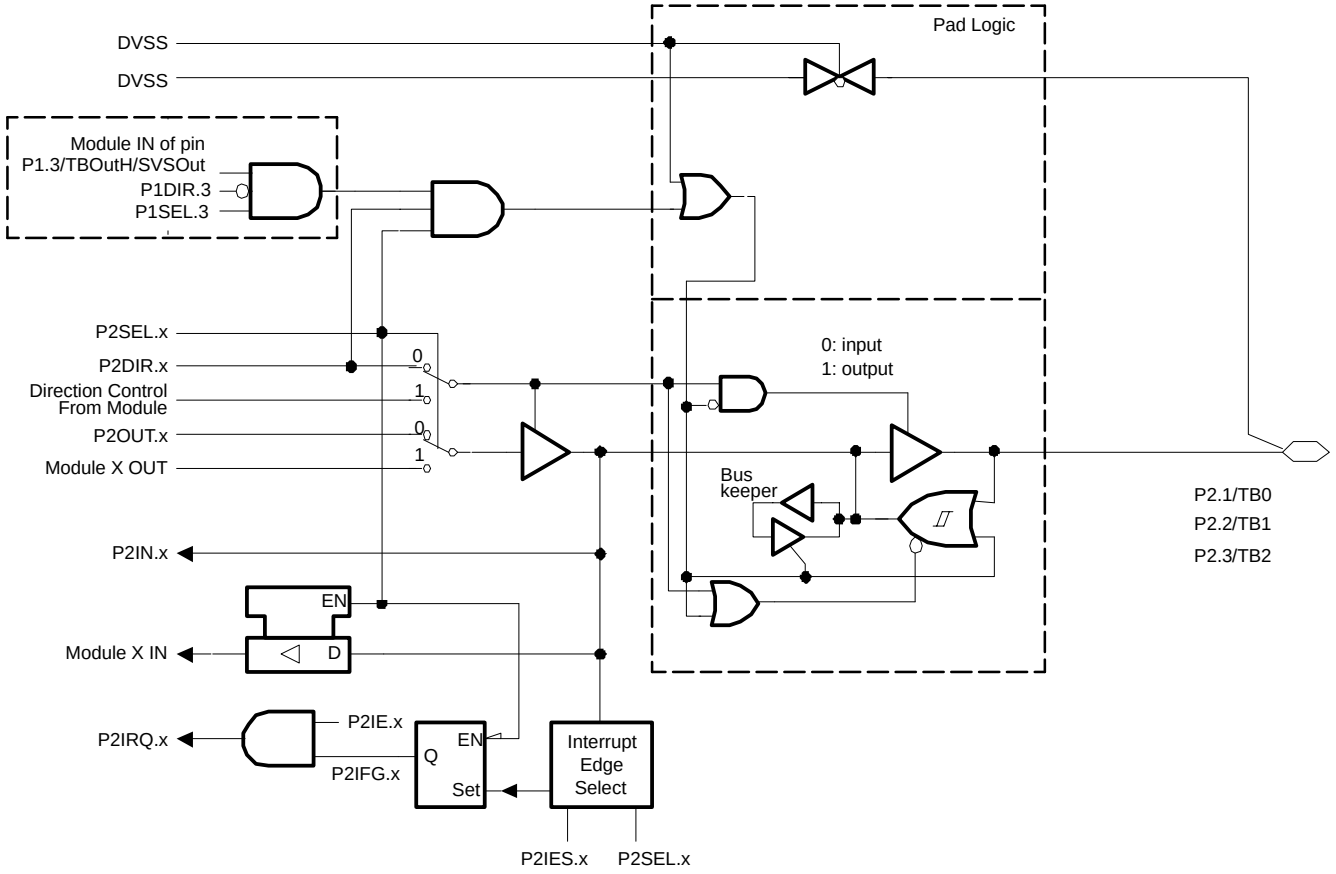
Note: x {0,4,5}

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	Out2 sig. †	P2IN.0	CCI2A†	P2IE.0	P2IFG.0	P2IES.0
P2Sel.4	P2DIR.4	DVCC	P2OUT.4	UTXD0‡	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4
P2Sel.5	P2DIR.5	DVSS	P2OUT.5	DVSS	P2IN.5	URXD0‡	P2IE.5	P2IFG.5	P2IES.5

†Timer_A
‡USART0

input/output schematic (continued)

port P2, P2.1 to P2.3, input/output with Schmitt-trigger



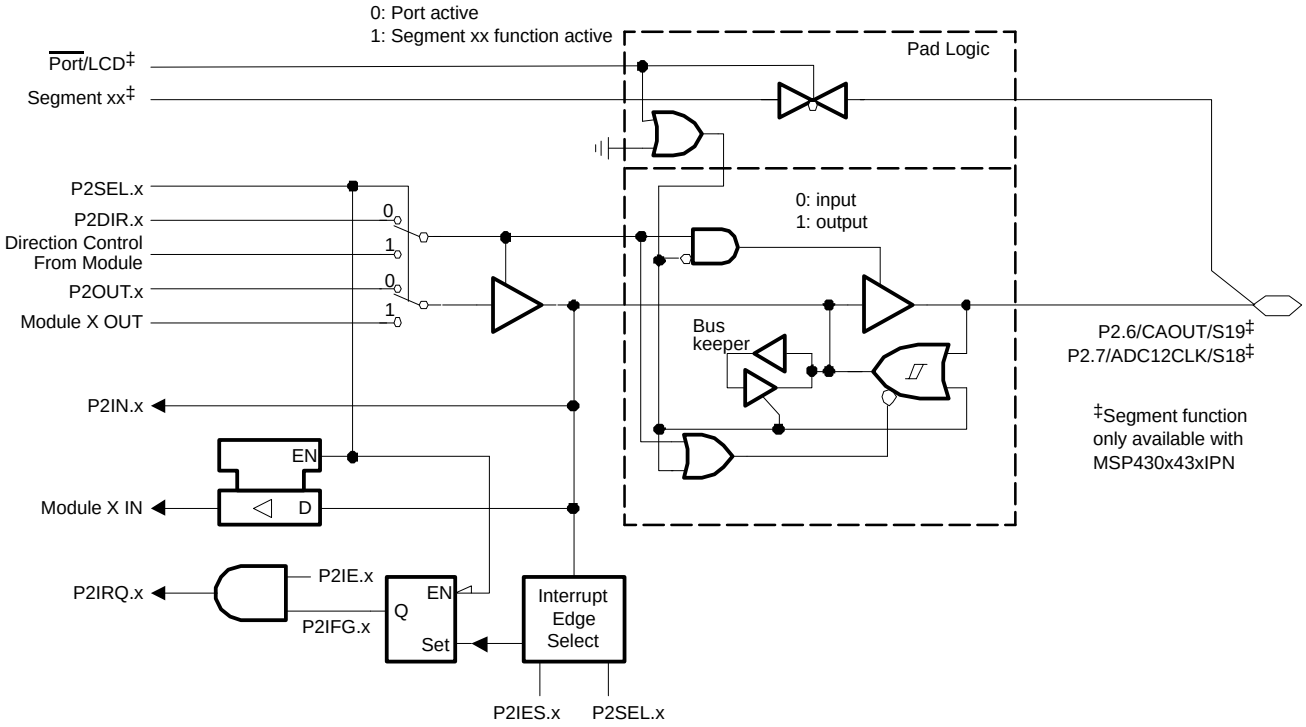
Note: $1 \le x \le 3$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	Out0 sig. †	P2IN.1	CCI0A † CCI0B	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	Out1 sig. †	P2IN.2	CCI1A † CCI1B	P2IE.2	P2IFG.2	P2IES.2
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out2 sig. †	P2IN.3	CCI2A † CCI2B	P2IE.3	P2IFG.3	P2IES.3

†Timer_B

input/output schematic (continued)

port P2, P2.6 to P2.7, input/output with Schmitt-trigger



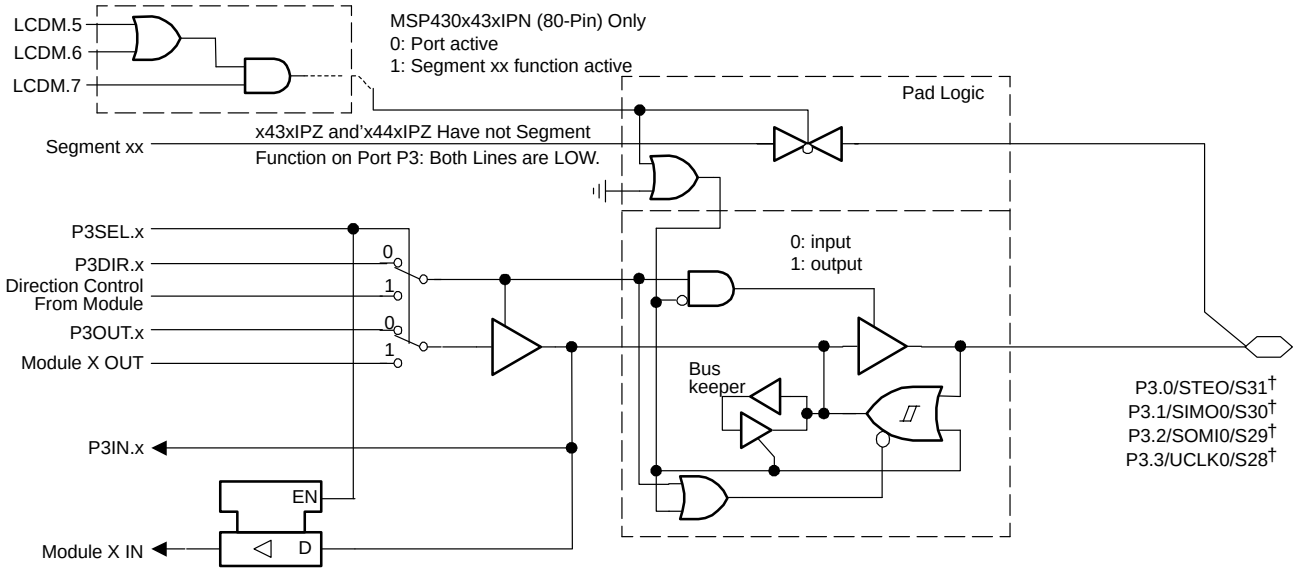
Note: $6 \le x \le 7$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x	Port/LCD ‡
P2Sel.6	P2DIR.4	P2DIR.6	P2OUT.6	CAOUT †	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6	0: LCDM<40h ‡
P2Sel.7	P2DIR.5	P2DIR.7	P2OUT.7	ADC12CLK§	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7	0: LCDM<40h ‡

† Comparator_A
‡Port/LCD signal is 1 only with MSP430xIPN and LCDM ≥40h.
§ ADC12

input/output schematic (continued)

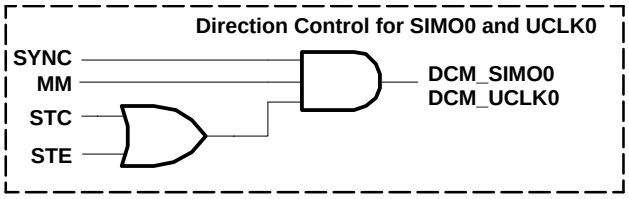
port P3, P3.0 to P3.3, input/output with Schmitt-trigger

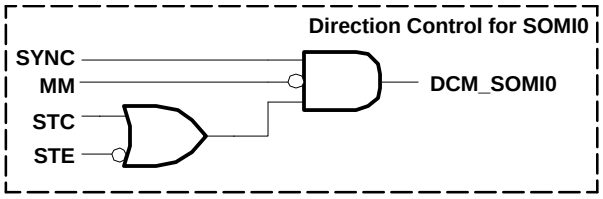


Note: $0 \le x \le 3$

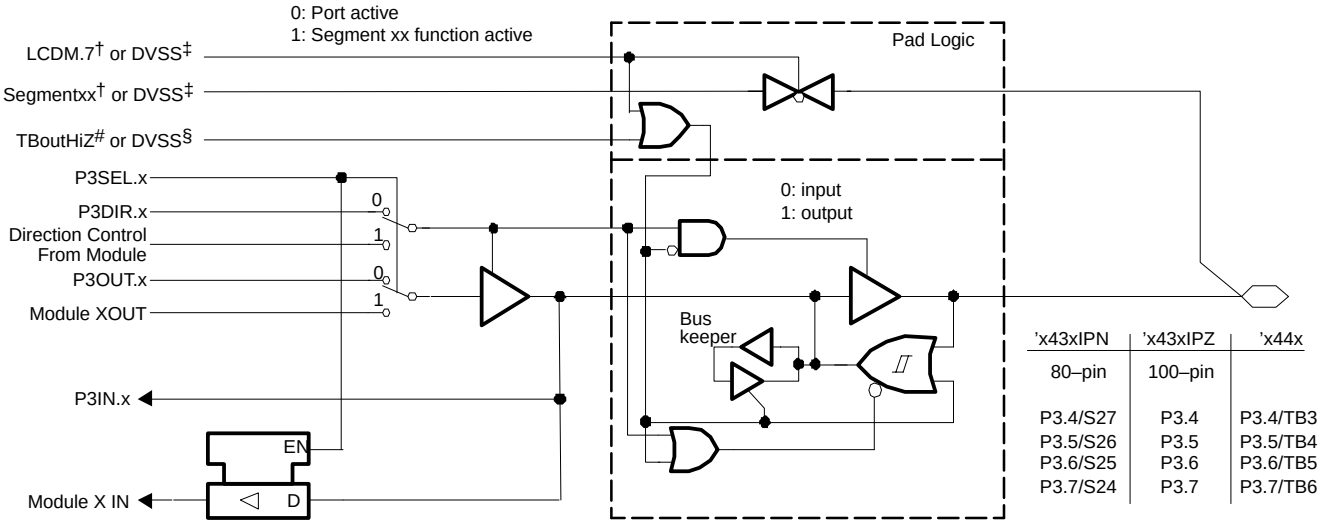
PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P3Sel.0	P3DIR.0	DV_{SS}	P3OUT.0	DV_{SS}	P3IN.0	STE0(in)
P3Sel.1	P3DIR.1	DCM_SIMO0	P3OUT.1	SIMO0(out)	P3IN.1	SIMO0(in)
P3Sel.2	P3DIR.2	DCM_SOMI0	P3OUT.2	SOMIO(out)	P3IN.2	SOMI0(in)
P3Sel.3	P3DIR.3	DCM_UCLK0	P3OUT.3	UCLK0(out)	P3IN.3	UCLK0(in)

† S24 TO S31 Shared with port function only at MSP430x43xIPN (80-pin QFP)

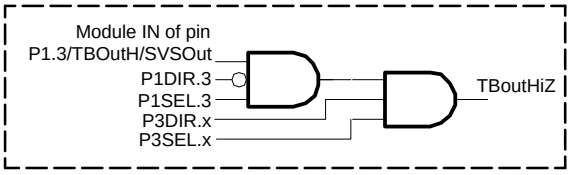




port P3, P3.4 to P3.7, input/output with Schmitt-trigger



Note: $4 \le x \le 7$

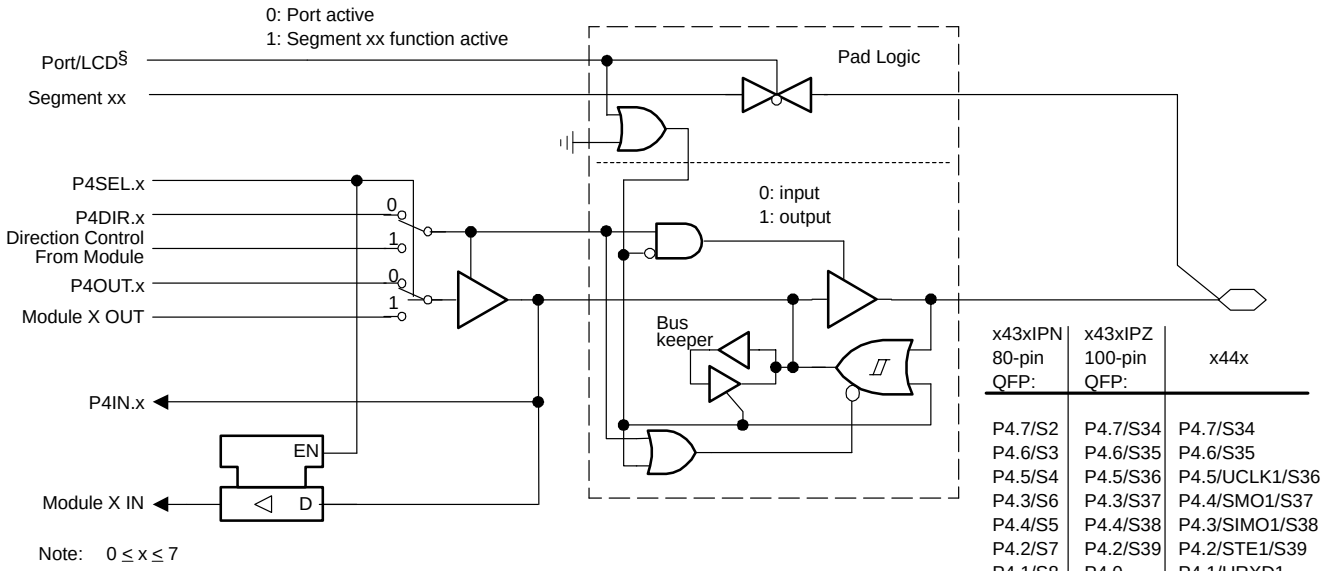


PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P3Sel.4	P3DIR.4	P3DIR.4	P3OUT.4	DVSS § OUT3 #	P3IN.4	unused § CCI3A/B#
P3Sel.5	P3DIR.5	P3DIR.5	P3OUT.5	DVSS § OUT4 #	P3IN.5	unused § CCI4A/B#
P3Sel.6	P3DIR.6	P3DIR.6	P3OUT.6	DVSS § OUT5 #	P3IN.6	unused § CCI5A/B#
P3Sel.7	P3DIR.7	P3DIR.7	P3OUT.7	DVSS § OUT6 #	P3IN.7	unused § CCI6A/B#

† MSP430x43xIPN
‡ MSP430x43xIPZ, MSP430x44xIPZ
§ MSP430x43x
# MSP430x44x

input/output schematic (continued)

port P4, P4.0 to P4.7, input/output with Schmitt-trigger



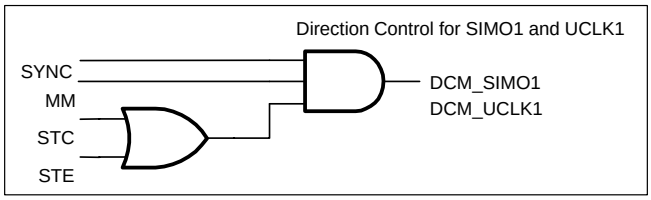
x43xIPN 80-pin QFP:	x43xIPZ 100-pin QFP:	x44x
P4.7/S2	P4.7/S34	P4.7/S34
P4.6/S3	P4.6/S35	P4.6/S35
P4.5/S4	P4.5/S36	P4.5/UCLK1/S36
P4.3/S6	P4.3/S37	P4.4/SMO1/S37
P4.4/S5	P4.4/S38	P4.3/SIMO1/S38
P4.2/S7	P4.2/S39	P4.2/STE1/S39
P4.1/S8	P4.0	P4.1/URXD1
P4.0/S9	P4.1	P4.0/UTXD1

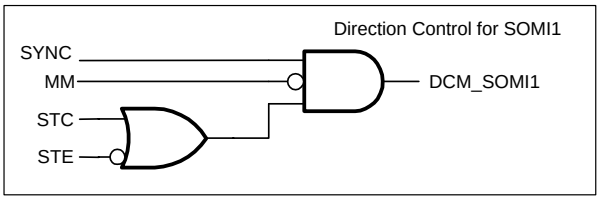
PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P4Sel.0	P4DIR.0	P4DIR.0† DV_{CC}‡	P4OUT.0	DV_{SS}† UTXD1‡	P4IN.0	unused
P4Sel.1	P4DIR.1	P4DIR.1† DV_{SS}‡	P4OUT.1	DV_{SS}	P4IN.1	unused† URXD1‡
P4Sel.2	P4DIR.2	P4DIR.2† DV_{SS}‡	P4OUT.2	DV_{SS}	P4IN.2	unused† STE1(in)‡
P4Sel.3	P4DIR.3	P4DIR3.† DCM_SIMO1‡	P4OUT.3	DV_{SS}† SIMO1(out)‡	P4IN.3	unused† SIMO1(in)‡
P4Sel.4	P4DIR.4	P4DIR4.† DCM_SOMI1‡	P4OUT.4	DV_{SS}† SOMI1(out)‡	P4IN.4	unused SOMI1(in)‡
P4Sel.5	P4DIR.5	P4DIR5.† DCM_UCLK1‡	P4OUT.5	DV_{SS}† UCLK1(out)‡	P4IN.5	unused† UCLK1(in)‡
P4Sel.6	P4DIR.4	P4DIR.6	P4OUT.6	DV_{SS}	P4IN.6	unused
P4Sel.7	P4DIR.5	P4DIR.7	P4OUT.7	DV_{SS}	P4IN.7	unused

† Signal at MSP430x43x
‡ Signal at MSP430x44x
§

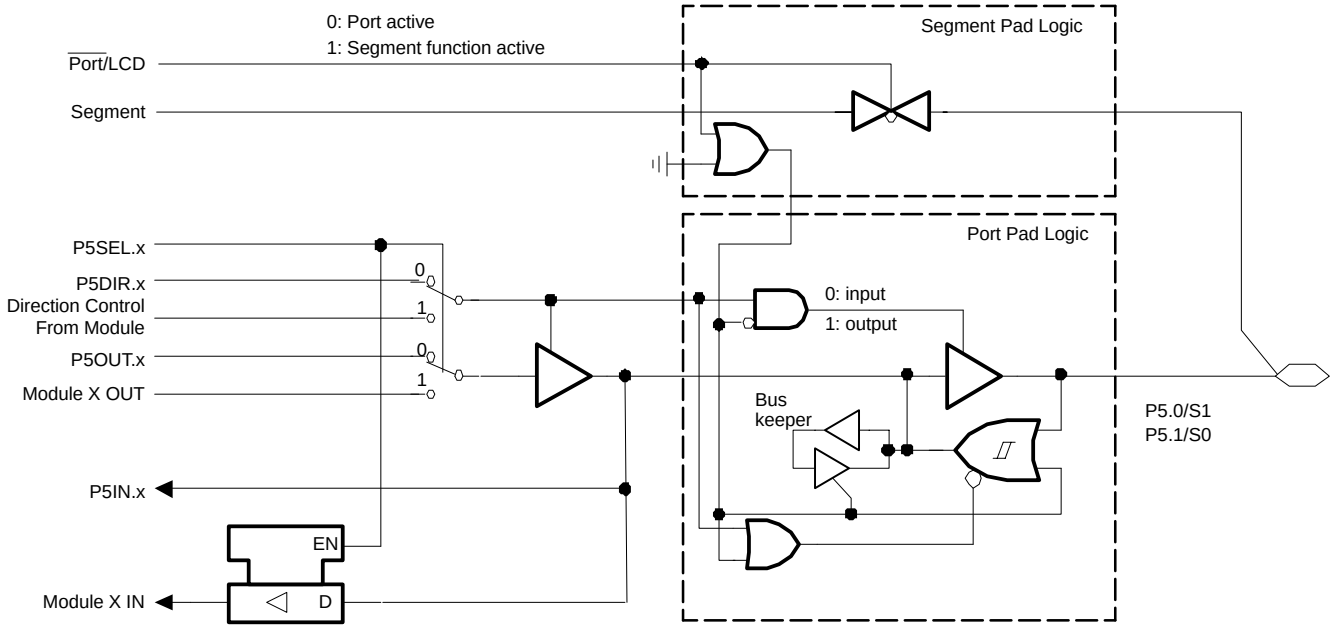
DEVICE	PORT BITS	PORT FUNCTION	LCD SEG. FUNCTION
x43xIPN 80-pin QFP	P4.0 . . .P4.7	LCDM < 020h	LVDM ≥ 020h
x43xIPZ 100-pin QFP	P4.2 . . .P4.5	LCDM < 0E0h	LVDM ≥ 0E0h
x44xIPZ 100-pin QF	P4.6 . . .P4.7	LCDM < 0C0h	LVDM ≥ 0C0h

input/output schematic (continued)





port P5, P5.0 to P5.1, input/output with Schmitt-trigger

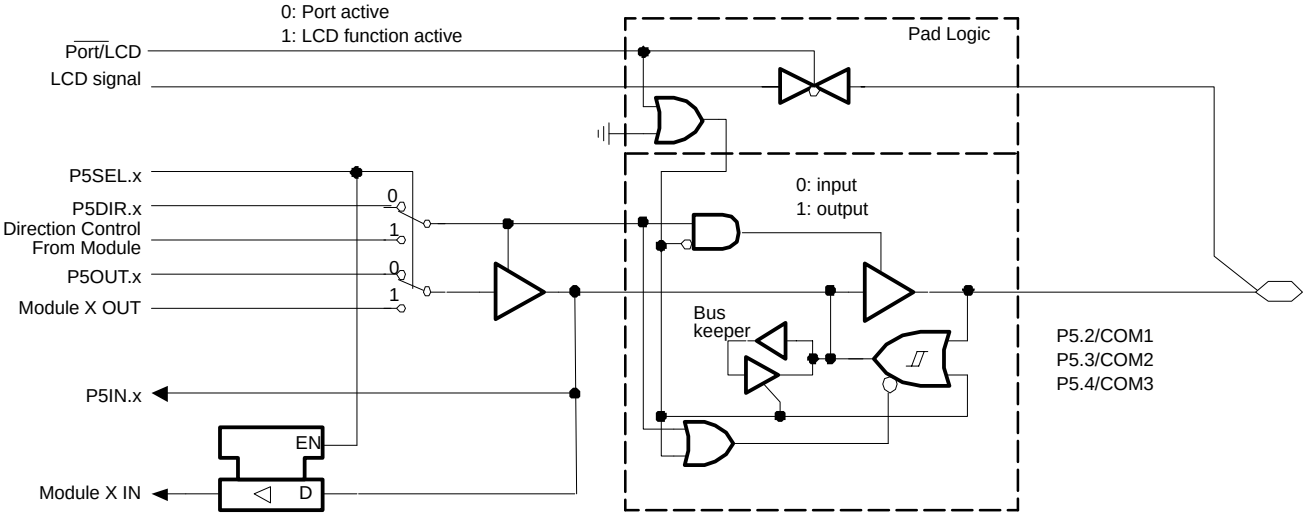


Note: $0 \le x \le 1$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	Segment	Port/LCD
P5Sel.0	P5DIR.0	P5DIR.0	P5OUT.0	DVSS	P5IN.0	unused	S1	0: LCDM<20h
P5Sel.1	P5DIR.1	P5DIR.1	P5OUT.1	DVSS	P5IN.1	unused	S0	0: LCDM<20h

input/output schematic (continued)

port P5, P5.2 to P5.4, input/output with Schmitt-trigger

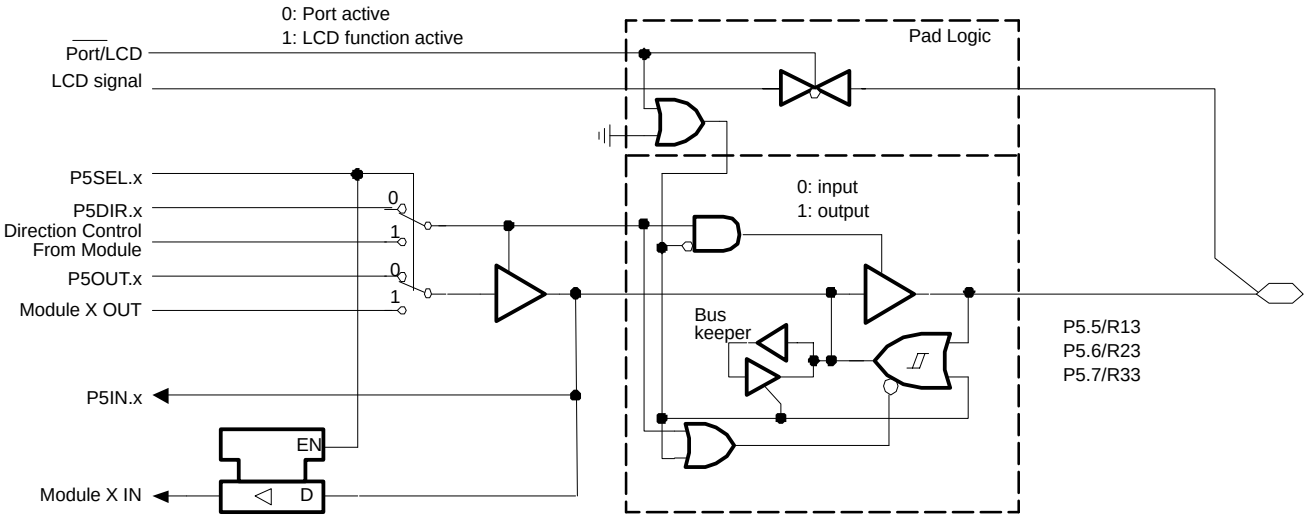


Note: $2 \le x \le 4$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	LCD signal	$\overline{\text{Port}}$/LCD
P5Sel.2	P5DIR.2	P5DIR.2	P5OUT.2	DVSS	P5IN.2	unused	COM1	P5SEL.2
P5Sel.3	P5DIR.3	P5DIR.3	P5OUT.3	DVSS	P5IN.3	unused	COM2	P5SEL.3
P5Sel.4	P5DIR.4	P5DIR.4	P5OUT.4	DVSS	P5IN.4	unused	COM3	P5SEL.4

input/output schematic (continued)

port P5, P5.5 to P5.7, input/output with Schmitt-trigger

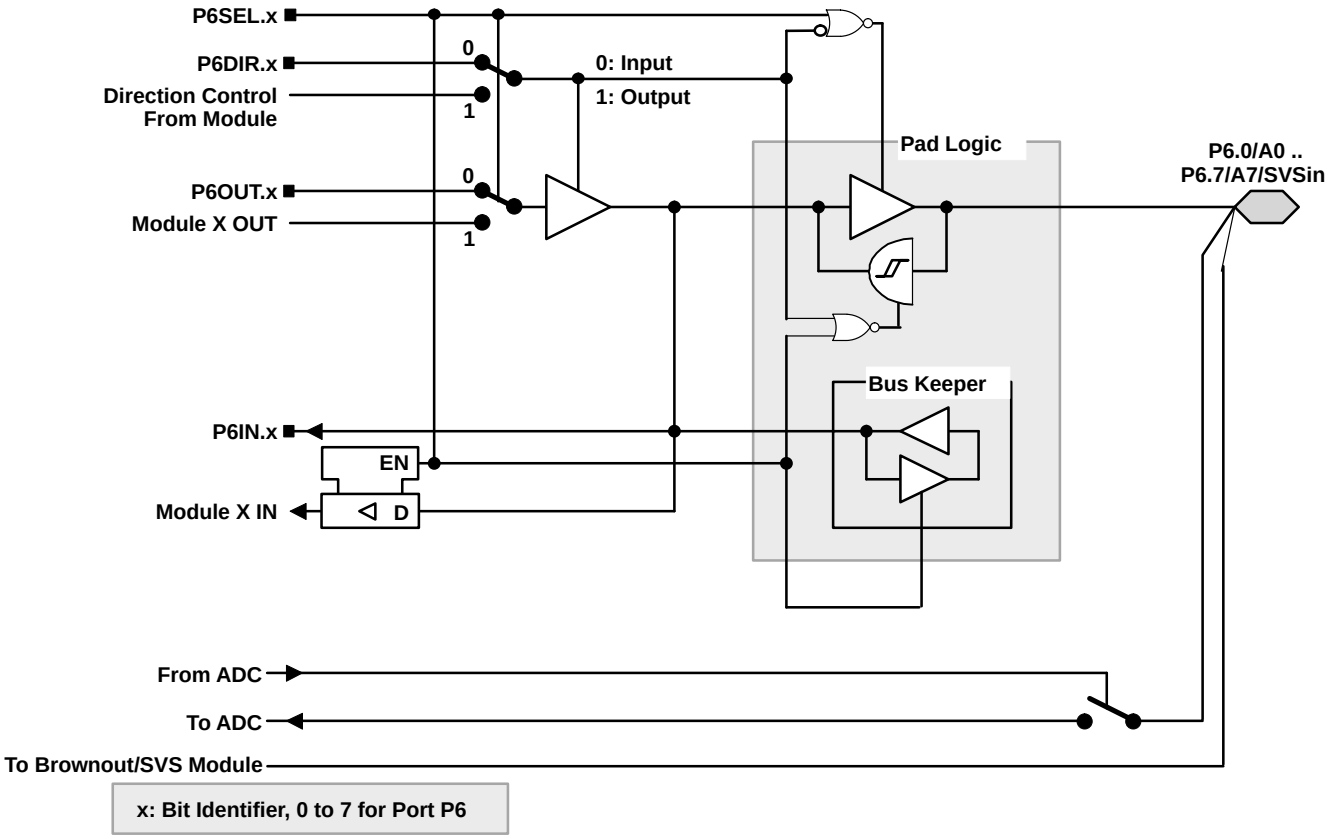


Note: $5 \le x \le 7$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	LCD signal	Port/LCD
P5Sel.5	P5DIR.5	P5DIR.5	P5OUT.5	DVSS	P5IN.5	unused	R13	P5SEL.5
P5Sel.6	P5DIR.6	P5DIR.6	P5OUT.6	DVSS	P5IN.6	unused	R23	P5SEL.6
P5Sel.7	P5DIR.7	P5DIR.7	P5OUT.7	DVSS	P5IN.7	unused	R33	P5SEL.7

input/output schematic (continued)

port P6, P6.0 to P6.7, input/output with Schmitt-trigger



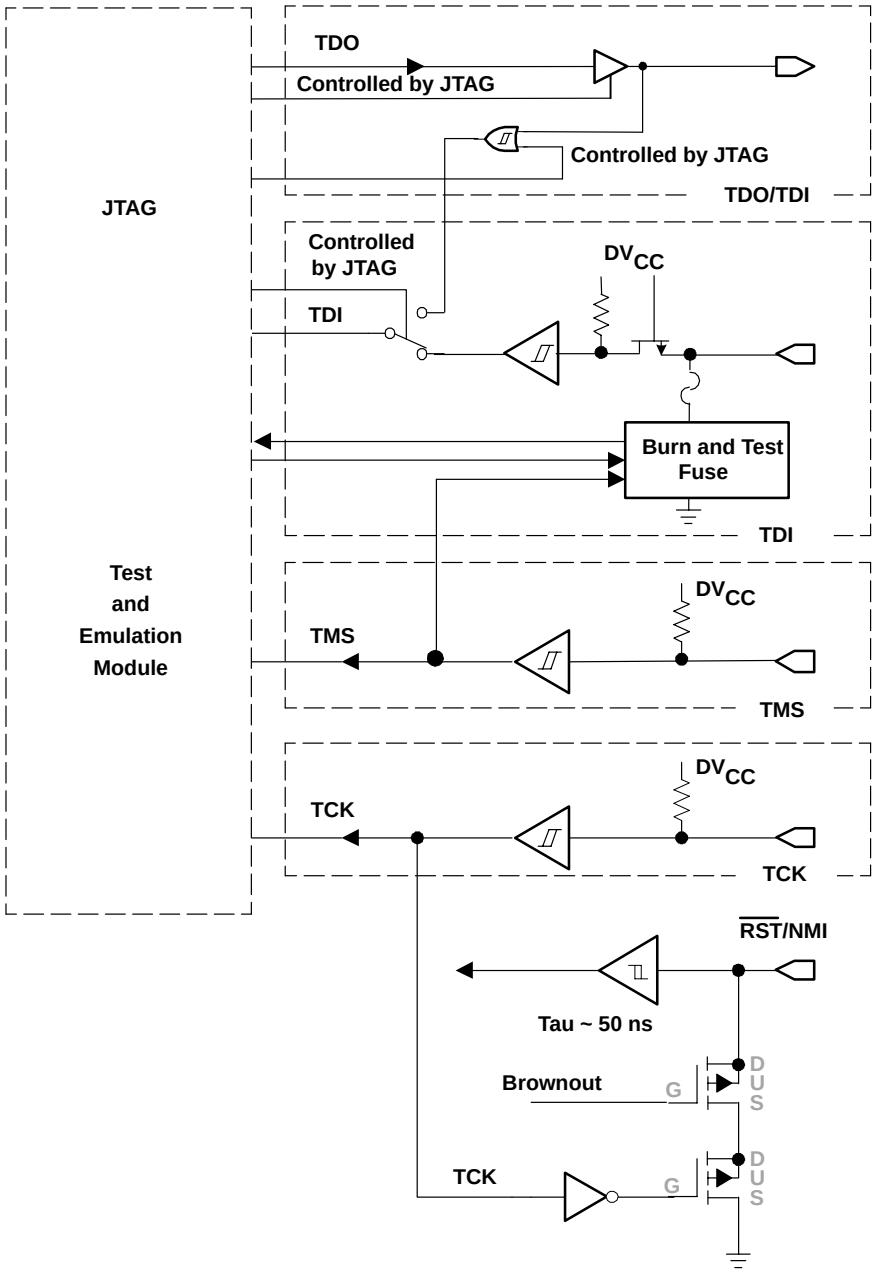
NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1←0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 μA.
Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, even if the signal at the pin is not being used by the ADC12.

PnSel.x	PnDIR.x	Dir. Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV_{SS}	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV_{SS}	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV_{SS}	P6IN.2	unused
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DV_{SS}	P6IN.3	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV_{SS}	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV_{SS}	P6IN.5	unused
P6Sel.6	P6DIR.6	P6DIR.6	P6OUT.6	DV_{SS}	P6IN.6	unused
P6Sel.7	P6DIR.7	P6DIR.7	P6OUT.7	DV_{SS}	P6IN.7	unused

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.
The signal at pin P6.7/A7/SVSin is also connected to the input multiplexer in the module brownout/supply voltage supervisor.

input/output schematic (continued)

JTAG pins TMS, TCK, TDI, TDO/TDI, input/output with Schmitt-trigger or output



JTAG fuse check mode

MSP430 devices that have the fuse on the TDI terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ($I_{(TF)}$) of 1 mA at 3 V can flow from the TDI pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 27). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

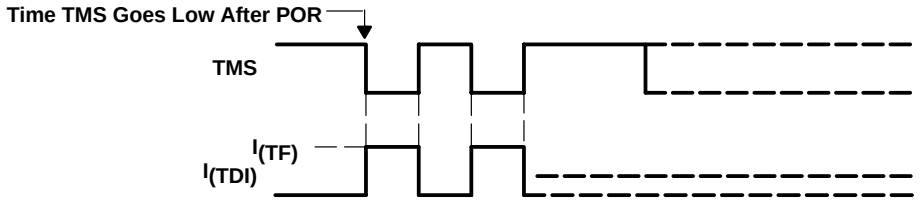
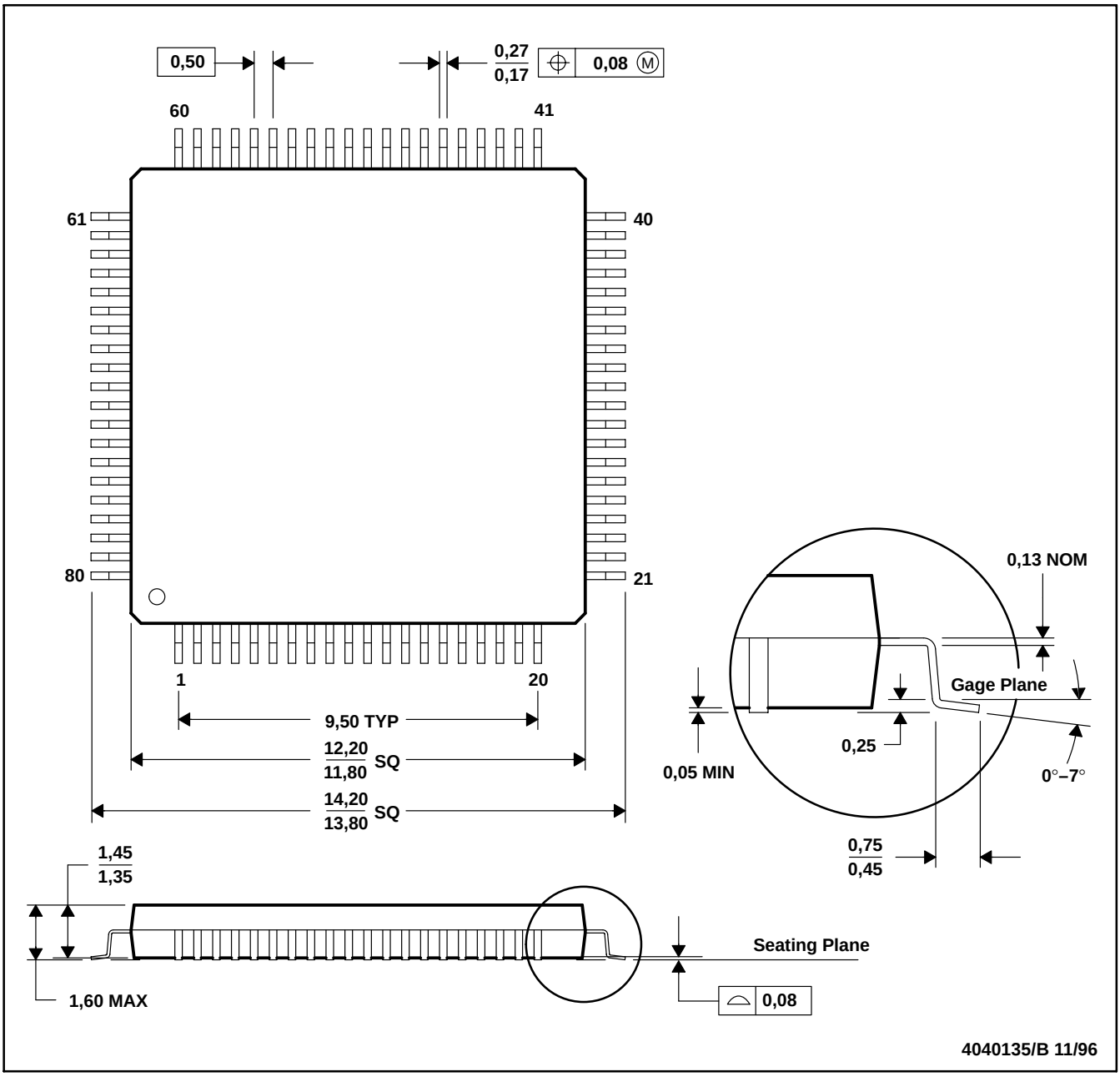


Figure 27. Fuse Check Mode Current MSP430x43x, MSP430x44x

MECHANICAL DATA

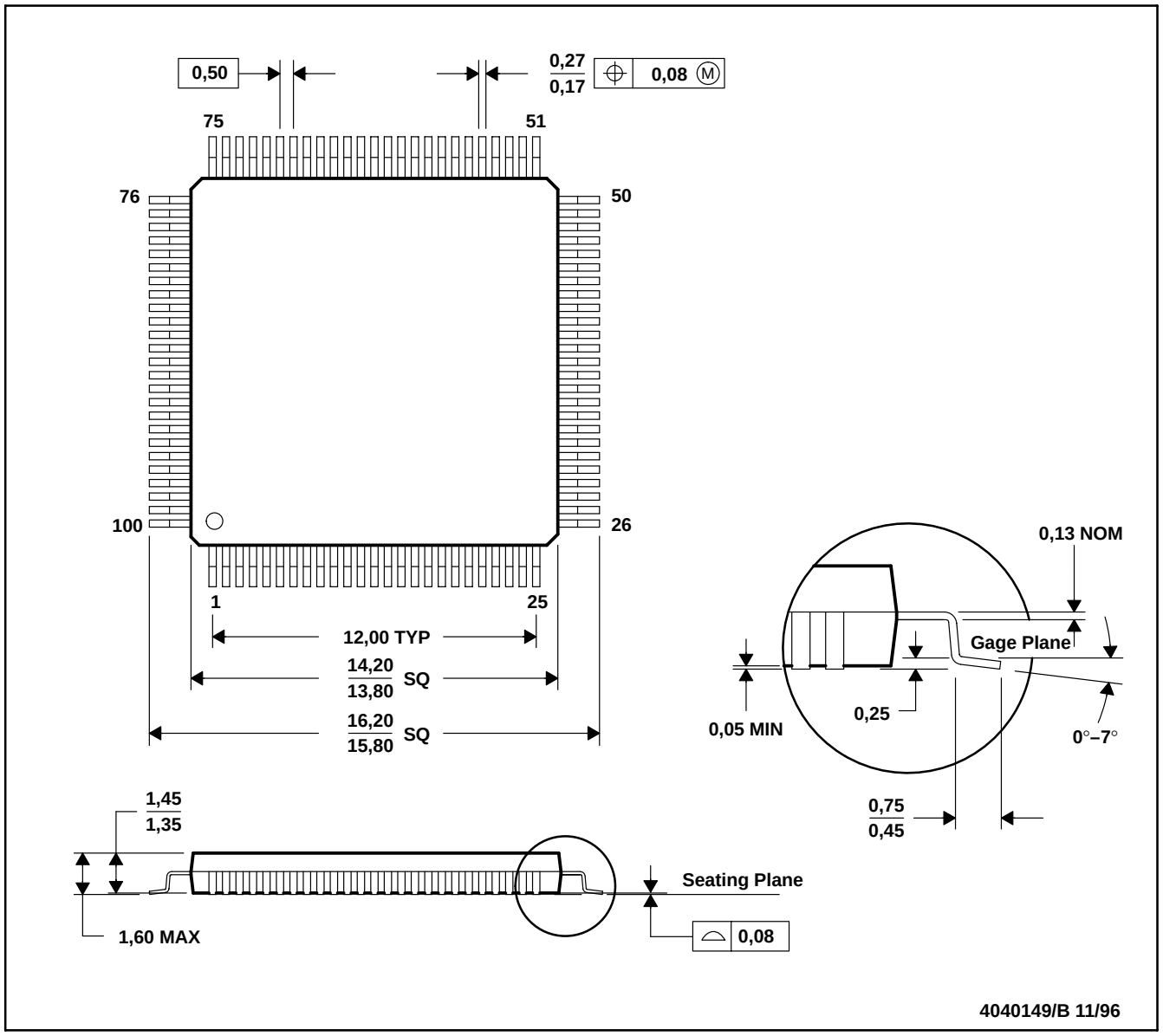
PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

MECHANICAL DATA

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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