FUJI Power Supply Control IC

Power Factor Correction

FA5502P/M

Application Note

June `02
Fuji Electric Co., Ltd.
Matsumoto Factory

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Note

• Parts tolerance and characteristics are not defined in all application described in this Data book. When design an actual circuit for a product, you must determine parts tolerances and characteristics for safe and economical operation.

1. Description

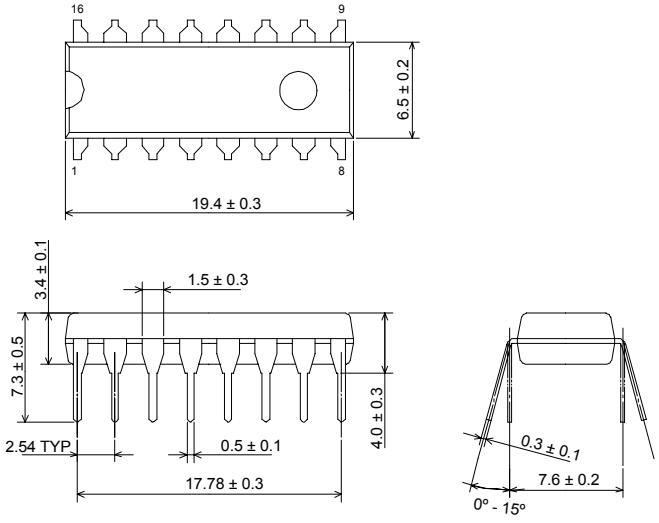
FA5502P/M is a control IC for a power factor correction system. This IC uses a CMOS device with high dielectric strength (30V) to implement low power consumption. This IC uses the average current control system to ensure stable operation. With this system, a power factor of 99% or better can be achieved.

2. Features

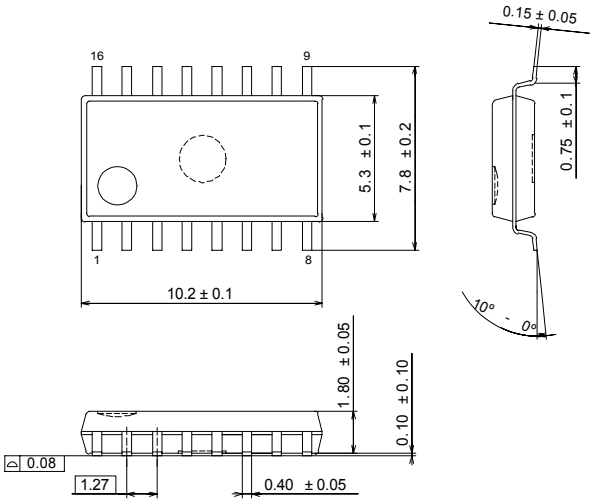
- Low current consumption by CMOS process
- Stand-by : 3μA(max), Start-up : 30μA(max), Operating : 4mA(typ)
- Good regulation of PFC output voltage from no-load to full-load
- Drive circuit for connecting a power MOSFET(I_{OUT} = ±1.5A)
- Pulse-by-pulse overcurrent and overvoltage limiting function
- ±2% accuracy reference voltage for setting DC output and overvoltage protection
- Output ON/OFF control function by external signal
- External synchronizing input pin for synchronous operation with other circuits
- Undervoltage lockout function (ON:16.5V, OFF:8.9V)
- 16-pin package (DIP/SOP)

3. Outline

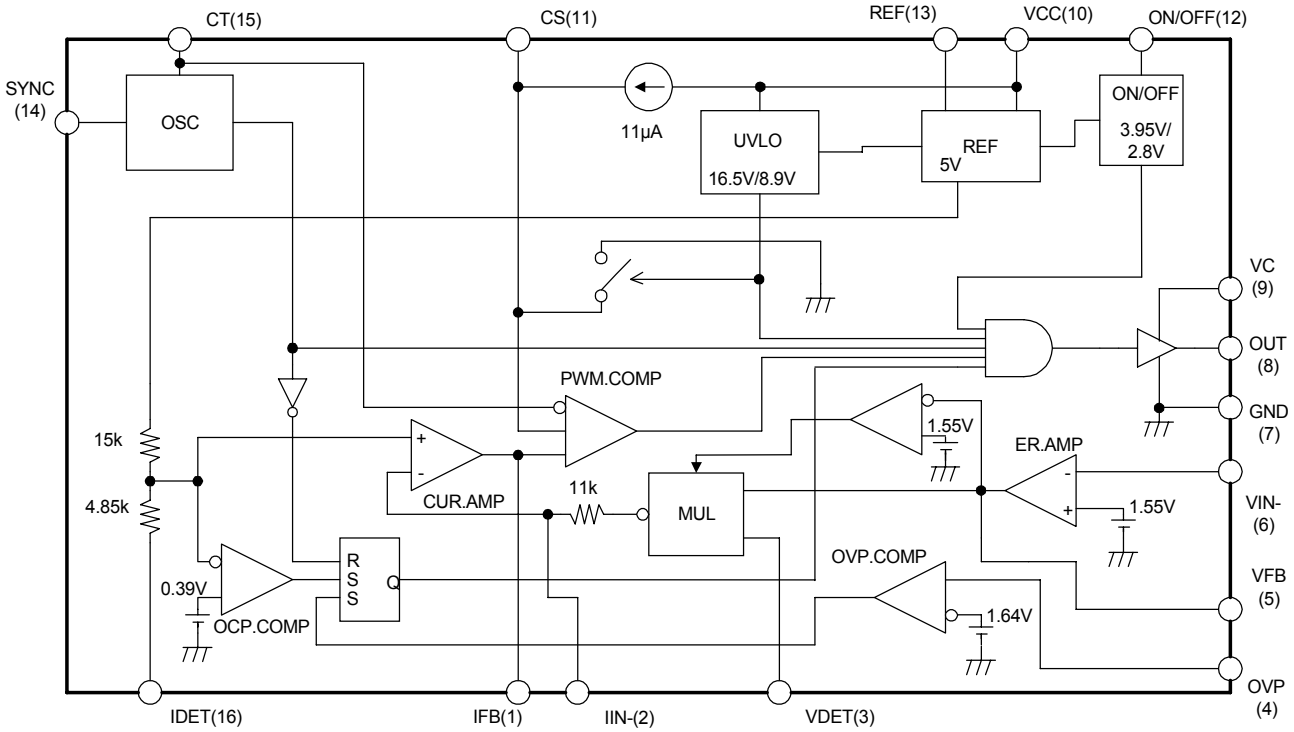
DIP-16 (FA5502P)



SOP-16 (FA5502M)



4. Block diagram



5. Pin assignment

Pin No.	Symbol	Function	Description
1	IFB	Current error amplifier output	Output of current error amplifier to connect compensation network
2	IIN-	Inverting input to current error amplifier	Inverting input of current error amplifier to connect compensation network
3	VDET	Multiplier input	Input of multiplier to detect sinusoidal waveform
4	OVP	Overvoltage protection input	Input to overvoltage protection circuit
5	VFB	Voltage error amplifier output	Output of voltage error amplifier to connect compensation network
6	VIN-	Inverting input to voltage error amplifier	Inverting input to voltage error amplifier to detect PFC output voltage
7	GND	Ground	Ground
8	OUT	Output	Output for direct driving a power MOSFET
9	VC	Power supply to output circuit	Power supply to output circuit
10	VCC	Power Supply	Power supply for IC
11	CS	Soft-start	A pin to connect a capacitor for soft-start
12	ON/OFF	Output ON/OFF control input	Input of ON/OFF control circuit
13	REF	Reference voltage	Reference voltage output
14	SYNC	Oscillator synchronization input	Input of synchronization signal
15	CT	Oscillator timing capacitor and resistor	A pin to connect timing capacitor and resistor to set oscillation frequency
16	IDET	Non-inverting input to current error amplifier	Input of inductor current signal

6. Ratings and characteristics

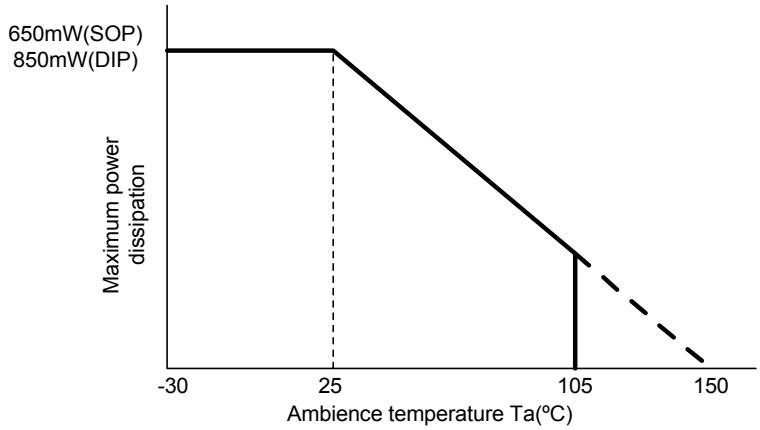
The contents are subject to change without notice. When using a product, be sure to obtain the latest specifications.

(1) Absolute maximum ratings

Item			Symbol	Rating	Unit
Supply Voltage	VC pin		V_C	Vcc	V
	VCC pin Low impedance source (Icc>15mA)		V_{CC1}	30	V
	VCC pin Internal zener clamp voltage (Icc<15mA)		V_{CC2}	Self Limiting	V
Output peak current			I_{OUT}	±1.5	A
SYNC,VIN-,VDET and OVP pins Input voltage			V_{SYNC} V_{VIN-} V_{VDET} V_{OVP}	-0.3 to 5.0	V
IDET pin input voltage			V_{IDET}	-10 to 5.0	V
ON/OFF pin input voltage			$V_{ON/OFF}$	-0.3 to Vcc	V
REF pin source current			I_{REF}	-10	mA
Power dissipation (Ta=25ºC)		DIP-16	Pd	850	mW
		SOP-16		650	mW
Ambiance temperature			Ta	-30 to +105	°C
Maximum junction temperature			Tj	+150	°C
Storage temperature			Tstg	-40 to +150	°C

Note) VC and ON/OFF pins voltage must be less than or equal to VCC pin voltage in all the conditions.
Peak current at OUT pin may flow to rated value neither according to supply voltage nor temperature conditions.

Maximum dissipation curve



(2) Recommended operating conditions

Item	Symbol	MIN	TYP.	MAX	Unit
Supply voltage	Vcc,Vc	10		28	V
IDET pin input voltage	V_{IDET}	-1.0		0	V
VDET pin input voltage	V_{VDET}	0		2.4	V
VDET pin peak input voltage	V_{PVDET}	0.65		2.4	V
Oscillation frequency	f_{OSC}	15		150	kHz
Oscillation timing capacitance	C_T	330		1000	pF
Oscillation timing resistance	R_T	10		75	kΩ
Noise filter resistance connected to IDET pin	Rn	0		27	Ω
REF-GND capacitance	Cref	0.1	0.47		µF

Note) If the synchronous operation is not necessary, connect the SYNC pin to GND.

(3) Electrical Characteristics (Unless otherwise specified, Vcc=Vc=18V, Ta=25°C, C_T=470pF, R_T=22kΩ)

Reference voltage section (REF pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Output voltage	V_{REF}		4.8	5	5.2	V
Line regulation	Vrdv	Vcc=10 to 28V			±25	mV
Load regulation	Vrdi	I_{Load}=0.1 to 2mA	-50	-25		mV
Temperature stability	Vrd$_T$	Ta=-30 to 105°C		±0.5		mV/°C

Oscillator section (CT, SYNC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Oscillation frequency	f_{OSC}	C_T=470pF, R_T=22kΩ, Ta=25°C	71	78	85	kHz
Voltage stability	fdv	Vcc=10 to 28V		±1	±3	%
Temperature stability	fd$_T$	Ta=-30 to +105°C		±0.04	±0.07	%/°C
Output peak voltage	V_{OSC}			3.4		V
Synchronizing input threshold voltage	V_{THSYNC}	SYNC pin voltage	1.0	1.5	2.0	V
SYNC pin input current	I_{SYNC}	SYNC pin=2V	75	125	175	µA

Pulse width modulation circuit section (OUT pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Maximum duty cycle	D_{MAX}		91	94	97	%

Overcurrent limiter circuit section (IDET pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Input threshold voltage	V_{THOCP}	IDET pin voltage	-1.20	-1.10	-1.00	V
Delay time	Tpd$_{OCP}$			150		ns

Soft start circuit section (CS pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Charge current	I_{CHG}	CS pin=0V		-11		µA
Input threshold voltage	V_{THCS0}	Dutycycle=0%		0.34		V
	V_{THCSM}	Dutycycle=D_{MAX}		3.40		V

Output ON/OFF control circuit section (ON/OFF pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
On-state input current	I_{THON}	ON/OFF pin=V_{THON}			±500	nA
ON/OFF control threshold voltage	V_{THON}	OFF→ON	3.55	3.95	4.35	V
	V_{THOFF}	ON→OFF	2.40	2.80	3.20	V

Voltage error amplifier section (VIN-, VFB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Reference voltage	Vr		1.519	1.550	1.581	V
Line regulation	Vredv	Vcc=10 to 28V		±0.5		mV
Temperature stability	Vred$_T$	Ta=-30 to 105°C		±0.2		mV/°C
Input bias current	I_{BE}				±500	nA
Open loop gain	Ave		60			dB
Output voltage	V_{OE+}	No load	3.7	4.1		V
	V_{OE-}	No load		50	200	mV
Output source current	I_{OE+}	VFB pin=0V		-2.8		mA
Output sink current	I_{OE-}	VFB pin=2V		280		µA

Current error amplifier section (IIN-, IFB, IDET pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Input threshold voltage	V_{THIDET}	VDET pin=0V VFB pin=Vr Rn=30Ω	-50	0	50	mV
Input bias current	I_{BC}	IDET pin=0V	-350	-250	-150	μA
Open loop gain	Avc		60			dB
Output voltage	V_{OC+}	No load	3.55	3.8		V
	V_{OC-}	No load		50	200	mV
Output source current	I_{OC+}	IFB pin=0V		-5.1		mA
Output sink current	I_{OC-}	IFB pin=2V		800		μA

Multiplier section (VDET, IIN-, VFB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
VDET pin input voltage	V_{MVDET}		0		2.4	V
VFB pin input voltage	V_{MVFB}		1.5		3.5	V
Input bias current	I_{BVDET}	VDET pin=0V	-1.5	-0.5		μA
Output current	I_M	IIN- pin=0V		-44		μA
Output voltage factor	K			-1.2		-

Overvoltage protection circuit section (OVP pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Input threshold voltage	V_{THOVP}	OVP pin voltage	1.607	1.640	1.673	V
VTHOVP/Vr ratio	α		1.037	1.058	1.079	-
Input bias current	I_{BOVP}	OVP pin=0V	-1.0	-0.3		μA
Delay time	Tpdovp			150		ns

Undervoltage lockout circuit section (VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Start-up threshold voltage	V_{THUON}		15.5	16.5	17.5	V
Shutdown threshold voltage	V_{THUOFF}		8.2	8.9	9.6	V
Hysteresis voltage	V_{UHYS}		6.8	7.6	8.4	V

Output circuit section (OUT, VC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Low output voltage	V_{OL}	I_{OL}=100mA		0.5	1.0	V
High output voltage	V_{OH}	I_{OH}=-100mA, Vcc=18V	15.5	16.5		V
Rise time	tr	No load		50		ns
Fall time	tf	No load		50		ns

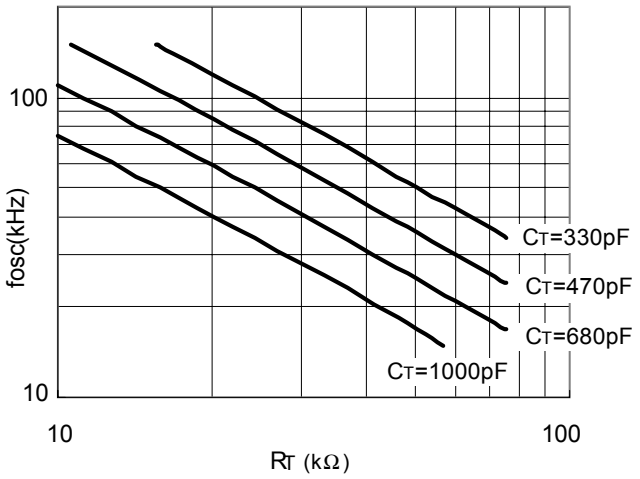
Power supply current (VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Stand-by current	I_{CCST}	Vcc=14V			3	μA
Starting-up current	I_{CCSTA}	Vcc=start threshold		10	30	μA
Operating-state supply current	I_{CCOP}	No load		4	6	mA
OFF-state supply current	I_{CCOFF}	ON/OFF pin=0V		80	200	μA

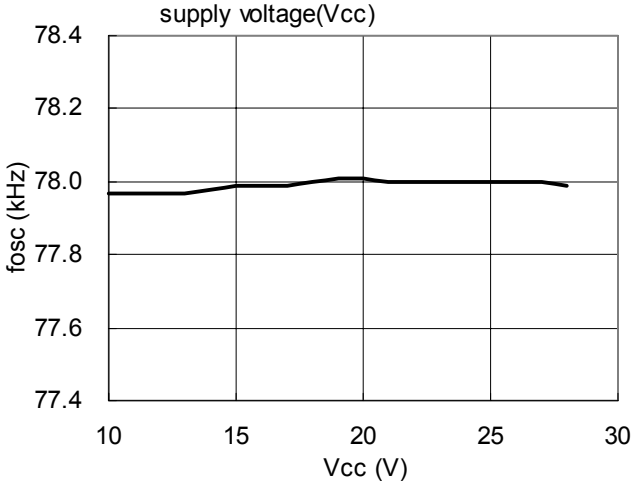
7. Characteristic curves

(Unless otherwise specified, Vcc=Vc=18V, Ta=25°C, C_T=470pF, R_T=22kΩ)

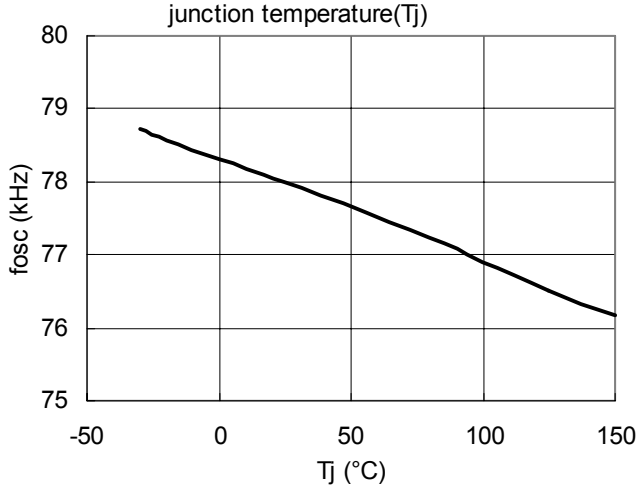
Oscillation frequency (fosc) vs. timing resistor (R_T)



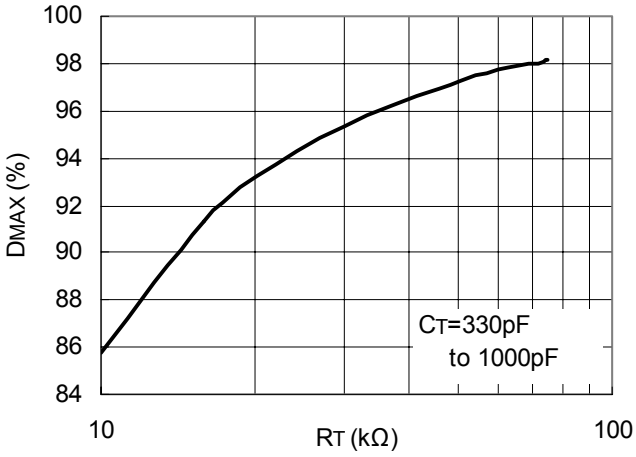
Oscillation frequency(fosc) vs. supply voltage(Vcc)



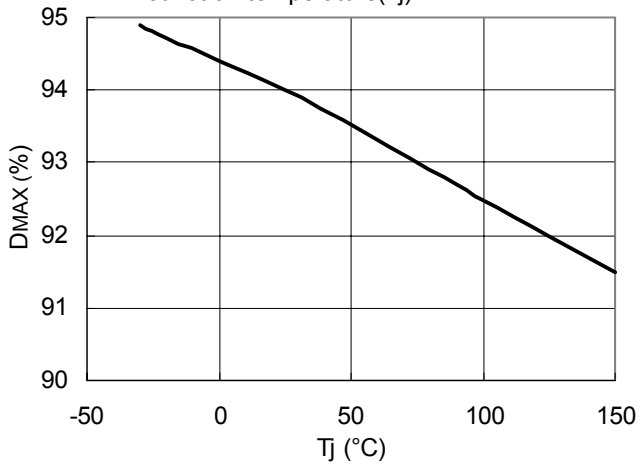
Oscillation frequency(fosc) vs. junction temperature(Tj)



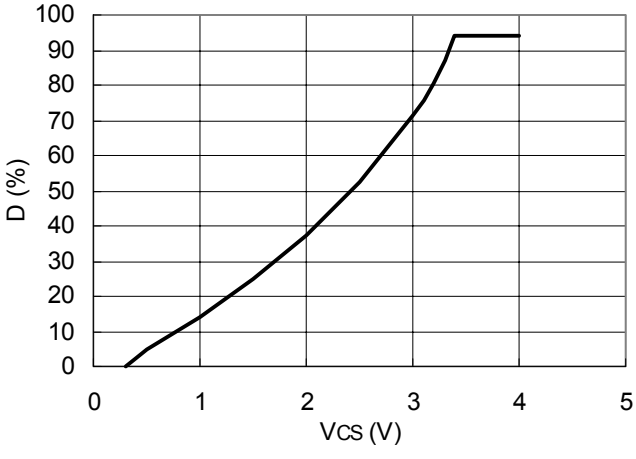
Maximum duty cycle(D_{MAX}) vs. timing resistor(R_T)



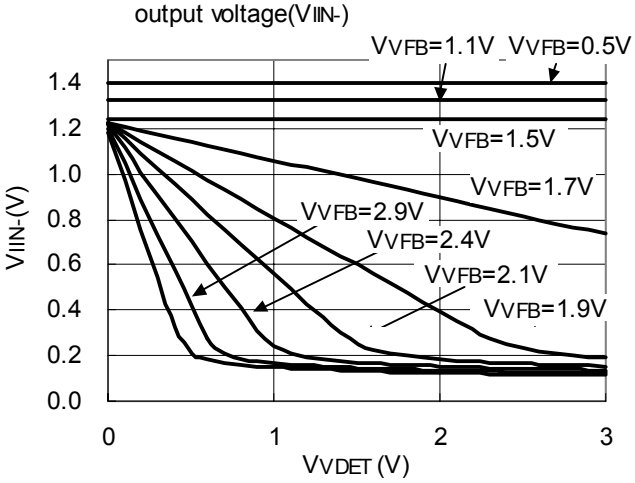
Maximum duty cycle(D_{MAX}) vs. Junction temperature(Tj)



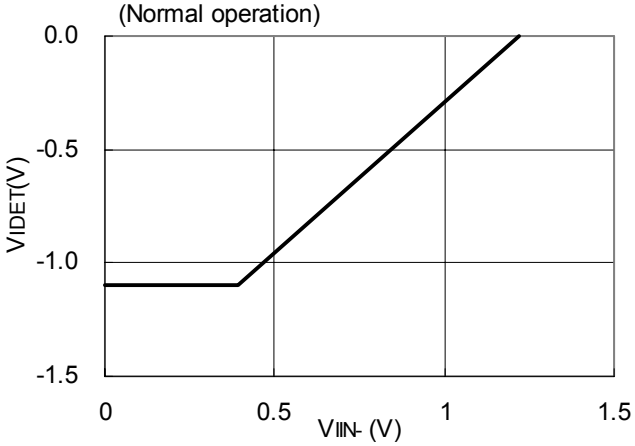
Output duty cycle(D) vs. CS pin voltage(V_{CS})



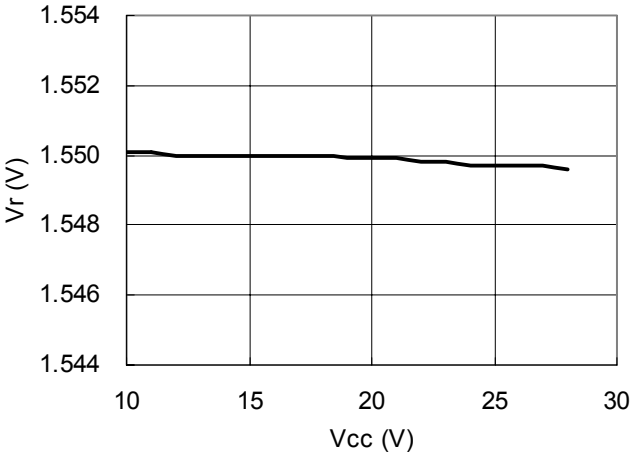
Multiplier input voltage(V_{VDET}) vs.
output voltage(V_{IIN-})



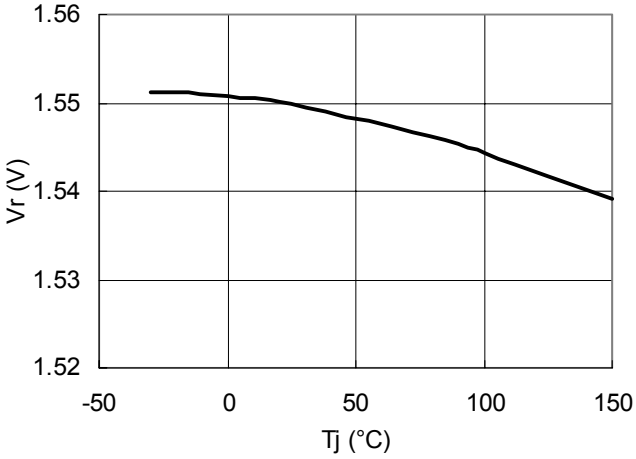
IDET pin voltage(V_{IDET}) vs.
IIN- pin voltage(V_{IIN-})
(Normal operation)



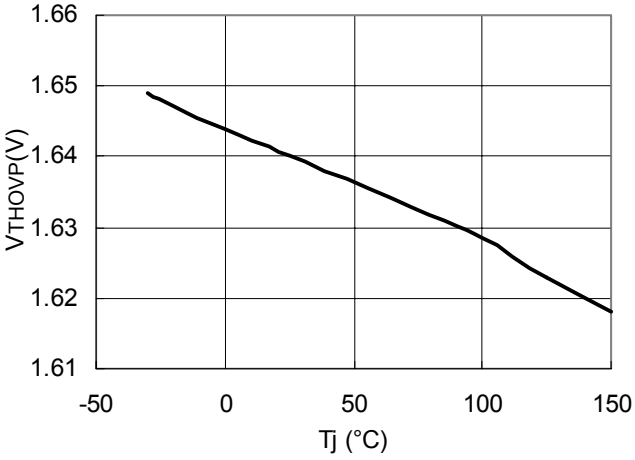
Voltage error amplifier
reference voltage(Vr) vs. supply voltage(Vcc)



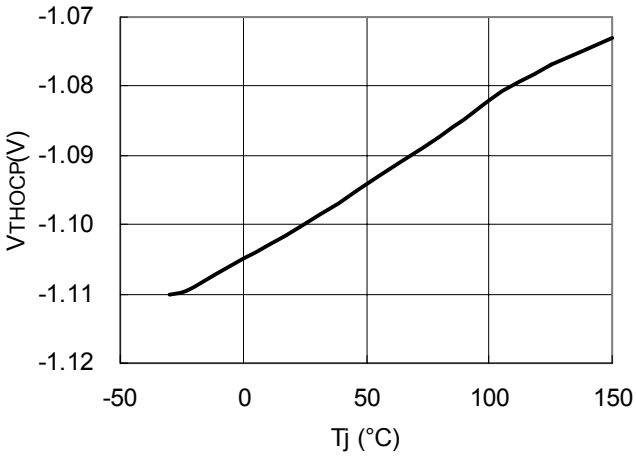
Voltage error amplifier
reference voltage(Vr) vs. junction temperature(Tj)



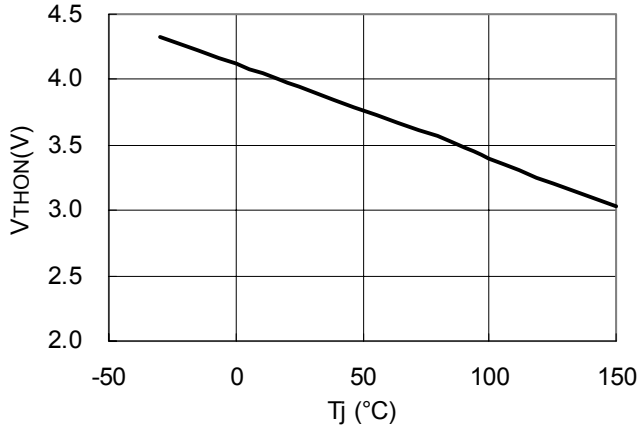
OVP input threshold voltage(V_{THOVP}) vs.
junction temperature(Tj)



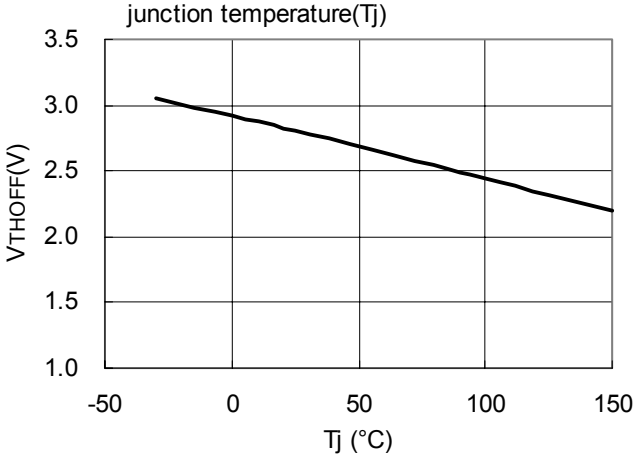
OCP input threshold voltage(V_{THOCP}) vs.
junction temperature(Tj)



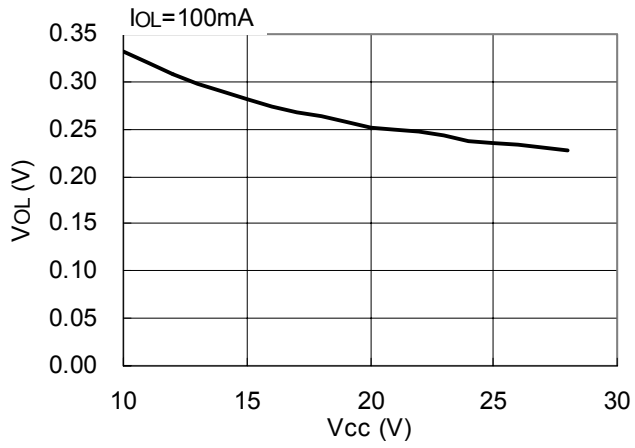
ON/OFF control circuit
ON threshold voltage(V_{THON}) vs.
junction temperature(Tj)



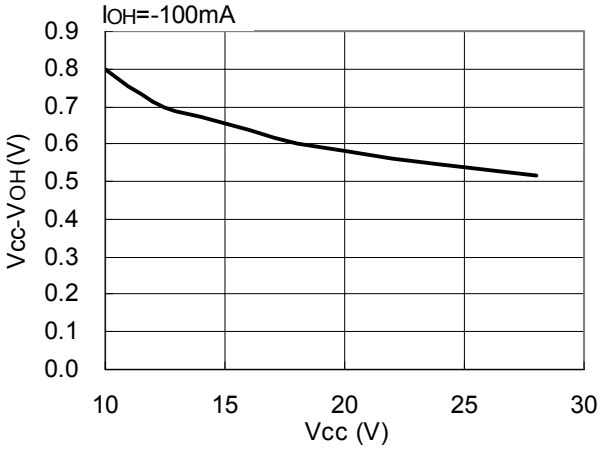
ON/OFF control circuit
OFF threshold voltage(V_{THOFF}) vs.
junction temperature(Tj)



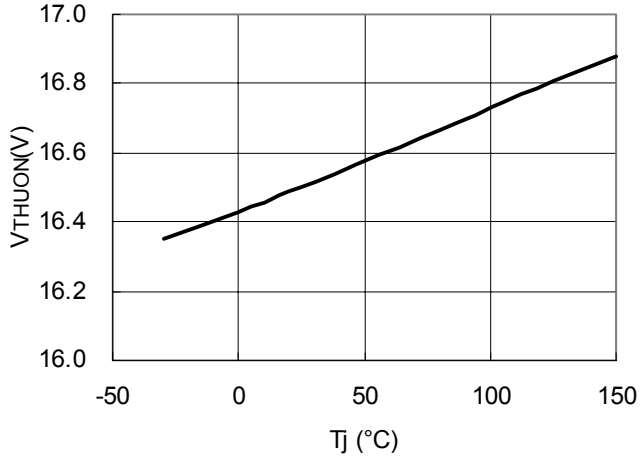
L-level output voltage(V_{OL}) vs.
supply voltage(Vcc)



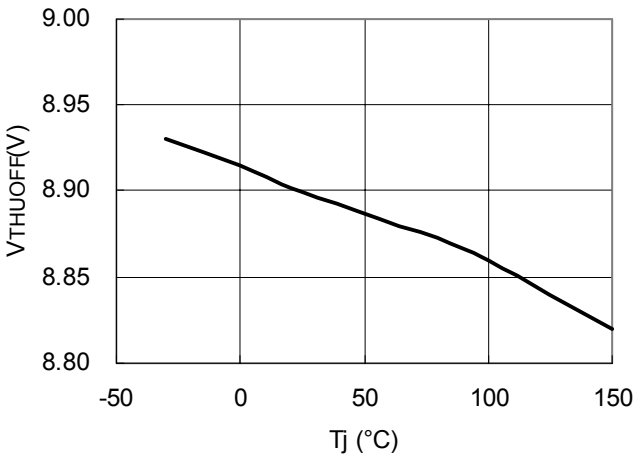
H-level output voltage(V_{OH}) vs.
supply voltage(Vcc)



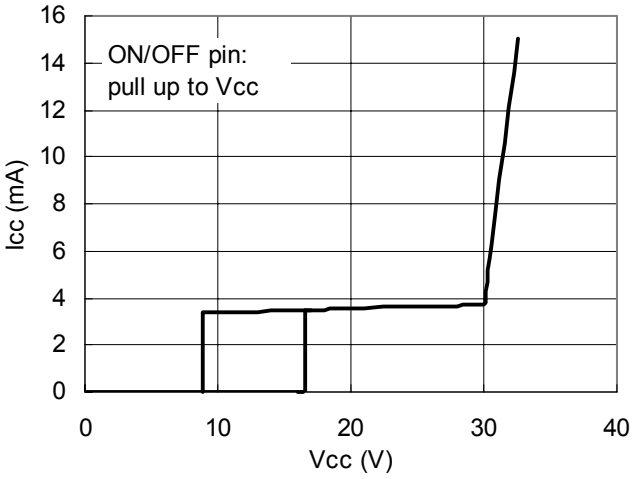
UVLO startup threshold voltage(V_{THUON}) vs.
junction temperature(Tj)



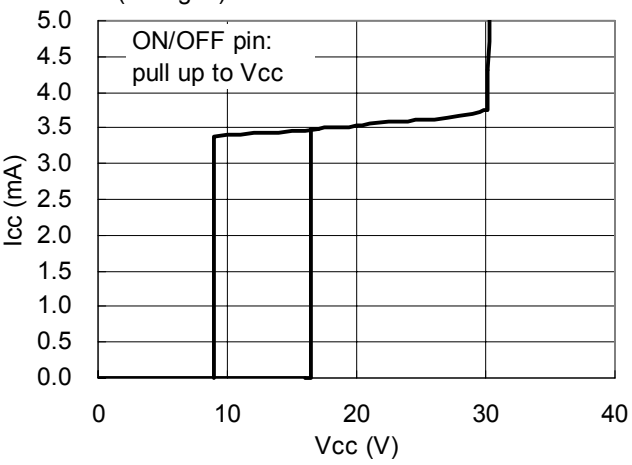
UVLO shutdown threshold voltage(V_{THUOFF}) vs.
junction temperature(Tj)



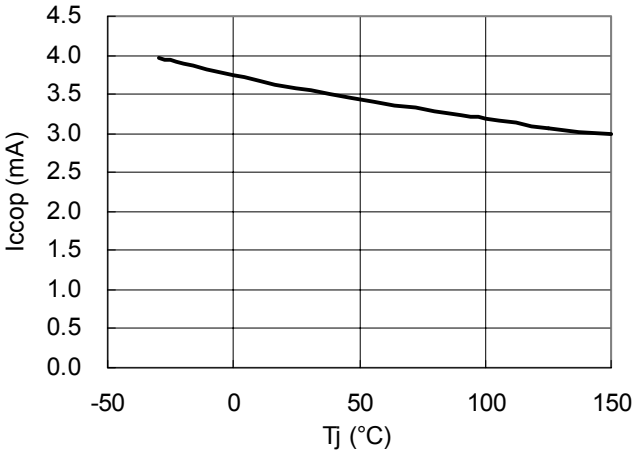
Supply current(Icc) vs. supply voltage(Vcc)



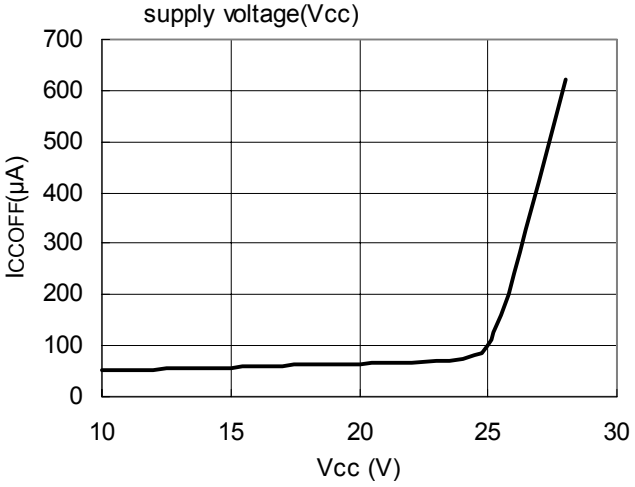
Supply current(Icc) vs. supply voltage(Vcc) (enlarged)



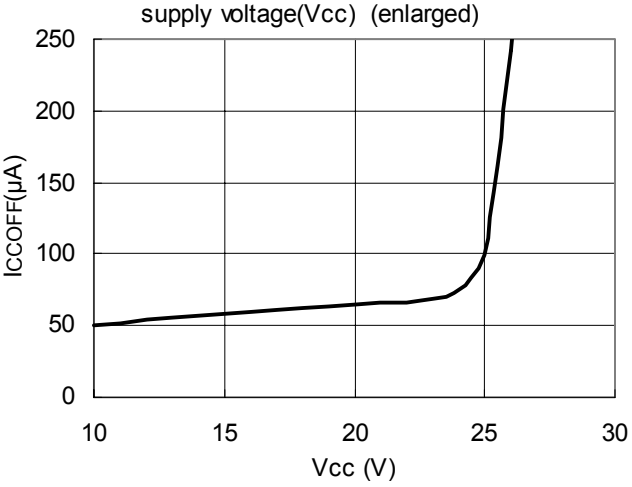
Operating-state supply current(Iccop) vs. junction temperature(Tj)



OFF-state supply current(I_{CCOFF}) vs. supply voltage(Vcc)



OFF-state supply current(I_{CCOFF}) vs. supply voltage(Vcc) (enlarged)



8. Description of each circuit

(1) Oscillator section

The oscillator generates sawtooth waveform between 0.3V and 3.4V by charging and discharging capacitor. Fig.1 shows the connection. The oscillation frequency is determined by CT and RT.
(see characteristics curve).

The oscillator waveform is input to the PWM comparator. The oscillator is also used for determining the maximum duty cycle of output pulses. Concretely, a signal is sent to the output circuit section and the OUT pin is forced to be Low level during the CT discharge period (fall time of CT pin voltage).

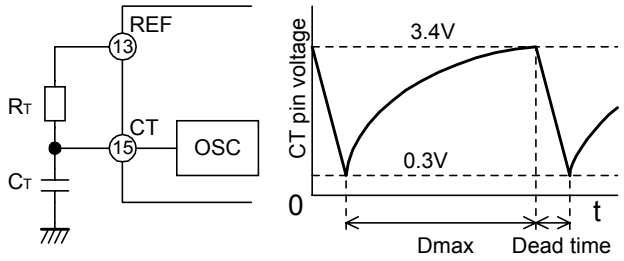


Fig.1 Oscillator circuit

SYNC pin (pin 14) is a synchronizing signal input pin. It is usable for synchronized operation. When it is desired to adopt synchronized operation, the free-running frequency (determined by CT and RT) must be set about 10% lower than that of external synchronizing signal.

The input resistance in SYNC pin is approximately 16kΩ. Usually, a square-wave synchronizing signal is differentiated by R and C, and the voltage input to SYNC pin is so arranged to be below 1V within CT discharge period. Concretely, the waveform must satisfy the condition in Fig.3.

Depending on the amplitude, etc. of square-wave signal used as external synchronizing signal, the RC differentiating circuit shown in Fig.2 could not generate a waveform in Fig.3. In such a case, add a resistor between SYNC pin and GND so as to clear the condition in Fig.3.

Fig.5 shows timing chart of synchronized operation.

Note that diode D2 in Fig.2 is required so that no negative voltage will be applied to SYNC pin while in the discharge period of capacitor Csy in the differentiating circuit. Considering the rated voltage of SYNC pin, use a Schottky diode of a low forward voltage.

Unless the external synchronization function is used, connect SYNC pin to GND pin to avoid a malfunction.

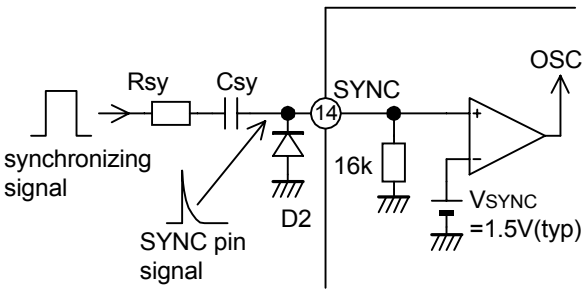


Fig.2 SYNC pin circuit (1)

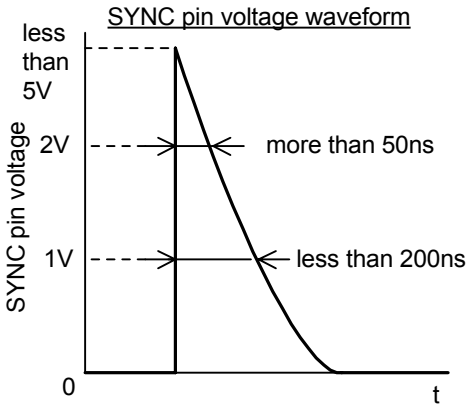


Fig.3 Condition for SYNC pin signal

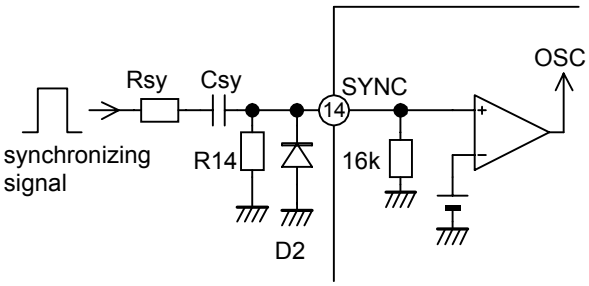


Fig.4 SYNC pin circuit (2)

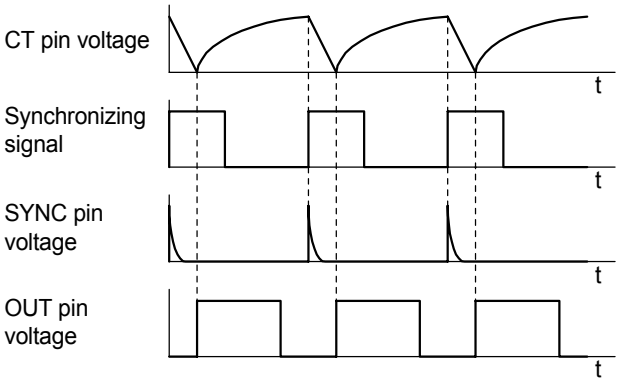


Fig.5 Timing chart of synchronized operation

(2) Voltage error amplifier and overvoltage limiting circuit

ER.AMP is an error amplifier which constitutes a voltage feedback loop for keeping the output voltage constant. The non-inverting input is internally connected to reference voltage Vr of 1.55V (typ.). Fig.6 shows the connection. The output voltage is determined by:

$$V_O = \frac{R1+R2}{R1} \times Vr \quad \cdots\cdots (1)$$

The error amplifier output is pinned out at VFB pin (pin 5). Between VFB pin and VIN- pin, RC network are connected for loop compensation. The voltage gain Av is expressed by

$$A_V = \frac{R4}{R3(1+j\omega C1 \times R4)} \quad \cdots\cdots (2)$$

Cutoff frequency fc is expressed by:

$$f_C = \frac{1}{2\pi C1 \times R4} \quad \cdots\cdots (3)$$

If 100Hz or 120Hz ripples appear at the error amplifier output, the PFC converter will not operate stably. Therefore, determine C1 and R4 so that voltage gain Av at 100 Hz or 120 Hz will be small enough. Also set fc to approximately 1Hz to ensure a stable operation. Practically, the optimum value should be determined by evaluation in the actual circuit.

To limit the output voltage when it has risen above the normal voltage, overvoltage limiting comparator OVP.COMP is incorporated. Its threshold voltage Vp is as follows:

$$V_P = \alpha \times Vr \quad (\alpha=1.058(typ)) \cdots\cdots (4)$$

According to the connection in Fig.6, therefore, the output overvoltage is limited to 1.058 times (typ.) the normal output voltage.

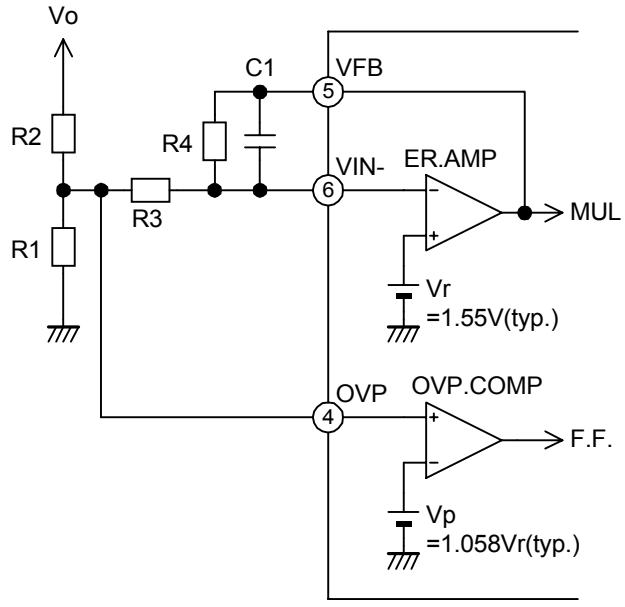


Fig.6 Voltage error amplifier and overvoltage limiting circuit

(3) Current error amplifier and overcurrent limiter circuit

CUR.AMP is an error amplifier which constitutes a current loop to control the line current to a sinusoidal waveform. As shown in Fig.7, to IIN- pin (pin 2), a multiplier output is connected via resistor RA as a current reference signal. Inductor current is monitored by IDET pin (pin 16). The IDET pin should be used within the voltage range from 0V to –1.0V in normal operation. RC network for loop compensation is connected between IFB pin and IIN- pin. According to the circuit in Fig.7, the characteristics of voltage gain AV are as shown in Fig.8. Where,

$$Z = \frac{1}{2\pi R5 \times C3} \quad \cdots\cdots (5)$$

$$P = \frac{1}{2\pi R5 \times C} \qquad C = \frac{C2 \times C3}{C2 + C3} \quad \cdots\cdots (6)$$

Voltage gain (G1) between Z and P (gain between IDET pin and IFB pin) in Fig.8 is:

$$G1 = 20\log\left(0.75\left(\frac{R5}{RA}+1\right)\right) \quad \cdots\cdots (7)$$

Select C2 and C3 so that P/Z will be about 10 for adequate phase margin. The output of current error amplifier is input to PWM comparator.
The optimum value of loop compensation should be determined by evaluation in actual circuit referring to application circuit, etc.

To limit the overcurrent, overcurrent limiting comparator OCP.COMP is provided. The threshold voltage at IDET pin is -1.10V (typ.). If a noise is picked up at IDET pin, suppress it by connecting Rn and Cn. Rn must be lower than 27 Ω.

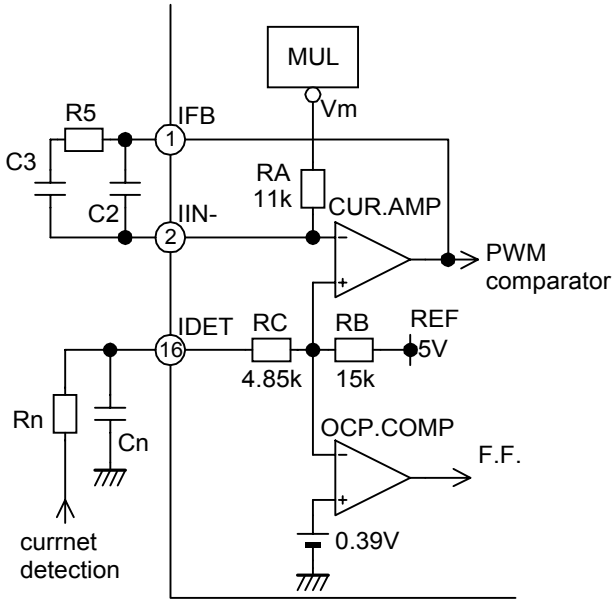


Fig.7 Current error amplifier and overcurrent limiting circuit

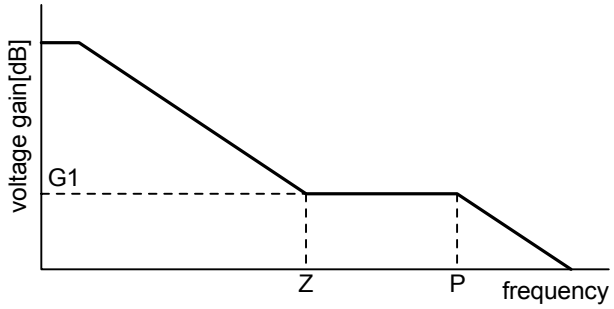


Fig.8 Voltage gain of CUR.AMP

(4) PWM comparator

Fig.9 shows the configuration of PWM comparator. Oscillator output V_{CT} and current error amplifier output V_{IFB} are compared. While $V_{CT} < V_{IFB}$, PWM comparator output goes High and OUT pin also goes High. Note that, during the oscillator discharge period, OUT pin is forced to be Low, thereby determining the maximum duty cycle. (see characteristics curve).

CS pin (pin 11) is a soft start pin. When start up, an internal constant current (11μA (typ.)) charges capacitor C4 for soft start. Priority is given to V_{CS} or V_{IFB} whichever is lower. Fig.10 shows PWM comparator timing chart.

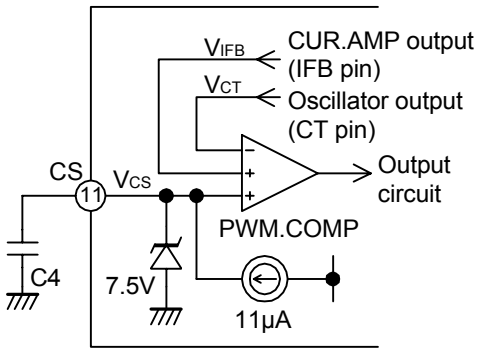


Fig.9 PWM comparator circuit

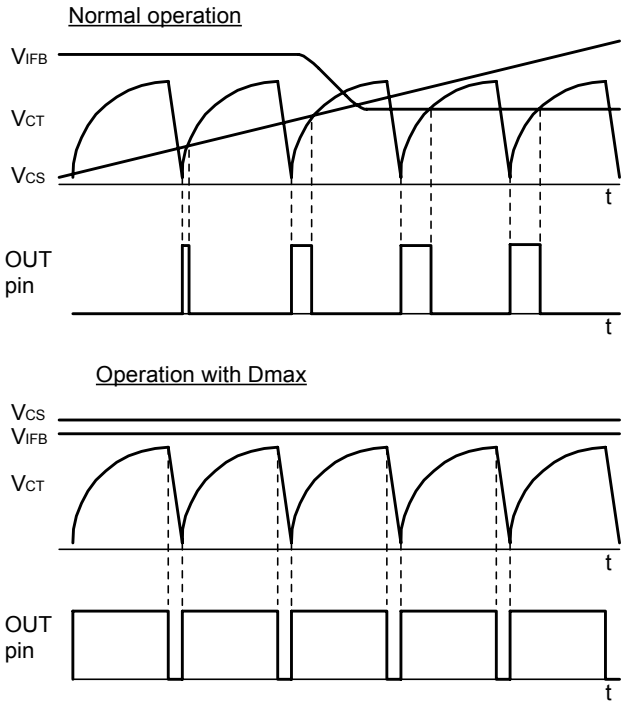


Fig.10 PWM comparator timing chart

(5) Multiplier

The multiplier generates a current reference signal. The rectified line voltage is divided down by resistor and monitored by VDET pin (pin 3). Considering the dynamic range of multiplier, design the R6 and R7 in Fig.11 so that the peak voltage at VDET pin within a range from 0.65V to 2.4V over the entire range of line voltage. VFB pin is normally above 1.55V and, at this status, multiplier output voltage Vm is approximately expressed by:

$$Vm = 1.25 - K \times (V_{VFB} - 1.55) \times V_{VDET} \quad \cdots\cdots (8)$$

Where

K: Output voltage factor (multiplier section)

When VFB pin is lower than 1.55V, compensation circuit for light load operates.

As shown in Fig.7, Vm is applied via a resistor of 11 kΩ to inverting input (IIN-) of current error amplifier CUR. AMP. (For input/output characteristics of multiplier, see characteristics curve.)

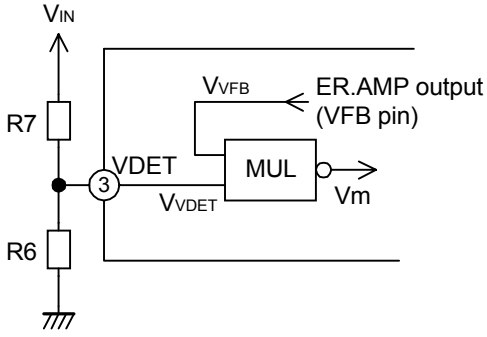


Fig.11 Multiplier circuit

(6) ON/OFF control circuit

Fig.12 shows the configuration of the ON/OFF control circuit. The ON/OFF control circuit consists of a comparator with hysteresis. To turn the IC from OFF mode to operating mode, pull up the ON/OFF pin voltage to 3.95V (typ.) or higher. On the other hand, to turn the IC from operating mode to OFF mode, pull down the ON/OFF pin to 2.80V (typ.) or lower.

In the OFF mode, the reference (REF) voltage is cut off, and the CS pin and OUT pin go approximately 0V. IC consumption current during OFF mode is 200μA (max.) which is much smaller than at an operating mode.

The input current at ON/OFF pin is a very small value of 500nA.

In the case that external signal is applied to ON/OFF pin, the ON/OFF pin voltage must not exceed the VCC pin voltage, even when start up or stop operation.

If ON/OFF operation is not made by external signal, the ON/OFF pin is normally pulled up to Vcc pin through 10kΩ to 1MΩ. Then ON/OFF pin voltage goes to approximately Vcc voltage.

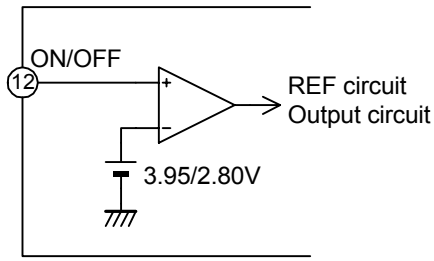


Fig.12 ON/OFF control circuit

(7) Output circuit

As shown in Fig.13, VC pin (pin 9) is configured as the high power terminal, independent of the IC power terminal (VCC pin). This pin allows an independent drive resistance when the power MOSFET is ON and OFF. Suppose the drive resistance when ON and OFF are Rg (on) and Rg (off),

Rg(on)=Rg1+Rg2 • • • • • (9)
Rg(off)=Rg2 • • • • • (10)

At standby, the OUT pin is kept Low.

If the drain voltage of power MOSFET oscillates, a parasitic capacitance between gate and drain may swing the OUT pin (pin 8) of IC below 0V. If OUT pin voltage falls below -0.3V, a current may flow to the parasitic element in IC, whereby the IC may malfunction. In such a case, Schottky diode must be connected between OUT pin and GND so as not to allow a parasitic current to flow to IC.

If VC pin is fed with a source which is independent of VCC pin, the voltage of VC pin must not exceed that of VCC pin even start up or stop operation.

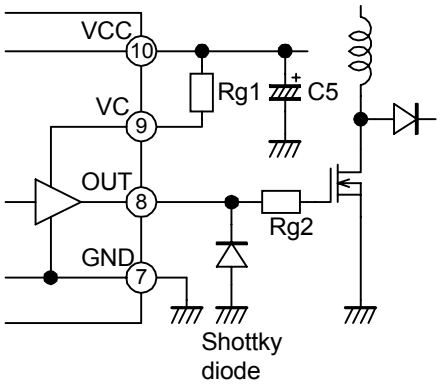


Fig.13 Output circuit

(8) Undervoltage lockout circuit

This IC contains an undervoltage lockout circuit to prevent malfunction when the Vcc voltage drops. When the Vcc voltage rises from 0V, this IC starts operation at 16.5V (typ.). If the Vcc voltage drops after the IC starts up, this IC stops operation at 8.9V(typ.). When IC stops operation by undervoltage lockout circuit, OUT pin and CS pin is kept low

(9) Compensation circuit for light load

If the output of multiplier and the input of current error amplifier do not have offset voltage, the input current to the converter is approximately zero under condition that the PFC converter operates in no load. But an actual multiplier and current error amplifier may have offset voltage. If the offset voltage is negative, the input current, which corresponds to the offset voltage, flows into the converter even when the PFC converter operates in no load. In this case, the PFC output voltage rises abnormally because of too much input current.

To avoid these, this IC has an automatic offset correction circuit for light load. The output voltage of error amplifier is approximately 1.55V or higher in normal operation.

If the output voltage drops below 1.55V, this circuit operates. If there is a negative offset voltage, the output voltage of error amplifier falls below 1.55V in the case that the PFC converter operates in no load or light load. Then, the offset voltage is corrected in the multiplier circuit. Because of this operation, even under no load or light load, the PFC output voltage does not rise abnormally, but is always kept stable. The amount of correction changes linearly according to the output of error amplifier, which can make operation stable.

Fig.14 shows the outline of the effect of this circuit.

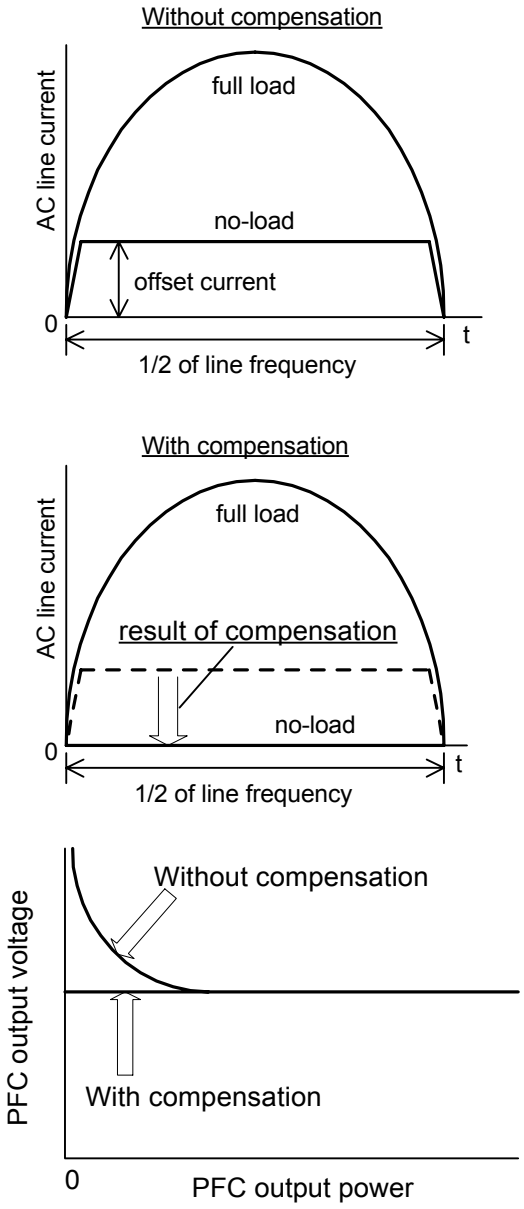


Fig.14 Operation outline of compensation circuit for light load

9. Design advice

(1) Vcc circuit

Vcc voltage can be supplied from an auxiliary winding of the inductor. An example circuit is shown in Fig.15.

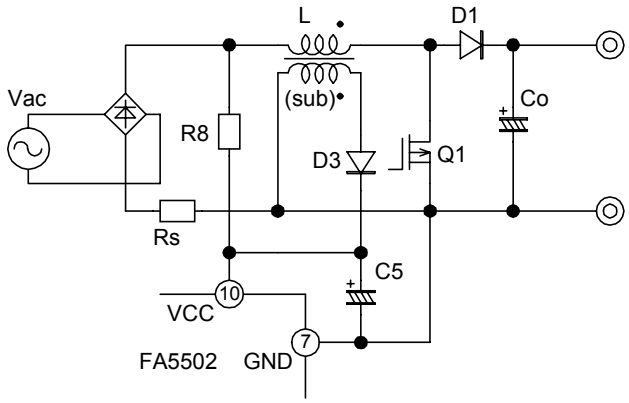


Fig.15 Vcc circuit (1)

In this circuit, R8 is a start up resistor. The start up resistor R8 should be satisfied the following formula in order to supply with at least 30μA of IC start up current.

$$R8 < \frac{\sqrt{2} \times Vac(min) - 17.5}{30 \times 10^{-6}} \quad \cdots\cdots (11)$$

Note that this formula is a minimum condition for starting the IC. Practically, determine the value upon taking into account the start up time required for converter. The start up time must be determined upon measurement at actual circuit operation.

In steady state, Vcc is supplied from the auxiliary winding (sub) of inductor. When the IC is just starting up, however, it takes time for the voltage from auxiliary winding to rise enough. The value of capacitor C5 connected to Vcc pin should be determined to prevent Vcc from falling below the OFF threshold voltage of UVLO during this period. The capacity of C5 should be determined by evaluation in the actual circuit because the time lag is different in each circuit.

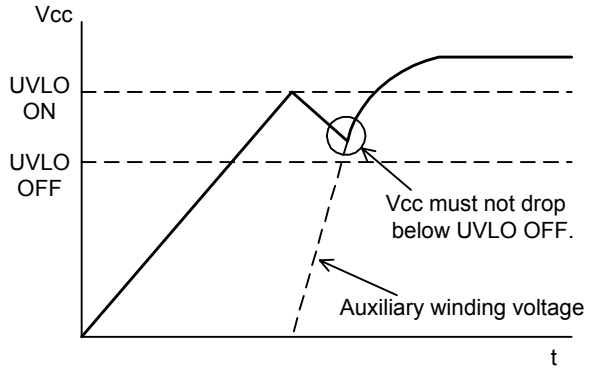


Fig.16 Vcc voltage at start up

Even after PFC starts up, Vcc may fall due to step changes of the load or inputs. To prevent the IC from stopping in those cases, the circuit shown in Fig.17 is effective to prolong the hold time of the Vcc voltage. After the PFC converter starts up, Vcc is supplied through C6. Therefore, you can prolong the hold time of Vcc by using a large capacity for C6.

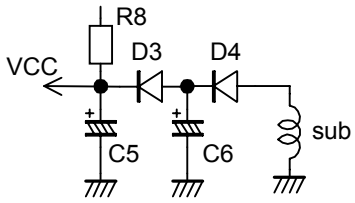


Fig.17 Vcc circuit (2)

In some case, the Vcc voltage cannot be supplied enough in light load condition. In this case, the circuit shown in Fig.18 may be effective to improve the Vcc. The appropriate value of C7 and R9 should be determined by evaluation in actual circuit because they depend on each circuit.

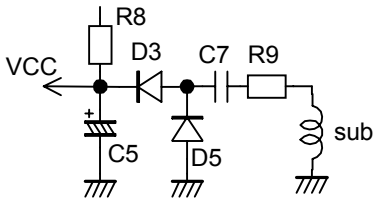


Fig.18 Vcc circuit (3)

(2) Supplying Vcc from external power supply

If Vcc is not supplied from the auxiliary winding of inductor but from an external power supply, pay attention to the followings.

- In order to start up the IC, Vcc must be above the ON threshold voltage VTHUON (17.5V (max.)) of undervoltage lockout circuit (UVLO). When starting up, apply at least this VTHUON. After starting up, the operation is available within the recommended range of 10 to 28V.
- If a noise is applied to Vcc pin, it may cause malfunction. To avoid a noise, connect a capacitor near VCC pin even when Vcc is supplied from an external power supply. To prevent a malfunction, suppress the noise below about ±0.6V. And, make sure there is no malfunction attributable to noise.

(3) Designing a boost converter

Fig.19 shows a basic circuit of boost converter used as an PFC converter. The following describes how to determine each values of the circuit.

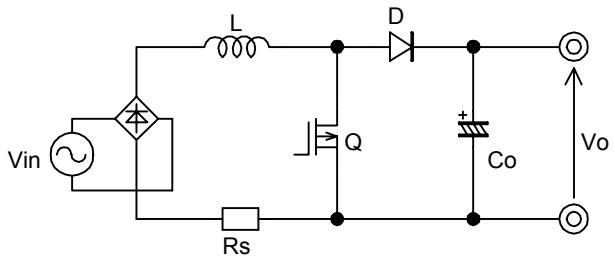


Fig.19 Boost converter circuit

(3-1) Output voltage

Set the output voltage of boost converter at least 10V higher than the peak value of maximum input voltage to ensure a stable operation. When it is used as PFC converter, the input voltage has a sinusoidal waveform. Therefore, set the output voltage Vo by:

$$Vo \geq \sqrt{2} \times Vin_{(max)} + 10 \ [V] \quad \cdots (12)$$

$Vin_{(max)}$: Maximu AC input voltage [Vrms]

(3-2) Inductor

When PFC converter operates in the continuous current mode, select an approximate inductance considering the ratio of inductor ripple current to the peak input current by:

$$L \geq \frac{Vin^2\left(Vo - \sqrt{2} \times Vin\right)}{\gamma \times fs \times Pin \times Vo} \quad \cdots\cdots (13)$$

Where,

Vin: AC input voltage [Vrms]

γ: Ratio of ripple content to peak input current.
(Set to approx. 0.2, see Fig.20)

fs: Switching frequency [Hz]

Pin: Maximum input power [W]

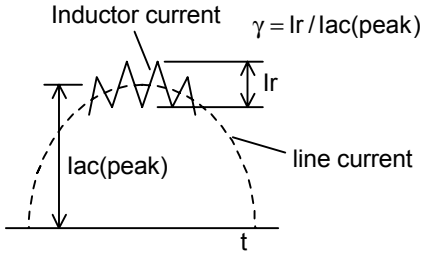


Fig.20 Outline of inductor and AC line current

(3-3) Current detecting resistance Rs

Rs is a resistor which allows to detect an inductor current to control the line current into sinusoidal.

Because the threshold voltage for overcurrent limiting circuit is -1.1V (typ.), peak inductor current limit Ip is calculated by:

$$Ip = \frac{1.1}{R_S} \ [A] \quad \cdots\cdots (14)$$

So that the voltage inputted to IDET pin will not be beyond -1V, whereby the overcurrent limiting circuit will not operate at a normal operation, calculate Rs by:

$$R_S \leq \frac{Vin_{(min)}}{\sqrt{2} \times Pin_{(max)}} \ [\Omega] \quad \cdots\cdots (15)$$

Where,

Vin (min): Minimum AC input voltage [Vrms]

Pin (max): Maximum input position [W]

As a matter of fact, the peak current changes with switching ripple current contained in the inductor current, circuit efficiency, etc. Definitely determine it by evaluation on a actual circuit.

(3-4) Smoothing capacitor

PFC converter output contains ripple voltage of twice the line frequency as shown in Fig.21.

Instantaneous value Vo(t) of output voltage is approximated by:

$$Vo(t) = Vo - \frac{Io}{2\omega_0 \times Co} \times \sin(2\omega_0 \times t) \quad \cdots\cdots (16)$$

Where,

Io: Output current [A]

$\omega_0 = 2\pi f_0$ (f_0: AC line frequency [Hz])

Co: Output smoothing capacitance [F]

Therefore, output ripple voltage Vrp (p-p) is:

$$Vrp = \frac{Io}{\omega_0 \times Co} \quad \cdots\cdots (17)$$

Using formula (17), determine the necessary value. The overvoltage limiting circuit of FA5502 monitors the instantaneous output voltage. Therefore, determine the capacitance of smoothing capacitor Co so that the instantaneous output voltage including the ripple at a normal operation will not reach the overvoltage limit.

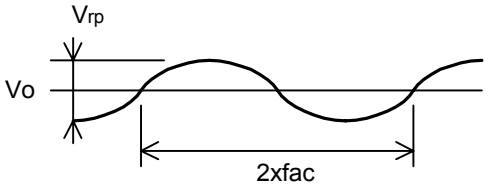


Fig.21 Output ripple voltage

(4) Output overvoltage at light load

A compensation circuit for light load is incorporated for preventing an overvoltage when light or no load. Though, according to the condition, this circuit may not compensate enough and overvoltage may occur. To prevent overvoltage, the following condition must be satisfied.

- Noise filter resistor Rn connected to IDET pin (pin 16) must be below 27Ω.
- As shown in Fig.22, DC gain limiting resistor R10 for current error amplifier must not be connected between IFB pin (pin 1) and IIN- pin (pin 2).

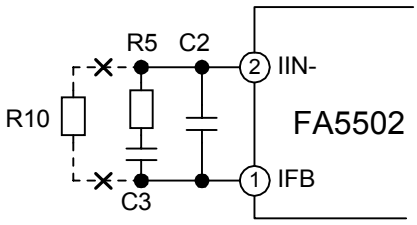


Fig.22 Prevention of overvoltage at light load

(5) Notes for setting the output voltage and overvoltage limit

In the actual circuit, the output voltage drops depending on the line voltage or load current. Therefore, the output voltage may be lower than the voltage calculated by expression (1) in "8-(2)". When setting the output voltage, sufficiently evaluate it on an actual circuit.

On the circuit shown in Fig.6 in "8-(2)", the overvoltage setting is fixed at 1.058 times the output voltage setting.

For setting the overvoltage independently of the output voltage setting, connect voltage divider additionally to OVP pin as shown in Fig.23.

On the circuit in Fig.23, even if the voltage divider for setting the output voltage has troubled, the overvoltage limiting circuit operates properly, thereby preventing the output voltage from rising excessively.

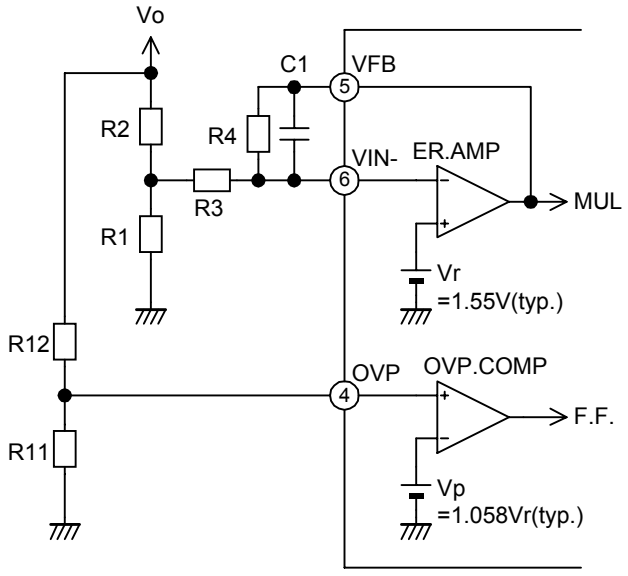


Fig.23 Independent setting of OVP limit

(6) Improvement of output voltage regulation

As stated in “9-(5)”, the output voltage may change with input voltage or load current on the circuit in Fig.6 in "8-(2)", thereby causing a problem in some case. In such a case, the circuit in Fig.24 may improve the regulation.

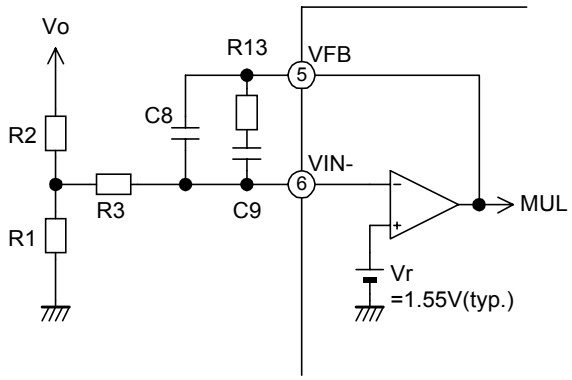


Fig.24 ER.AMP circuit for improvement of regulation

Voltage gainAv2 of this circuit is expressed by:

$$A_{V2} = \frac{1 + j\omega C9 \times R13}{j\omega((C8 + C9) + j\omega C8 \times C9 \times R13)R3} \quad \cdots (18)$$

Optimum values depend on an each circuit. Referring the following relations or the example applied to “10 Example of application circuit”, adjust the values on actual circuit.

- Set the voltage gain Av2 at 100 or 120 Hz almost the same as before changing the compensation circuit.

- Determine C8, C9 and R13 so as to satisfy the following relations.

  • Set fz determined by the following expression to several Hz to several ten Hz.

  $$f_Z = \frac{1}{2\pi C9 \times R13} \quad \cdots\cdots (19)$$

  • Set fp determined by the following expression so that the fp/fz ratio is about 10.

  $$fp = \frac{1}{2\pi C \times R13} \qquad C = \frac{C8 \times C9}{C8 + C9} \quad \cdots\cdots (20)$$

  *Example of values applied to “10 Example of application circuit”
  C8=0.033μF, C9=0.15μF,
  R13=330kΩ, R3=100kΩ
  (These values are given as references and not intended for guaranteeing the operation in any circuit.)

In this circuit, not only the output voltage characteristics at a steady status but also transient response to line voltage and load current may change. Before determining the circuit values, evaluate sufficiently.

(7) Prevention of intermittent switching of low frequency

An intermittent switching below 10 Hz may occur in some application. It may be avoided by the following methods. They are given as typical preventions of intermittent switching and may not be effective for certain circuits. They may also affect the characteristics of PFC converter. Sufficiently check the operation on a actual circuit.

(7-1) Lowering the dc gain of voltage error amplifier

Lower the dc gain of the voltage error amplifier. Concretely, reduce the resistance of R4 on the circuit in Fig.6 in "8-(2)". Note that, in this case, the line and load regulation will be lowerd.

(7-2) Connection of Rofst

Adjust the offset of the current error amplifier. Concretely, connect a resistor Rofst of 1MΩ or higher between REF pin and IIN- pin as shown in Fig.25. Note that, in this case, the input current will be distorted and the power factor will be slightly lowered.

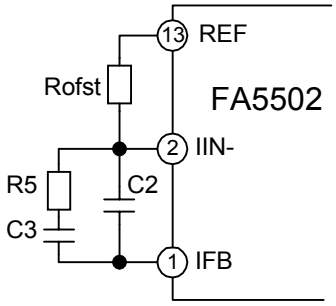


Fig.25 Connection of Rofst

(7-3) Change of compensation network of voltage error amplifier

Replace the compensation network connected to the voltage error amplifier with the circuit in Fig.24 in "9-(6)". Note that, in this case, the transient response may be different from that before the change.

(8) Improvement of operation around zero crossing

In some application, surge current may appear on the line current around zero crossing. This surge current may cause harmonic current especially in high order. In such a case, the following method may suppress this surge current.

(8-1) Connection of Rofst

As shown in Fig.25, connect resistor Rofst between REF pin and IIN- pin. Use a resistor of about 1MΩ or higher.

(8-2) Increase of Dmax

Increase the maximum duty cycle. Concretely, select such a network of R_T and C_T for the same frequency that C_T is a smaller and R_T a larger.

(See (9) Oscillator setting and maximum duty cycle.)

(9) Oscillator setting and maximum duty cycle

The maximum duty cycle is determined by forcing the OUT pin to be Low during the oscillator discharge period. The oscillator discharge period changes with R_T and C_T connected to CT pin. On a network of C_T and R_T providing the same oscillation frequency, the discharge period shortens and the maximum duty cycle increases by minimizing C_T and maximizing R_T. (See characteristics curve.) The maximum duty cycle may affect the input current waveform, particularly at zero crossing. Therefore, sufficiently test C_T and R_T before determining them. Too small C_T could not give a stable oscillation on account of noise, etc. It should be 330pF or more according to the recommended condition.

(10) Npte in use of SYNC pin

If the external synchronizing signal is not a square waveform or if has a trapezoid shape, a differentiating circuit of RC network may not satisfy the waveform condition shown in Fig.3 in “8-(1)”. In such a case, convert the external synchronizing signal into a square waveform by means of comparator or the like before inputting it to a differentiating circuit of RC network. (See "8-(1) Oscillator section".)

(11) Prevention of malfunction by noise

Noise applied to each pin may cause malfunction of IC. If noise causes malfunction, see the notes summarized below and confirm in actual circuit to prevent malfunction.

Capacitor for noise suppressing should be connected as close to IC as possible so as to suppress noise effectively.

(11-1) REF pin

REF pin voltage is supplied to each components of IC as voltage source and reference voltage. A noise applied to this pin may cause a malfunction of IC. To suppress a malfunction by noise, connect a capacitor of 0.1 μF or more between REF pin and GND.

(11-2) IDET pin

If a noise is applied to IDET pin which detects induvtor current, the overcurrent limiting circuit may suffer from a malfunction. In such a case, insert an RC filter at IDET pin.

(11-3) OVP pin

If a noise applied to OVP pin causes a malfunction, connect a noise suppressing capacitor between OVP and GND pins.

(11-4) CT pin

A noise applied to CT pin, which is an oscillator output, may disturb the oscillation frequency or OUT pulses. The wiring between oscillator timing capacitor C_T and IC must be as short as possible so as to suppress the noise to CT pin. Pay utmost attention to

GND wiring so as not to generate a common impedance with other wires.

(11-5) VCC pin

A noise applied to VCC pin may cause a malfunction. To suppress this noise, connect a capacitor near VCC pin even if IC is energized by another power supply. Determine the capacitance so that the noise generated at VCC pin will be within about ±0.6V . Then, make sure no malfunction occurs by noise.

(12) Voltage rating of IDET pin

The voltage rating of IDET pin, which monitors an inductor current, is -10V. In case of a general boost circuit, a inrush current for charging the output smoothing capacitor Co flows at the instant when an AC input voltage is connected. This current may be by far greater than the input current at a normal operation. As a result, a voltage much higher than normal may be applied to IDET pin. Pay attention so that a voltage beyond the maximum voltage rating of -10V will not be applied to IDET pin even at an instant when an AC input voltage has been connected. If there are cases where a voltage higher than rating is applied to IDET pin, insert a limiting circuit for inrush current, or add a Zener diode as shown in Fig.26 or 27 to suppress the voltage applied to IDET pin.

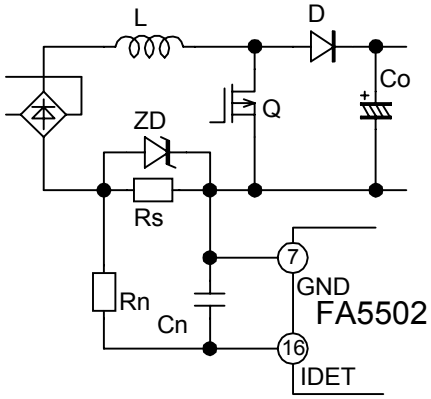


Fig.26 IDET pin protection (1)

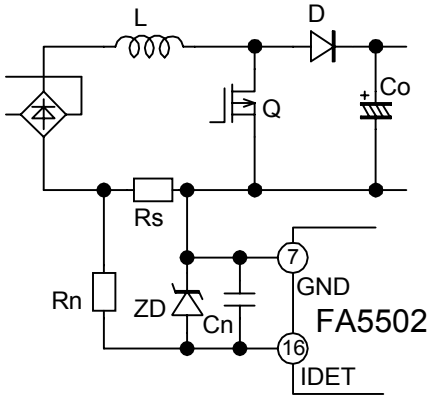
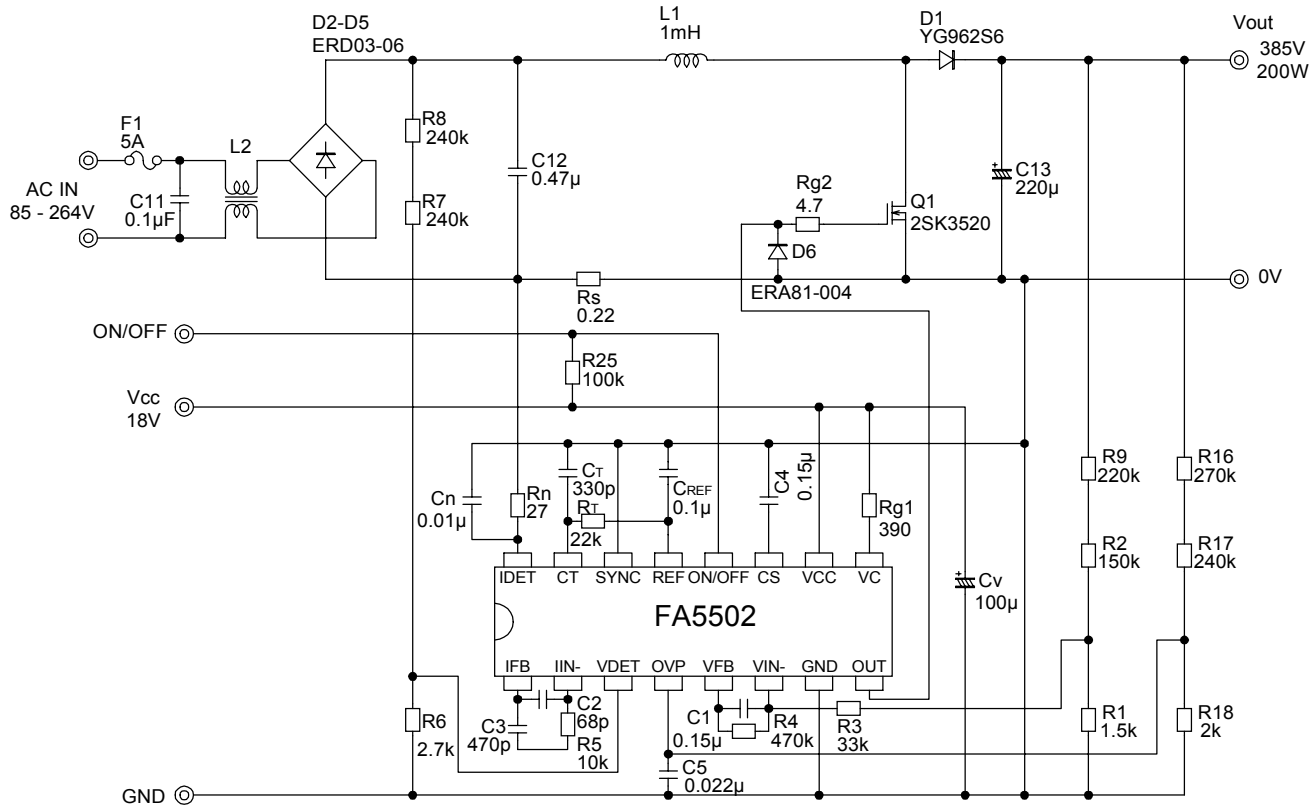


Fig.27 IDET pin protection (2)

(13) Prevention of malfunction by negative voltage of each pin

IDET pin is so designed as to input a negative voltage. In the case of other pins, however, if large negative voltage is applied, parasitic elements in IC may operate and it may cause a malfunction. Pay attention so that the voltage applied to pins other than IDET pin will not be lower than -0.3V.

10. Example of application circuit



Note

This application circuit exemplifies the use of IC for your reference only. Parts tolerance, parts characteristics, influence of noise, etc. are not defined in this application circuit. When design an actual circuit for a product, you must determine parts tolerance, parts characteristics, influence of noise, etc. for safe and economical operation. Neither Fuji nor its agents shall be liable for any injury caused by any use of this circuit.