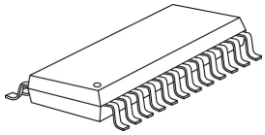
# 16-Channel Constant Current LED Driver With 16-bit PWM Control

## Features

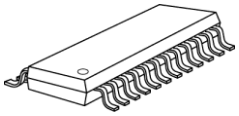
- Backward compatible with MBI5026 and MBI5030 in package
- 16 constant-current output channels
- 16-bit color depth PWM control
- Scrambled-PWM technology to improve refresh rate
- 6-bit programmable output current gain
- Constant output current range: 2~30mA @ 5.0V / 3.3V supply voltage
- Output current accuracy:
  Between channels: <±1.5% (typ.), and
  Between ICs: <±3.0% (typ.)
- Staggered delay of output, preventing from current surge
- Maximum data clock frequency: 30MHz
- Schmitt trigger input
- 3.0V-5.5V supply voltage

**Small Outline Package**



GF: SOP24L-300-1.00

**Shrink SOP**



GP: SSOP24L-150-0.64

## Product Description

MBI5041 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with 16-bit color depth. MBI5041 features a 16-bit shift register which converts serial input data into each pixel gray scale of output port. At MBI5041 output port, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs with a wide range of $V_F$ variations. The output current can be preset through an external resistor. Moreover, the preset current of MBI5041 can be further programmed to 64 gain steps for LED global brightness adjustment.

With Scrambled-PWM (S-PWM) technology, MBI5041 enhances Pulse Width Modulation by scrambling the “on” time into several “on” periods. The enhancement equivalently increases the visual refresh rate. When building a 16-bit color depth video, S-PWM reduces the flickers and improves the fidelity. MBI5041 offloads the signal timing generation of the host controller which just needs to feed data into drivers. MBI5041 drives the corresponding LEDs to the brightness specified by image data. With MBI5041, all output channels can be built with 16-bit color depth (65,536 gray scales). Each LED’s brightness can be calibrated enough from minimum to maximum brightness with compensated gamma correction or LED deviation information inside the 16-bit image data.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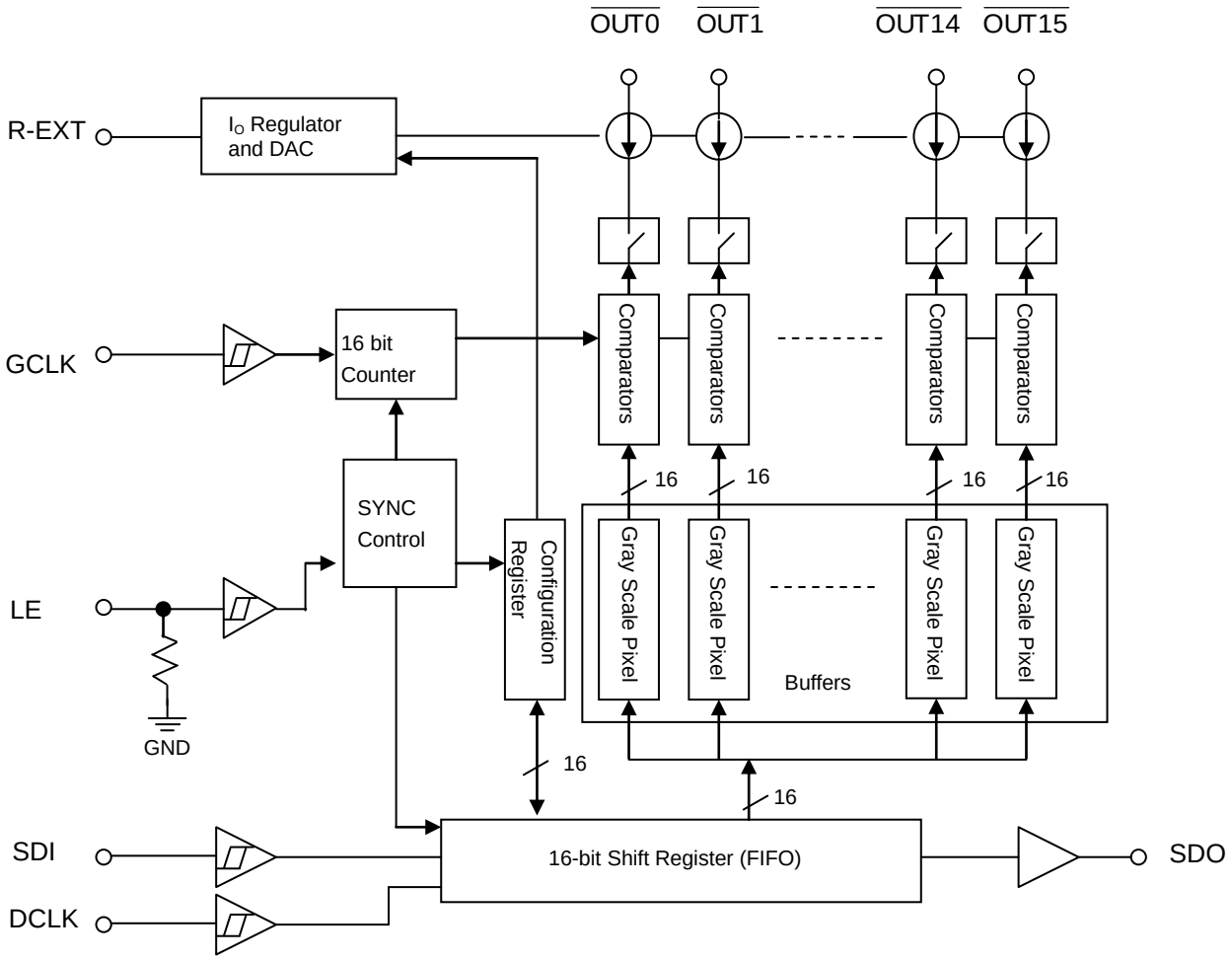
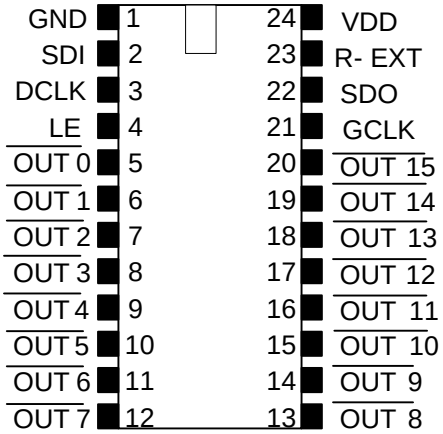
## Block Diagram



## Pin Configuration



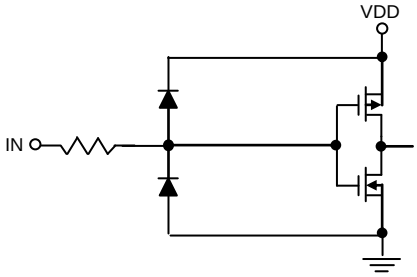

MBI5041GF/GP

## Terminal Description

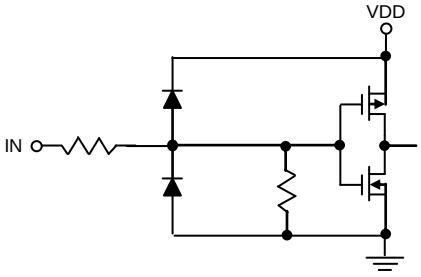
| Pin Name | Function |
|---|---|
| GND | Ground terminal for control logic and current sink |
| SDI | Serial-data input to the shift register |
| DCLK | Clock input terminal used to shift data on rising edge and carries command information when LE is asserted |
| LE | Data strobe terminal and controlling command with DCLK |
| $\overline{OUT0}$ ~ $\overline{OUT15}$ | Constant current output terminals |
| GCLK | Gray scale clock terminal<br>Clock input for gray scale. The gray scale display is counted by gray scale clock comparing with input data |
| SDO | Serial-data output to the receiver-end SDI of next driver IC |
| R-EXT | Input terminal used to connect an external resistor for setting up output current for all output channels |
| VDD | 3.3V/5V supply voltage terminal |

## Equivalent Circuits of Inputs and Outputs

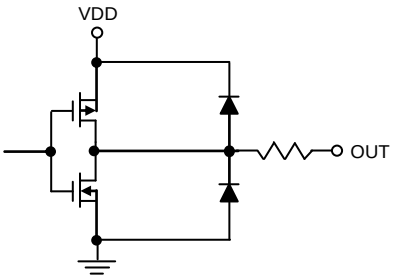
**GCLK, DCLK, SDI terminal**




**LE terminal**




**SDO terminal**




## Maximum Rating

| Characteristic | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Supply Voltage | | $V_{DD}$ | 7 | V |
| Input Pin Voltage (SDI, LE, DCLK, GCLK) | | $V_{IN}$ | -0.4~$V_{DD}$+0.4 | V |
| Output Current ($\overline{OUT0}$ ~ $\overline{OUT15}$) | | $I_{OUT}$ | +50 | mA |
| Sustaining Voltage at OUT Port | | $V_{DS}$ | -0.5~17 | V |
| GND Terminal Current | | $I_{GND}$ | +720 | mA |
| Power Dissipation (On PCB, Ta=25°C)* | GF Type | $P_D$ | 2.52 | W |
| | GP Type | | 2.03 | |
| Thermal Resistance (On PCB, Ta=25°C)* | GF Type | $R_{th(j-a)}$ | 49.69 | °C/W |
| | GP Type | | 61.56 | |
| Junction Temperature | | $T_{j,max}$ | 150** | °C |
| Operating Ambient Temperature | | $T_{opr}$ | -40~+85 | °C |
| Storage Temperature | | $T_{stg}$ | -55~+150 | °C |
| ESD Rating | HBM (MIL-STD-883G Method 3015.7, Human Body Mode) | HBM | ≧8000V | - |
| | MM (JEDEC EIA/JESD22-A115, Machine Mode) | MM | ≧400V | - |

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

## Electrical Characteristics ($V_{DD}$=5.0V)

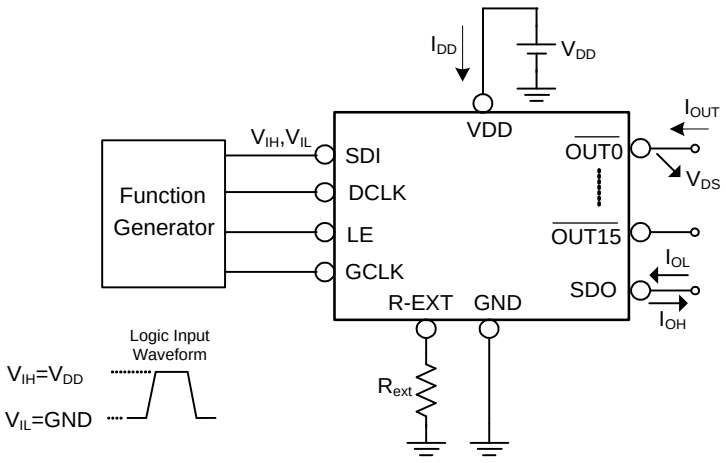
| Characteristics | | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| Supply Voltage | | $V_{DD}$ | - | | 4.5 | 5.0 | 5.5 | V |
| Sustaining Voltage at OUT Ports | | $V_{DS}$ | $\overline{OUT0}$ ~ $\overline{OUT15}$ | | - | - | 17.0 | V |
| Output Current | | $I_{OUT}$ | Refer to "Test Circuit for "Electrical Characteristics" | | 2 | - | 30 | mA |
| | | $I_{OH}$ | SDO | | - | - | -1.0 | mA |
| | | $I_{OL}$ | SDO | | - | - | 1.0 | mA |
| Input Voltage | "H" level | $V_{IH}$ | Ta=-40~85ºC | | 0.7x$V_{DD}$ | - | $V_{DD}$ | V |
| | "L" level | $V_{IL}$ | Ta=-40~85ºC | | GND | - | 0.3x$V_{DD}$ | V |
| Output Leakage Current | | $I_{OH}$ | $V_{DS}$=17.0V | | - | - | 0.5 | μA |
| Output Voltage | SDO | $V_{OL}$ | $I_{OL}$=+1.0mA | | - | - | 0.4 | V |
| | | $V_{OH}$ | $I_{OH}$=-1.0mA | | $V_{DD}$-0.4V | - | - | V |
| Current Skew (Channel) | | $dI_{OUT}$ | $I_{OUT}$=2mA $V_{DS}$=1.0V | $R_{ext}$=7KΩ | - | ±1.5 | ±3.0 | % |
| | | | $I_{OUT}$=25mA $V_{DS}$=1.0V | $R_{ext}$=560Ω | - | ±1.5 | ±3.0 | % |
| Current Skew (IC) | | $dI_{OUT2}$ | $I_{OUT}$=2mA $V_{DS}$=1.0V | $R_{ext}$=7KΩ | - | ±3.0 | ±6.0 | % |
| | | | $I_{OUT}$=25mA $V_{DS}$=1.0V | $R_{ext}$=560Ω | - | ±3.0 | ±6.0 | % |
| Output Current vs. Output Voltage Regulation* | | %/$dV_{DS}$ | $V_{DS}$ within 1.0V and 3.0V, $R_{ext}$=560Ω@25mA | | - | ±0.1 | ±0.3 | % / V |
| Output Current vs. Supply Voltage Regulation* | | %/$dV_{DD}$ | $V_{DD}$ within 4.5V and 5.5V | | - | ±1.0 | ±2.0 | % / V |
| Pull-down Resistor | | $R_{IN}$(down) | LE | | 250 | 450 | 800 | KΩ |
| Supply Current | "Off" | $I_{DD}$(off) 1 | $R_{ext}$=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off | | - | 1.8 | 5.0 | mA |
| | | $I_{DD}$(off) 2 | $R_{ext}$=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off | | - | 4.0 | 8.0 | |
| | | $I_{DD}$(off) 3 | $R_{ext}$=360Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off | | - | 6.0 | 10.0 | |
| | "On" | $I_{DD}$(on) 1 | $R_{ext}$=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On | | - | 4.2 | 8.0 | |
| | | $I_{DD}$(on) 2 | $R_{ext}$=360Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On | | - | 6.3 | 10.0 | |

*One channel on.

## Electrical Characteristics ($V_{DD}$=3.3V)

| Characteristics | | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| Supply Voltage | | $V_{DD}$ | - | | 3.0 | 3.3 | 3.6 | V |
| Sustaining Voltage at OUT Ports | | $V_{DS}$ | $\overline{OUT0}$ ~ $\overline{OUT15}$ | | - | - | 17.0 | V |
| Output Current | | $I_{OUT}$ | Refer to "Test Circuit for "Electrical Characteristics" | | 2 | - | 30 | mA |
| | | $I_{OH}$ | SDO | | - | - | -1.0 | mA |
| | | $I_{OL}$ | SDO | | - | - | 1.0 | mA |
| Input Voltage | "H" level | $V_{IH}$ | Ta=-40~85ºC | | 0.7x$V_{DD}$ | - | $V_{DD}$ | V |
| | "L" level | $V_{IL}$ | Ta=-40~85ºC | | GND | - | 0.3x$V_{DD}$ | V |
| Output Leakage Current | | $I_{OH}$ | $V_{DS}$=17.0V | | - | - | 0.5 | μA |
| Output Voltage | SDO | $V_{OL}$ | $I_{OL}$=+1.0mA | | - | - | 0.4 | V |
| | | $V_{OH}$ | $I_{OH}$=-1.0mA | | $V_{DD}$-0.4V | - | - | V |
| Current Skew (Channel) | | $dI_{OUT}$ | $I_{OUT}$=2mA $V_{DS}$=1.0V | $R_{ext}$=7KΩ | - | ±1.5 | ±3.0 | % |
| | | $dI_{OUT}$ | $I_{OUT}$=25mA $V_{DS}$=1.0V | $R_{ext}$=560Ω | - | ±1.5 | ±3.0 | % |
| Current Skew (IC) | | $dI_{OUT2}$ | $I_{OUT}$=2mA $V_{DS}$=1.0V | $R_{ext}$=7KΩ | - | ±3.0 | ±6.0 | % |
| | | $dI_{OUT2}$ | $I_{OUT}$=25mA $V_{DS}$=1.0V | $R_{ext}$=560Ω | - | ±3.0 | ±6.0 | % |
| Output Current vs. Output Voltage Regulation | | %/$dV_{DS}$ | $V_{DS}$ within 1.0V and 3.0V, $R_{ext}$=560Ω@25mA | | - | ±0.1 | ±0.3 | % / V |
| Output Current vs. Supply Voltage Regulation | | %/$dV_{DD}$ | $V_{DD}$ within 3.0V and 3.6V | | - | ±1.0 | ±2.0 | % / V |
| Pull-down Resistor | | $R_{IN}$(down) | LE | | 250 | 450 | 800 | KΩ |
| Supply Current | "Off" | $I_{DD}$(off) 1 | $R_{ext}$=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off | | - | 1.6 | 5.0 | mA |
| | | $I_{DD}$(off) 2 | $R_{ext}$=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off | | - | 3.8 | 8.0 | |
| | | $I_{DD}$(off) 3 | $R_{ext}$=360Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off | | - | 5.6 | 10.0 | |
| | "On" | $I_{DD}$(on) 1 | $R_{ext}$=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On | | - | 4.0 | 8.0 | |
| | | $I_{DD}$(on) 2 | $R_{ext}$=360Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On | | - | 6.0 | 10.0 | |

### Test Circuit for Electrical Characteristics



## Switching Characteristics ($V_{DD}$=5.0V)

(Test condition: Ta=25°C)

| Characteristics | | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Setup Time | SDI - DCLK ↑ | $t_{SU0}$ | $V_{DD}$=5.0V<br>$V_{IH}$=$V_{DD}$<br>$V_{IL}$=GND<br>$R_{ext}$=700Ω<br>$V_{DS}$=1V<br>$R_L$=200Ω<br>$C_L$=10pF<br>$C_1$=100nF<br>$C_2$=10μF<br>$C_{SDO}$=10pF | 1 | - | - | ns |
| | LE ↑ – DCLK ↑ | $t_{SU1}$ | | 1 | - | - | ns |
| | LE ↓ – DCLK ↑ | $t_{SU2}$ | | 5 | - | - | ns |
| Hold Time | DCLK ↑ - SDI | $t_{H0}$ | | 3 | - | - | ns |
| | DCLK ↑ - LE ↓ | $t_{H1}$ | | 7 | - | - | ns |
| Propagation Delay Time | DCLK - SDO | $t_{PD0}$ | | - | 25 | 33 | ns |
| | GCLK – $\overline{OUT\,4n}$ * | $t_{PD1}$ | | - | 25 | - | ns |
| | LE – SDO** | $t_{PD2}$ | | - | 30 | 40 | ns |
| Staggered Delay of Output | $\overline{OUT\,4n+1}$ * | $t_{DL1}$ | | - | 5 | - | ns |
| | $\overline{OUT\,4n+2}$ * | $t_{DL2}$ | | - | 10 | - | ns |
| | $\overline{OUT\,4n+3}$ * | $t_{DL3}$ | | - | 15 | - | ns |
| Pulse Width | LE | $t_{W(L)}$ | | 5 | - | - | ns |
| | DCLK | $t_{W(DCLK)}$ | | 15 | - | - | ns |
| | GCLK | $t_{W(GCLK)}$ | | 15 | - | - | ns |
| Output Rise Time of Output Ports | | $t_{OR}$ | | 9 | 15 | - | ns |
| Output Fall Time of Output Ports | | $t_{OF}$ | | 10 | 17 | - | ns |
| Data Clock Frequency | | $F_{DCLK}$ | | - | - | 30 | MHz |
| Gray Scale Clock Frequency*** | | $F_{GCLK}$ | | - | - | 33 | MHz |

* Refer to the Timing Waveform, where n=0, 1, 2, 3.

**In timing of “Read Configuration”, the next DCLK rising edge should be $t_{PD2}$ after the falling edge of LE.

***With uniform output current.

## Switching Characteristics ($V_{DD}$=3.3V)

(Test condition: Ta=25°C)

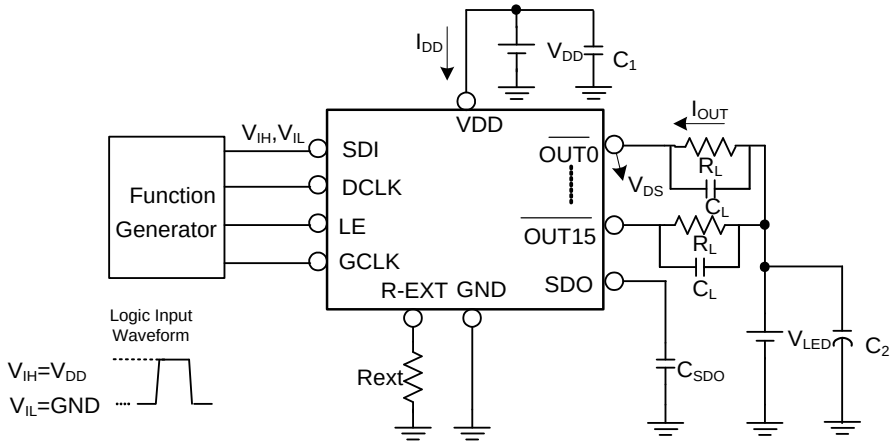
| Characteristics | | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Setup Time | SDI - DCLK ↑ | $t_{SU0}$ | $V_{DD}$=3.3V<br>$V_{IH}$=$V_{DD}$<br>$V_{IL}$=GND<br>$R_{ext}$=700Ω<br>$V_{DS}$=1V<br>$R_L$=200Ω<br>$C_L$=10pF<br>$C_1$=100nF<br>$C_2$=10μF<br>$C_{SDO}$=10pF | 1 | - | - | ns |
| | LE ↑ – DCLK ↑ | $t_{SU1}$ | | 1 | - | - | ns |
| | LE ↓ – DCLK ↑ | $t_{SU2}$ | | 5 | - | - | ns |
| Hold Time | DCLK ↑ - SDI | $t_{H0}$ | | 3 | - | - | ns |
| | DCLK ↑ - LE ↓ | $t_{H1}$ | | 7 | - | - | ns |
| Propagation Delay Time | DCLK – SDO | $t_{PD0}$ | | - | 30 | 40 | ns |
| | GCLK – $\overline{OUT\,4n}$ * | $t_{PD1}$ | | - | 30 | - | ns |
| | LE – SDO** | $t_{PD2}$ | | - | 40 | 50 | ns |
| Staggered Delay of Output | $\overline{OUT\,4n+1}$ * | $t_{DL1}$ | | - | 8 | - | ns |
| | $\overline{OUT\,4n+2}$ * | $t_{DL2}$ | | - | 16 | - | ns |
| | $\overline{OUT\,4n+3}$ * | $t_{DL3}$ | | - | 24 | - | ns |
| Pulse Width | LE | $t_{w(L)}$ | | 5 | - | - | ns |
| | DCLK | $t_{w(DCLK)}$ | | 20 | - | - | ns |
| | GCLK | $t_{w(GCLK)}$ | | 20 | - | - | ns |
| Output Rise Time of Output Ports | | $t_{OR}$ | | 10 | 17 | - | ns |
| Output Fall Time of Output Ports | | $t_{OF}$ | | 20 | 30 | - | ns |
| Data Clock Frequency | | $F_{DCLK}$ | | - | - | 25 | MHz |
| Gray Scale Clock Frequency*** | | $F_{GCLK}$ | | - | - | 20 | MHz |

* Refer to the Timing Waveform, where n=0, 1, 2, 3.

**In timing of “Read Configuration”, the next DCLK rising edge should be $t_{PD2}$ after the falling edge of LE.

***With uniform output current.

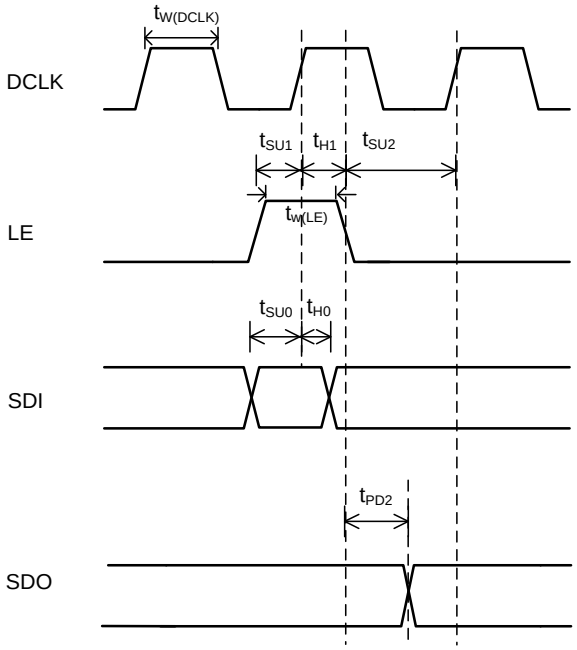
### Test Circuit for Switching Characteristics



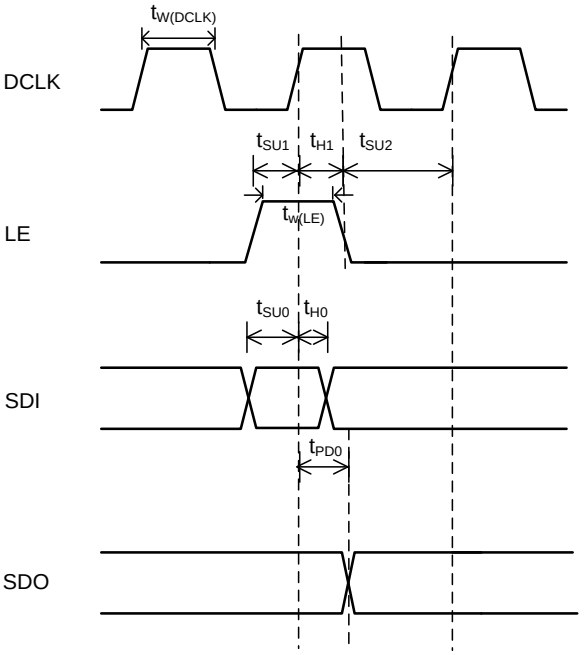
## Timing Waveform

(1)

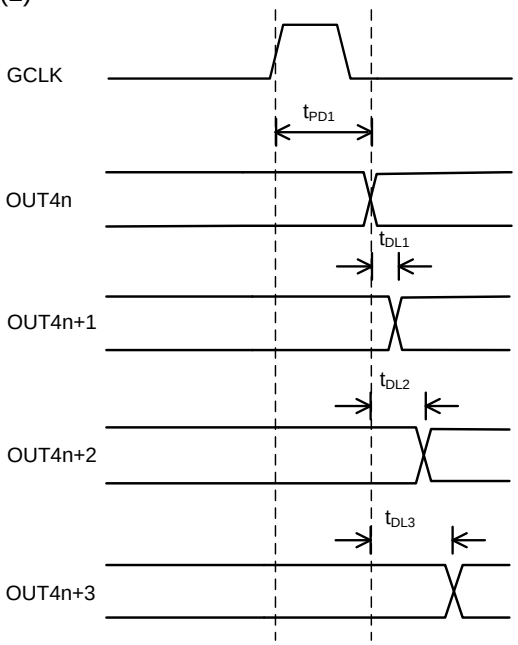
Timing Waveform for Read Configuration



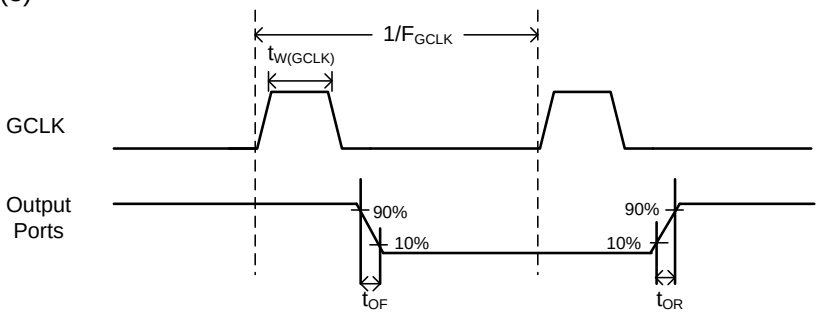

Timing Waveform for Data Latch and Global Latch




(2)




(3)

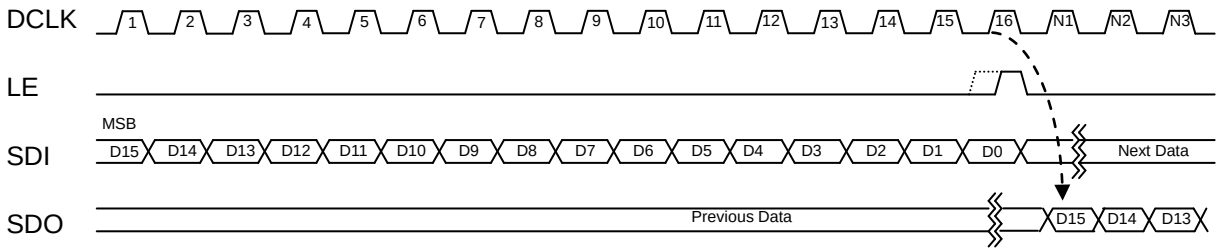


# Principle of Operation

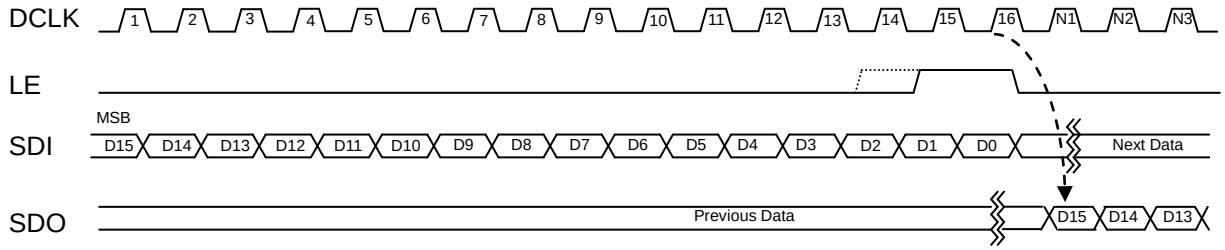
## Control Command

| Command Name | Signals Combination | | Description |
|---|---|---|---|
| | LE | Number of DCLK Rising Edge when LE is asserted | The Action after a Falling Edge of LE |
| Data Latch | High | 0 or 1 | Serial data are transferred to the buffers |
| Global Latch | High | 2 or 3 | Buffer data are transferred to the comparators |
| Read Configuration | High | 4 or 5 | Move out “configuration register” to the shift registers |
| Write Configuration | High | 10 or 11 | Serial data are transferred to the “configuration register” if the “Enable Writing Configuration” is sent in prior |
| Reset PWM Counter | High | 12 or 13 | If bit “B” of the configuration register is set to “1”, this command will reset PWM counter. |
| Enable Writing Configuration | High | 14 or 15 | Enable to writing configuration. It should be sent before writing configuration every time |

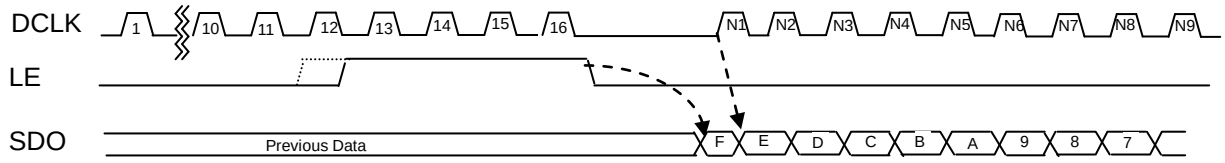
### Data Latch



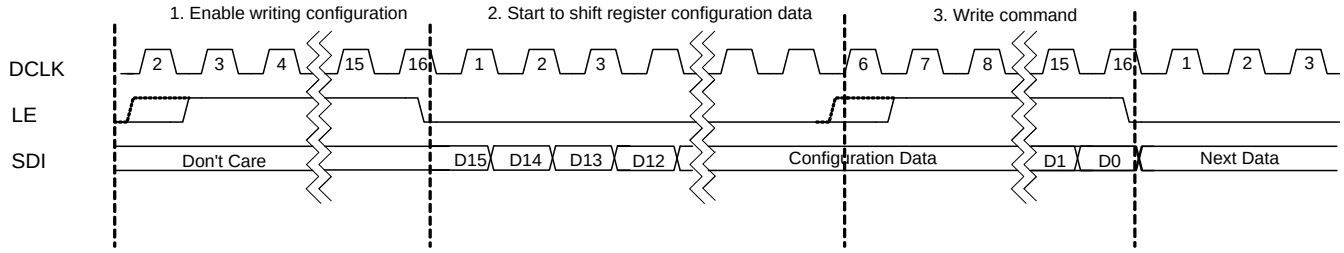

### Global Latch



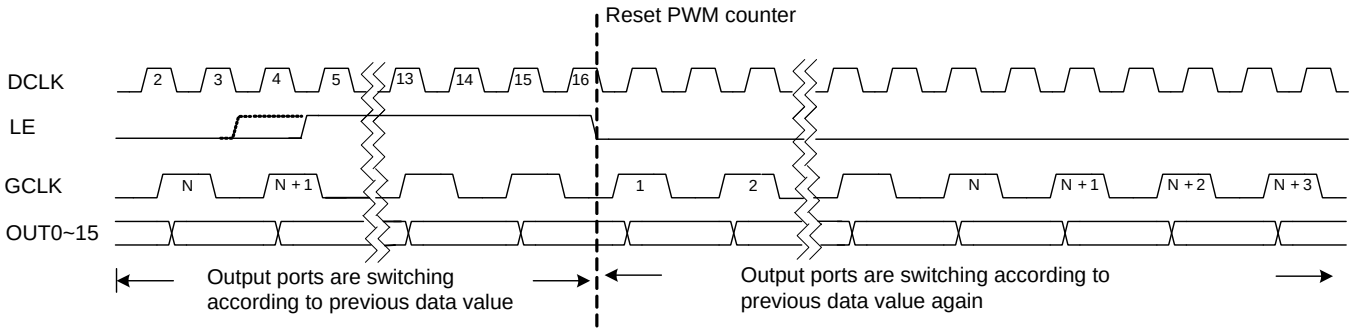

### Read Configuration



### Write Configuration




### Reset PWM Counter




## Setting Gray Scales of Pixels

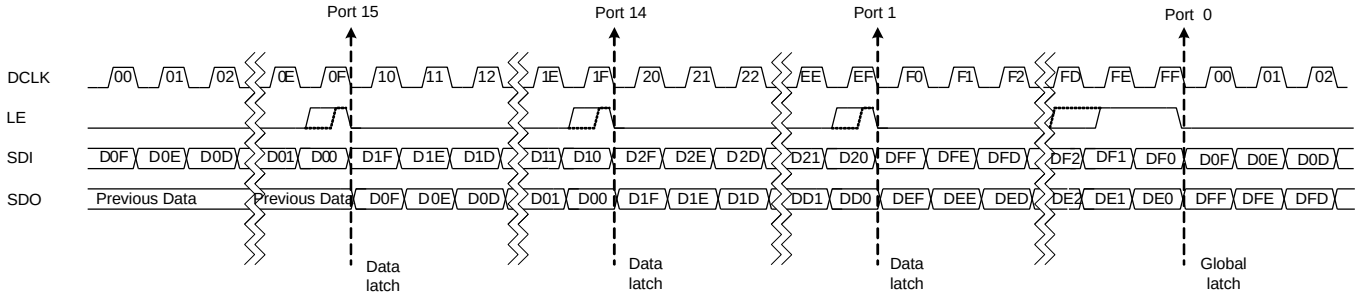
MBI5041 implements the gray level of each output port using the S-PWM control algorithm. With the 16-bit data, all output channels can be built with 65,536 gray scales.

There are two methods to issue the “global latch” command.

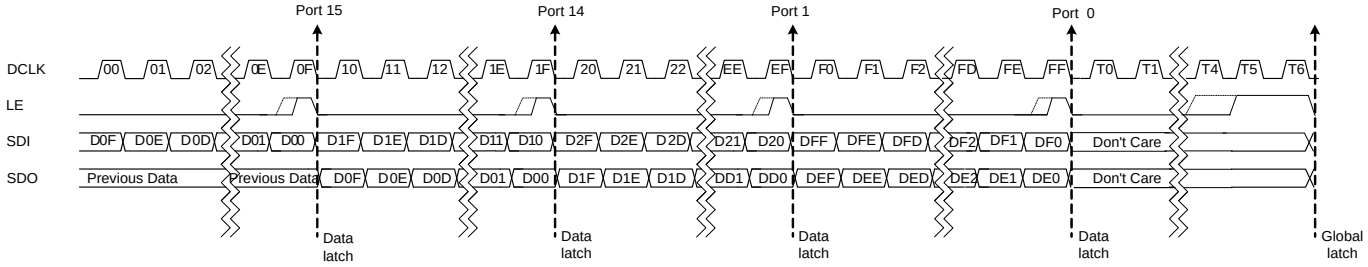
1. When configuration bit “F” is set to “0” (Default), the 16-bit input shift register latches 15 times of the gray scale data into each data buffer with a “data latch” command sequentially. With a “global latch” command for the 16$^{th}$ gray scale data, the data will be clocked in with the MSB first, loading the data from port 15 to port 0.
2. When configuration bit “F” is set to “1”, the 16-bit input shift register latches 16 times of the gray scale data into each data buffer with a “data latch” command sequentially. With a “global latch” command for additional latch, the data will be clocked in with the MSB first, loading the data from port 15 to port 0.

**Full Timing for Data Loading**

When bit “F” = “0”




When bit “F” = “1”




The sequence of output ports is from port 15 to port 0; the sequence of bits is from bit 15 to bit 0.

DCLK: “00” represents the 0 DCLK of port 15; “FF” represents the 15 DCLK of port 0.

SDI: “D0F” represents the MSB SDI of port 15; “DF0” represents the LSB SDI of port 0.

## Definition of Configuration Register

MSB LSB

| F | E | D | C | B | A | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

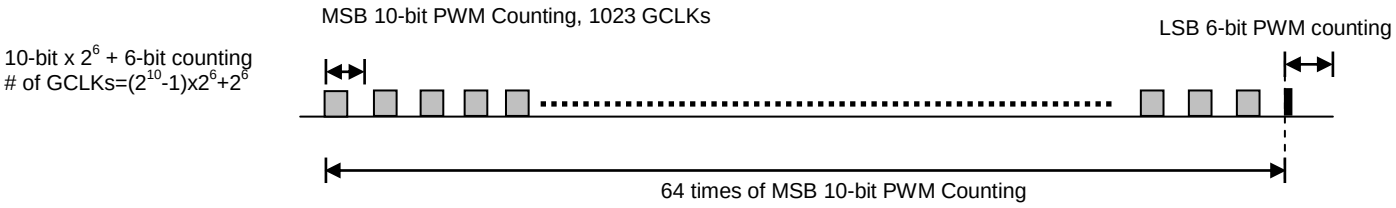
e.g.. Default Value

| F | E | D | C | B | A | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 6’b101011 | | | | | | 0 | 0 | 0 | 0 |

| Bit | Attribute | Definition | Value | Function |
|---|---|---|---|---|
| F | Read/Write | Data loading | 0 (Default) | 15 times of “data latch” + 1 “global latch” |
| | | | 1 | 16 times of “data latch” + 1 “global latch” |
| E~C | Read/Write | Reserved | Don’t care | NA |
| B | Read/Write | PWM counter reset | 0 (Default) | Disable |
| | | | 1 | Enable with 12 or 13 DCLKs (rising edge) when LE is asserted |
| A | Read/Write | PWM data synchronization mode | 0 (Default) | Auto-synchronization |
| | | | 1 | Manual synchronization |
| 9~4 | Read/Write | Current gain adjustment | 000000 ~ 111111 | 6’b101011 (Default) |
| 3~0 | Read/Write | Reserved | Don’t care | NA |

## The PWM Counting Mode

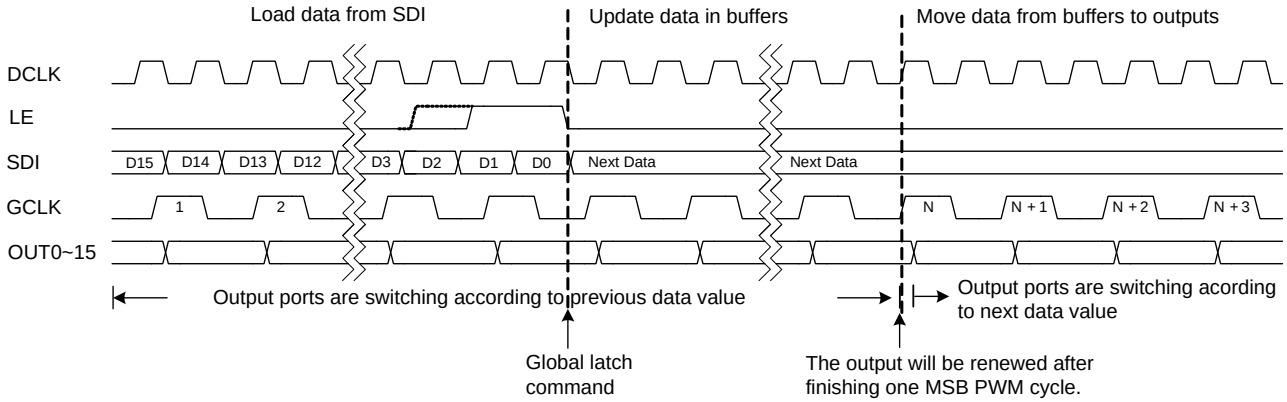
MBI5041 supports S-PWM, scrambled PWM, technology. With S-PWM , the total PWM cycles can be broken down into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles, and the MSB information can be dithered across many refresh cycles to achieve overall same high bit resolution.



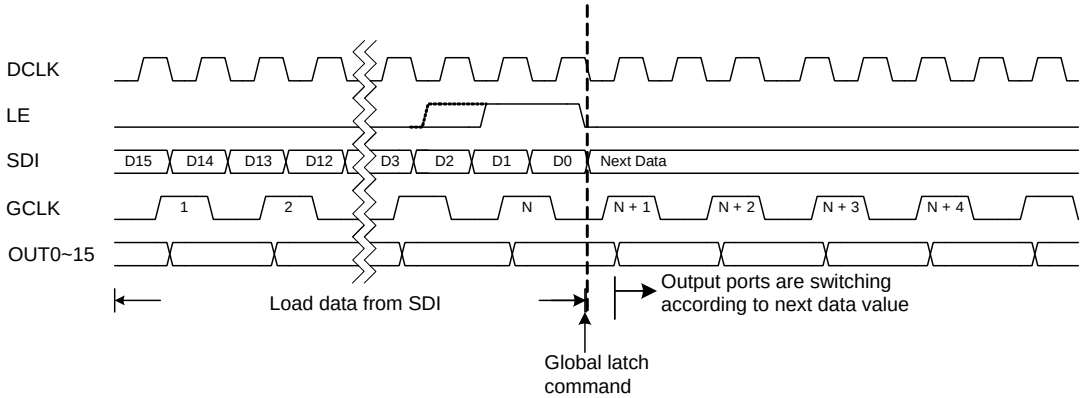

: Output ports are turned “on”.

## Synchronization for PWM Counting

Between the data frame and the video frame, when the bit “A” is set to “0” (Default), MBI5041 will automatically handle the synchronization of previous data and next data for PWM counting. The next image data will be updated to output buffers and start PWM counting when the previous data has finished one internal PWM cycle. It will prevent the lost count of image data resolution and guarantee the data accuracy. In this mode, system controller only needs to provide a continuous running GCLK for PWM counter. The output will be renewed after finishing one MSB PWM cycle.




When the bit “A” is set to “1”, MBI5041 will update the next image data into output buffer immediately, no matter the counting status of previous image data is. In this mode, system controller will synchronize the GCLK according image data outside MBI5041 by itself. Otherwise, the conflict of previous image data and next image data will cause the data lost.



## Constant Current

In LED display application, MBI5041 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The typical current variation between channels is less than 1.5%, and that between ICs is less than ±3.0%.

2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages ($V_F$). This guarantees LED to be performed on the same brightness as user's specification.

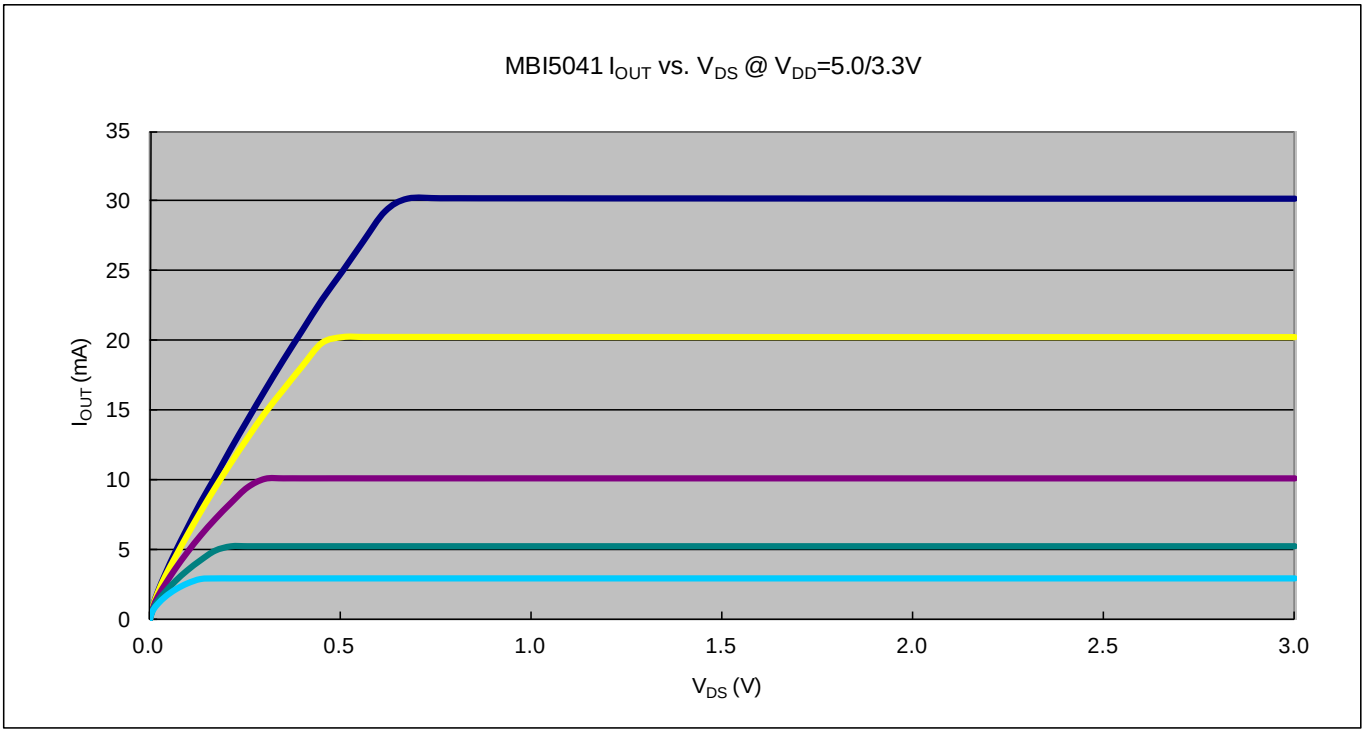



Figure 1

## Setting Output Current

The output current ($I_{OUT}$) is set by an external resistor, $R_{ext}$. The default relationship between $I_{OUT}$ and $R_{ext}$ is shown in the following figure.

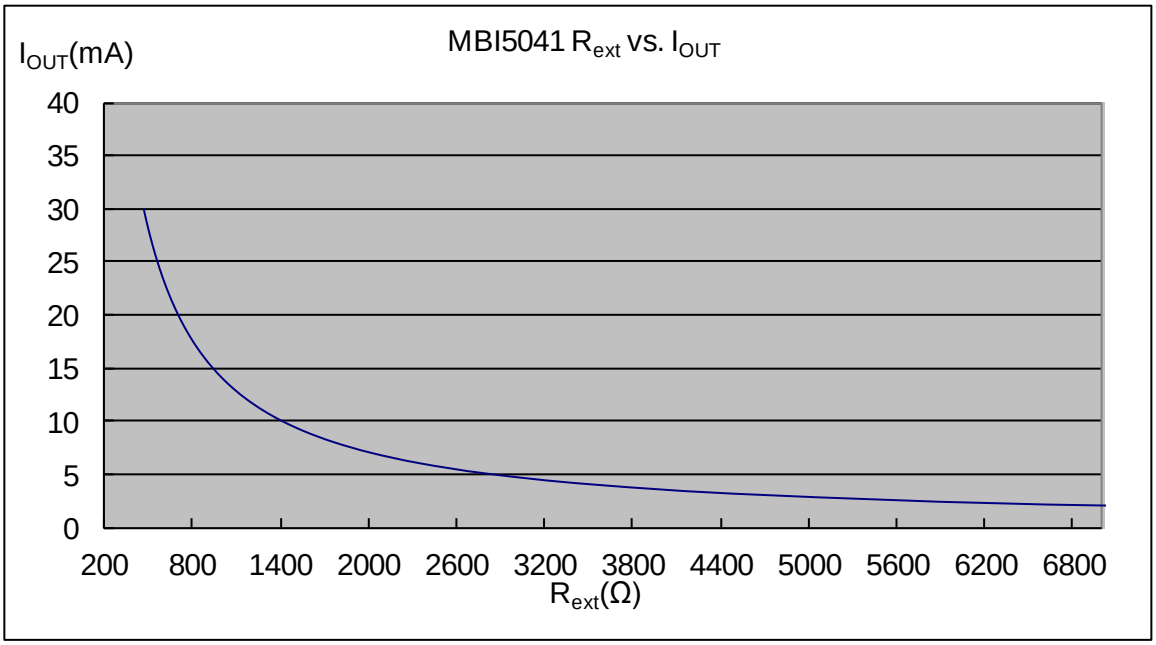


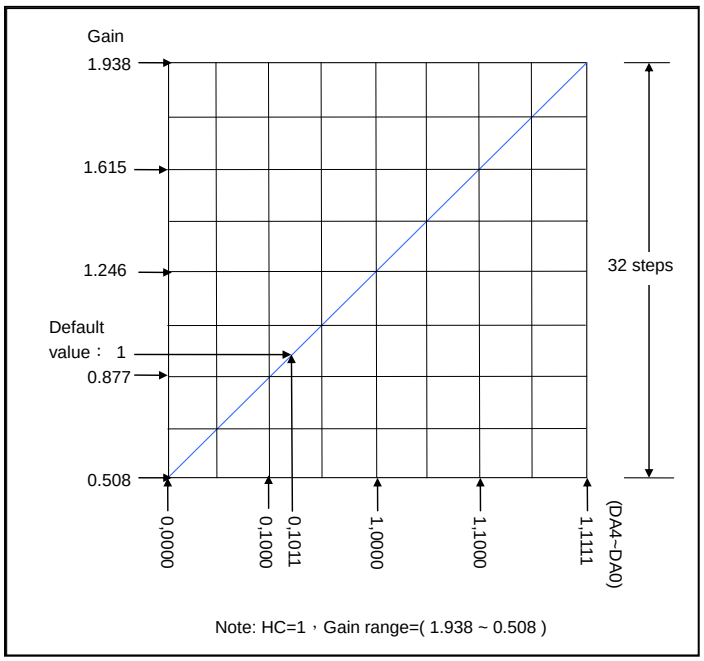

Figure 2

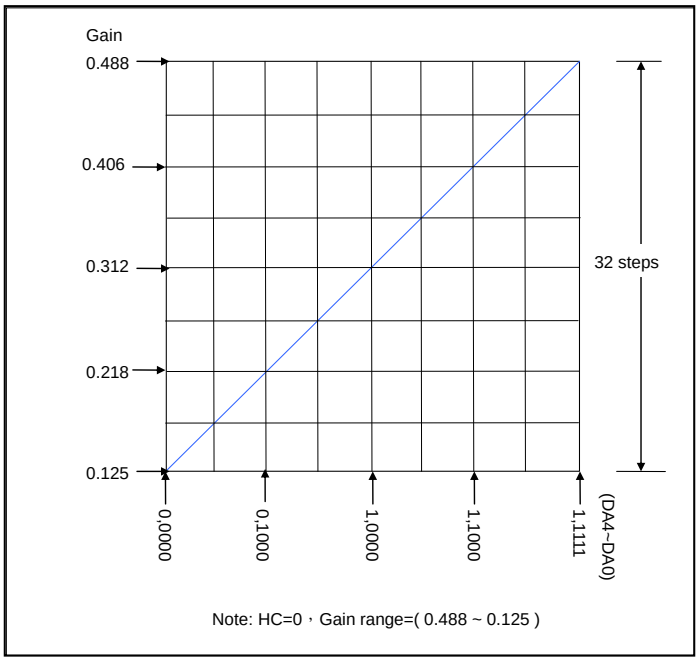
Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$=0.61VoltxG; $I_{OUT}$=($V_{R\text{-}EXT}$/$R_{ext}$)x23

Whereas $R_{ext}$ is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit9 – bit4 of the configuration register. The default value of G is 1. For your information, the output current is about 2mA when $R_{ext}$=7KΩ and 25mA when $R_{ext}$=560Ω if G is set to default value 1. The formula and setting for G are described in next section.

## Current Gain Adjustment




The bit 9 to bit 4 of the configuration register set the gain of output current, i.e., G. As totally 6-bit in number, i.e., ranged from 6'b000000 to 6'b111111, these bits allow the user to set the output current gain up to 64 levels. These bits can be further defined inside Configuration Register as follows:

| F | E | D | C | B | A | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | HC | DA4 | DA3 | DA2 | DA1 | DA0 | - | - | - | - |

1. Bit 9 is HC bit. The setting is in low current band when HC=0, and in high current band when HC=1.
2. Bit 8 to bit 4 are DA4 ~ DA0.

The relationship between these bits and current gain G is:

HC=1, D=(65xG-33)/3

HC=0, D=(256xG-32)/3

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

$D= DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0$

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 5-bit mantissa DA4~DA0.

For example,

HC=1, G=1.246, D=(65x1.246-33)/3=16

the D in binary form would be:

$D=16=1x2^4+0x2^3+0x2^2+0x2^1+0x2^0$

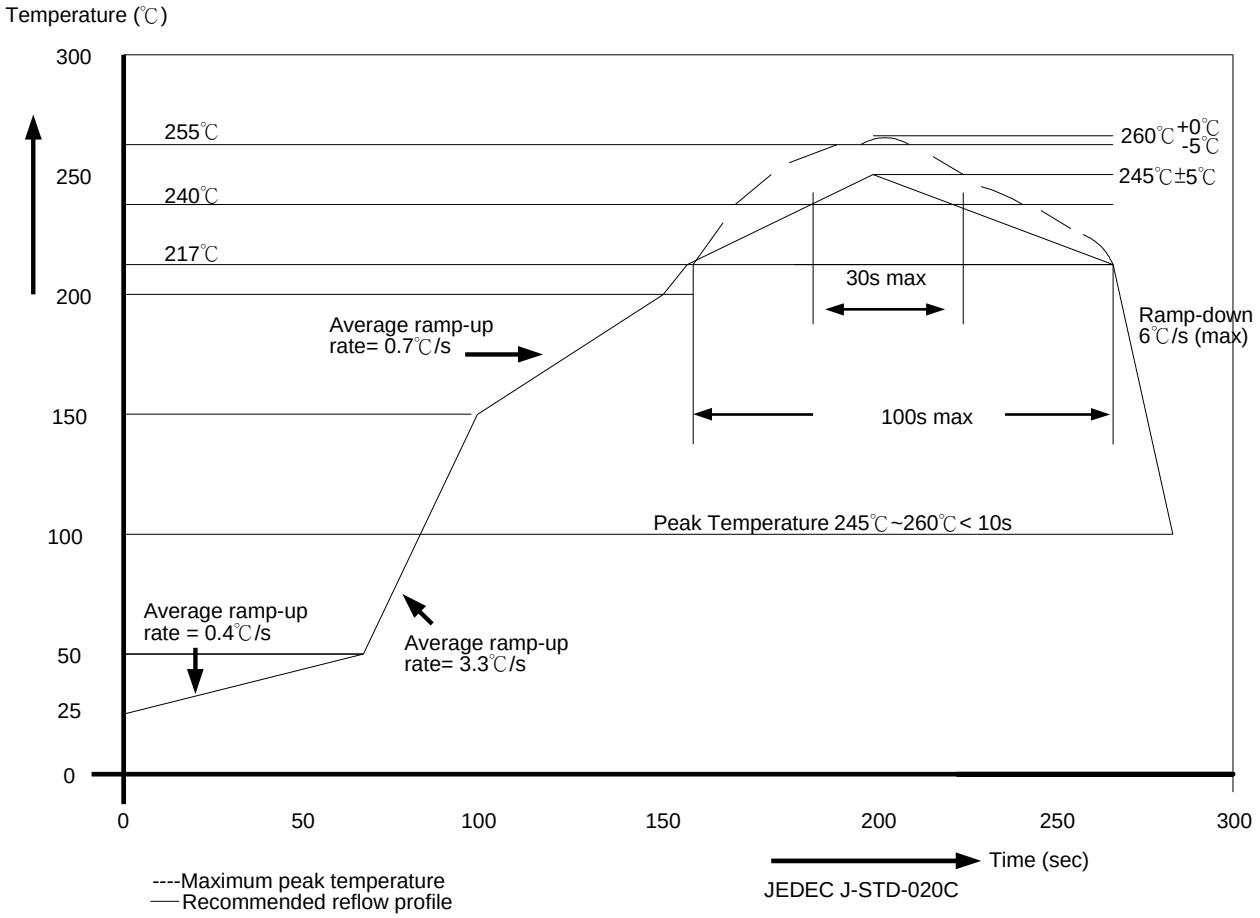
The 6 bits (bit 5~bit 0) of the configuration register are set to 6'b110000.

## Staggered Delay of Output

MBI5041 has a built-in staggered circuit to perform delay mechanism. Among output ports exist a graduated 5ns delay time among $\overline{OUT\,4n}$ , $\overline{OUT\,4n+1}$ , $\overline{OUT\,4n+2}$ , and $\overline{OUT\,4n+3}$ , by which the output ports will be divided to four groups at a different time so that the instant current from the power line will be lowered.

## Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defined "Pb-Free & Green " to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to reflow processes which adopt tin/lead (SnPb) solder paste. Please refer to JEDEC J-STD-020C for temperature setting. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.




| Package Thickness | Volume mm$^3$ <350 | Volume mm$^3$ 350-2000 | Volume mm$^3$ ≧2000 |
|---|---|---|---|
| <1.6mm | 260 +0 °C | 260 +0 °C | 260 +0 °C |
| 1.6mm – 2.5mm | 260 +0 °C | 250 +0 °C | 245 +0 °C |
| ≧2.5mm | 250 +0 °C | 245 +0 °C | 245 +0 °C |

*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

## Package Power Dissipation (PD)

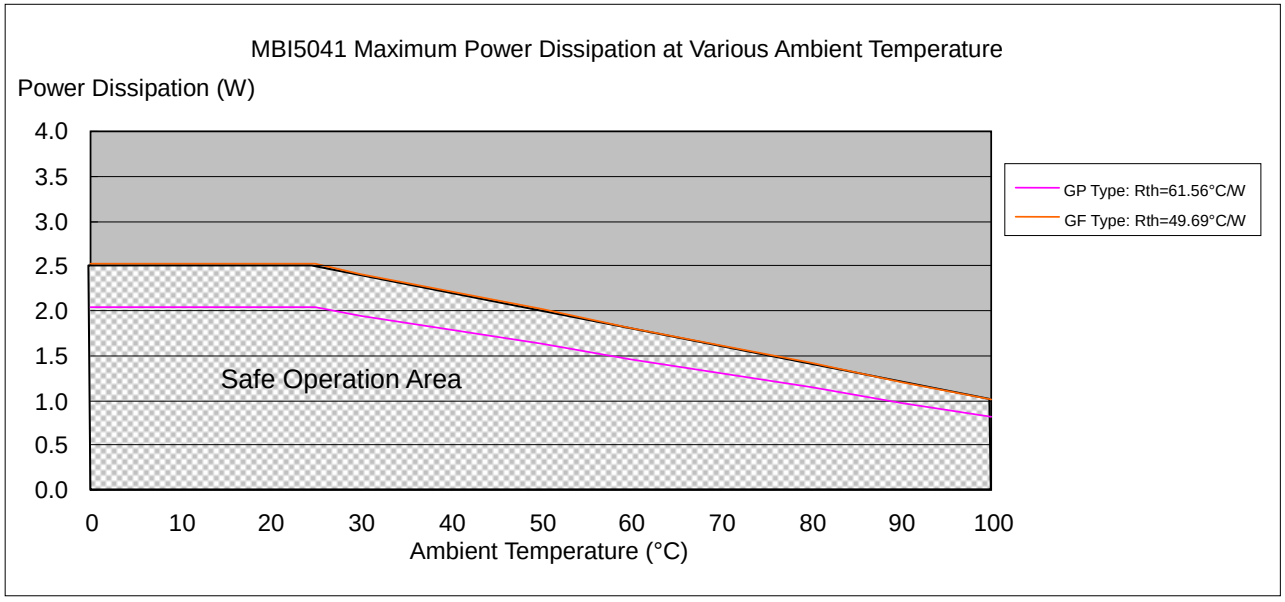
The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.

Please see the follow table for $P_D$ and $R_{th(j-a)}$ for different package

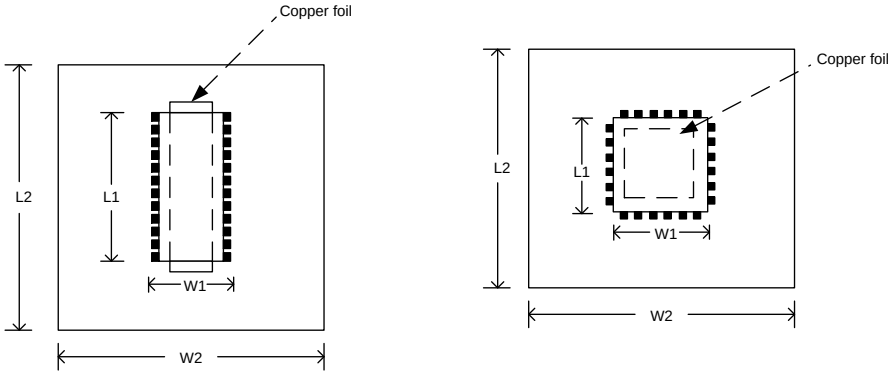
| Device Type | $R_{th(j-a)}$(°C/W) | $P_D$(W) |
|---|---|---|
| GF | 49.69 | 2.52 |
| GP | 61.56 | 2.03 |

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.



## Usage of Thermal Pad

The PCB area L2xW2 is 4 times of the IC's area L1xW1.The thickness of the PCB is 1.6mm, copper foil 1 Oz. The thermal pad on the IC's bottom has to be mounted on the copper foil.

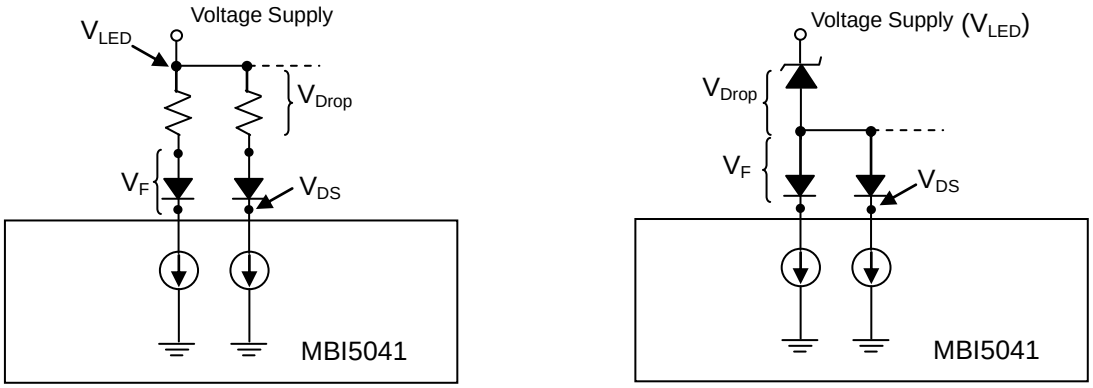



## LED Supply Voltage ($V_{LED}$)

MBI5041 are designed to operate with $V_{DS}$ ranging from 0.4V to 1.0V (depending on $I_{OUT}$=2~30mA) considering the package power dissipating limits. $V_{DS}$ may be higher enough to make $P_{D\ (act)} > P_{D\ (max)}$ when $V_{LED}$=5V and $V_{DS}=V_{LED}-V_F$, in which $V_{LED}$ is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, $V_{DROP}$.

A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

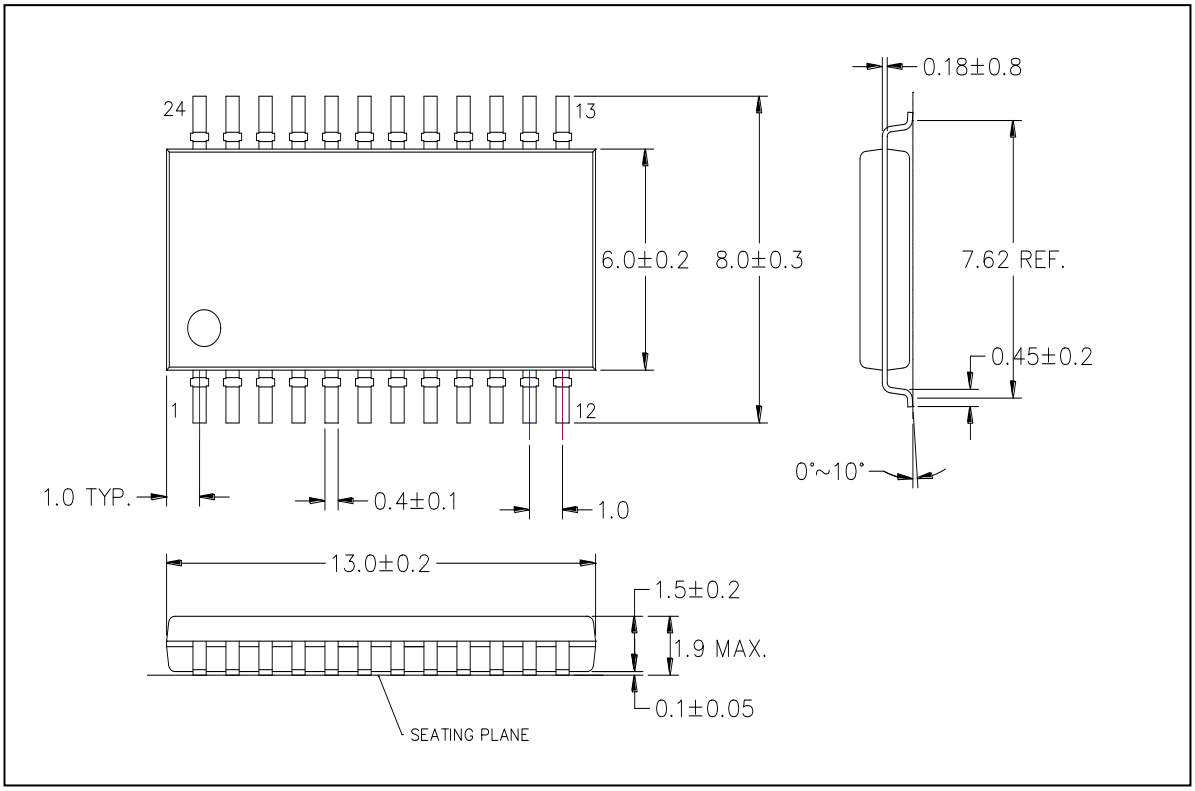
Resistors or Zener diode can be used in the applications as shown in the following figures.




## Switching Noise Reduction

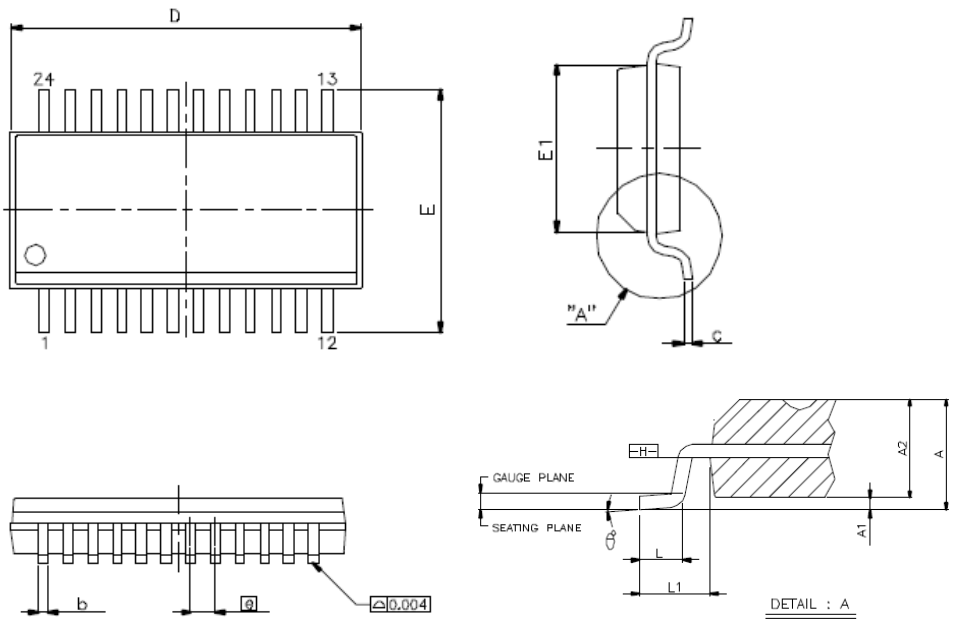
LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to "Application Note for 8-bit and 16-bit LED Drivers- Overshoot".

## Package Outline




MBI5041GF Outline Drawing

Note: The unit for the outline drawing is mm.

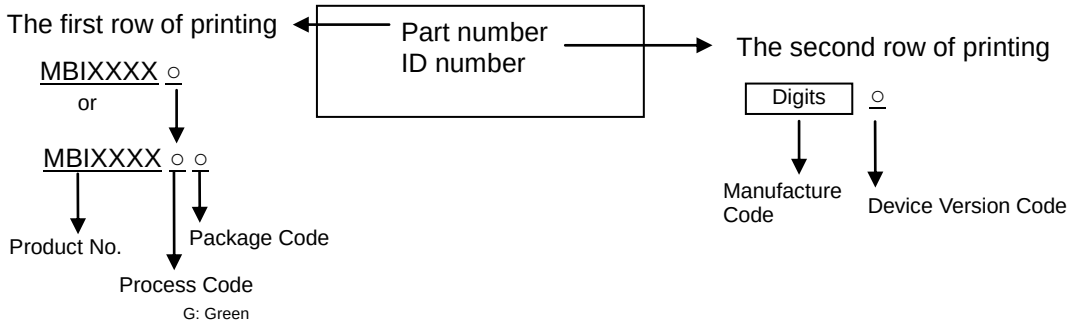



| SYMBOLS | Dimensions shown in inchs | | | Dimensions shown in millimeters | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.053 | 0.064 | 0.069 | 1.346 | 1.626 | 1.753 |
| A1 | 0.004 | 0.006 | 0.010 | 0.102 | 0.152 | 0.254 |
| A2 | — | — | 0.059 | — | — | 1.499 |
| D | 0.337 | 0.341 | 0.344 | 8.560 | 8.661 | 8.738 |
| E | 0.228 | 0.236 | 0.244 | 5.791 | 5.994 | 6.198 |
| E1 | 0.150 | 0.154 | 0.157 | 3.810 | 3.912 | 3.988 |
| b | 0.008 | — | 0.012 | 0.203 | — | 0.305 |
| c | 0.007 | — | 0.010 | 0.178 | — | 0.254 |
| L | 0.016 | 0.025 | 0.050 | 0.406 | 0.635 | 1.270 |
| e | 0.025 BASIC | | | 0.635 BASIC | | |
| L1 | 0.041 BASIC | | | 1.0414 BASIC | | |
| θ° | 0 | — | 8 | 0 | — | 8 |

MBI5041GF Outline Drawing

Note: The unit for the outline drawing is mm.

## Product Top Mark Information




## Product Revision History

| Datasheet version | Device Version Code |
|---|---|
| V1.00 | A |

## Product Ordering Information

| Part Number | RoHS Compliant Package Type | Weight (g) |
|---|---|---|
| MBI5041GF | SOP24-300-1.00 | 0.30 |
| MBI5041GP | SSOP24-150-0.64 | 0.11 |

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