High Performance 1A LDO

ISL80101

The ISL80101 ia a low-voltage, high-current, single output LDO specified for 1A output current. This part operates from input voltages of 2.2V to 6V and is capable of providing output voltages of 0.8V to 5V on the adjustable V_{OUT} versions. Fixed output voltage options available in 0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5V. Other custom voltage options available upon request.

For applications that demand in-rush current less than current limit or a longer delay for a valid V_{OUT}, an external capacitor on the soft-start pin provides adjustment. A supply independent ENABLE signal allows the part to be placed into a low quiescent current shutdown mode. Sub-micron CMOS process is utilized for this product family to deliver best in class analog performance and overall value.

This CMOS LDO will consume significantly lower quiescent current as a function of load over bipolar LDOs, which translates into higher efficiency and the ability to consider packages with smaller footprints. Quiescent current is modestly compromised to enable leading class fast load transient response and hence total AC regulation band for an LDO in this category.

Applications* (see page 14)

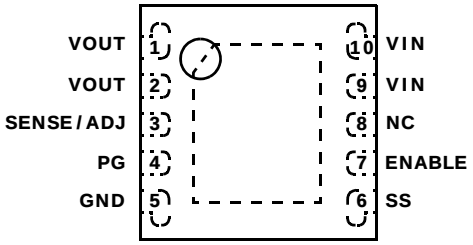
- DSP, FPGA and µP Core Power Supplies
- Noise-Sensitive Instrumentation Systems
- Post Regulation of Switched Mode Power Supplies
- Industrial Systems
- Medical Equipment
- Telecommunications and Networking Equipment
- Servers
- Hard Disk Drives (HD/HDD)

Features

- 0.2% initial V_{OUT} Accuracy
- Designed for 2.2V to 6V Input Supply
- Dropout Typically 130mV at 1A
- Fast Load Transient Response
- Rated Output Current Options of 1A
- Adjustable In-Rush Current Limiting
- Fixed and Adjustable V_{OUT} Options Available
- 58dB Typical PSRR
- Output Noise of 100µV_{RMS} between 300Hz to 300kHz
- PG Feature
- 1V Enable Input Threshold
- Short-Circuit Current Protection
- 1A Peak Reverse Current
- Over-Temperature Shutdown
- Any Cap Stable with Minimum 10µF Ceramic
- ±1.8% Guaranteed V_{OUT} Accuracy for Junction Temperature Range from -40°C to +125°C
- Available in a 10 Ld DFN Package and soon to follow TO220-5, TO263-5 and SOT223-5
- Pb-Free (RoHS Compliant)

Pin Configuration

ISL80101
(10 LD 3X3 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	VOUT	Output voltage pin.
3	SENSE/ADJ	Remote voltage sense for internally fixed V_{OUT} options. ADJ pin for externally set V_{OUT}.
4	PG	V_{OUT} in regulation signal. Logic low defines when V_{OUT} is not in regulation. Pin should be grounded if not used.
5	GND	GND pin.
6	SS	External cap controls the rate of the V_{OUT} ramp.
7	ENABLE	V_{IN} independent chip enable. TTL and CMOS compatible.
8	DNC	Do not connect this pin to ground or supply. Leave floating.
9, 10	VIN	Input supply pin.

Ordering Information

PART NUMBER (Notes 4, 5)	PART MARKING	VOUT VOLTAGE (Note 3)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #
ISL80101IRAJZ (Note 1)	DZAB	ADJ	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR08Z	DZBB	0.8V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR08Z-T (Note 2)	DZBB	0.8V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR12Z	DZCB	1.2V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR12Z-T (Note 2)	DZCB	1.2V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR15Z	DZDB	1.5V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR15Z-T (Note 2)	DZDB	1.5V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR18Z (Note 1)	DZEB	1.8V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR25Z (Note 1)	DZFB	2.5V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR33Z	DZGB	3.3V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR33Z-T (Note 2)	DZGB	3.3V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR50Z	DZHB	5.0V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR50Z-T (Note 2)	DZHB	5.0V	-40 to +125	10 Ld 3x3 DFN	L10.3x3

NOTES:

1. Add “-T” or “TK” for Tape and Reel. Please refer to TB347 for details on reel specifications.
2. Please refer to TB347 for details on reel specifications.
3. For other output voltages, contact Intersil Marketing.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), please see device information page for ISL80101. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

VIN relative to GND (Note 6) . . . . . -0.3V to +6.5V
VOUT relative to GND (Note 6) . . . . . -0.3V to +6.5V
PG, ENABLE, SENSE/ADJ, SS
Relative to GND (Note 6) . . . . . -0.3V to +6.5V

Recommended Operating Conditions

(Notes 9, 10)

Junction Temperature Range (TJ) (Note 9) . -40°C to +125°C
VIN relative to GND . . . . . 2.2V to 6V
VOUT range . . . . . 800mV to 5V
PG, ENABLE, SENSE/ADJ, SS relative to GND . . . . 0V to +6V
PG Sink Current . . . . . <10mA

Thermal Information

Thermal Resistance . . . . . θJA (°C/W) θJC (°C/W)
10 Ld DFN Package (Notes 7, 8) . . 45 4
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. ABS max voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
8. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
9. Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.
10. Electromigration specification defined as lifetime average junction temperature of +110°C where max rated DC current = lifetime average current.

Electrical Specifications

Unless otherwise noted, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25°C$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to Applications section of the datasheet and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
DC CHARACTERISTICS						
DC Ouput Voltage Accuracy	V_{OUT}	V_{OUT} Options: 0.8V, 1.2V, 1.5V and 1.8V				
		$2.2V \le V_{IN} < 3.6V$; $0A < I_{LOAD} \le 1A$	**-1.8**	0.2	**1.8**	%
		V_{OUT} Options: 2.5V, 3.3V and 5.0V				
		$V_{OUT} + 0.4V \le V_{IN} \le 6V$; $0A < I_{LOAD} < 1A$	**-1.8**	0.2	**1.8**	%
Feedback Pin (ADJ Option Only)	V_{ADJ}	$2.2V \le V_{IN} \le 6V$, $0A < I_{LOAD} < 1A$	**491**	500	**509**	mV
DC Input Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$V_{OUT} + 0.5V < V_{IN} < 5V$			**1**	%
DC Output Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	$0A < I_{LOAD} < 1A$, All voltage options	**-1**			%
Feedback Input Current		$V_{ADJ} = 0.5V$		0.01	1	µA
Ground Pin Current	I_Q	$I_{LOAD} = 0A$, $2.2V < V_{IN} < 6V$		3	**5**	mA
		$I_{LOAD} = 1A$, $2.2V < V_{IN} < 6V$		5	**7**	mA
Ground Pin Current in Shutdown	I_{SHDN}	ENABLE Pin = 0.2V, $V_{IN} = 6V$		0.2	**12**	µA
Dropout Voltage (Note 12)	V_{DO}	$I_{LOAD} = 1A$, $V_{OUT} = 2.5V$		130	**212**	mV
Output Short Circuit Current (1A Version)	OCP	$V_{OUT} = 0V$, $2.2V < V_{IN} < 6V$		1.75		A
Thermal Shutdown Temperature	TSD	$2.2V < V_{IN} < 6V$		160		°C

Electrical Specifications Unless otherwise noted, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25°C$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to Applications section of the datasheet and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
Thermal Shutdown Hysteresis (Rising Threshold)	TSDn	$2.2V < V_{IN} < 6V$		30		°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	f = 1kHz, I_{LOAD} = 1A; V_{IN} = 2.2V		58		dB
		f = 120Hz, I_{LOAD} = 1A; V_{IN} = 2.2V		72		dB
Output Noise Voltage		I_{LOAD} = 10mA, BW = 300Hz < f < 300kHz		100		μV_{RMS}
ENABLE PIN CHARACTERISTICS						
Turn-on Threshold		$2.2V < V_{IN} < 6V$	**0.3**	0.8	**1**	V
Hysteresis (Rising Threshold)		$2.2V < V_{OUT} + 0.4V < 6V$	**10**	80	**200**	mV
Enable Pin Turn-on Delay		$C_{OUT} = 10\mu F$, I_{LOAD} = 1A		100		µs
Enable Pin Leakage Current		V_{IN} = 6V, EN = 3V			**1**	µA
ADJUSTABLE INRUSH CURRENT LIMIT CHARACTERISTICS						
Current limit adjust	I_{PD}	V_{IN} = 3.5V, EN = 0V, SS = 1V	**0.5**	1	**1.3**	mA
	I_{CHG}		**-3.3**	-2	**-0.8**	µA
PG PIN CHARACTERISTICS						
V_{OUT} PG Flag Threshold			**75**	85	**92**	$\%V_{OUT}$
V_{OUT} PG Flag Hysteresis				4		%
PG Flag Low Voltage		V_{IN} = 2.5V, $I_{SINK} = 500\mu A$			**100**	mV
PG Flag Leakage Current		V_{IN} = 6V, PG = 6V			**1**	µA

NOTES:

11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

12. Dropout is defined by the difference in supply V_{IN} and V_{OUT} when the supply produces a 2% drop in VOUT from its nominal value.

Typical Application Diagrams

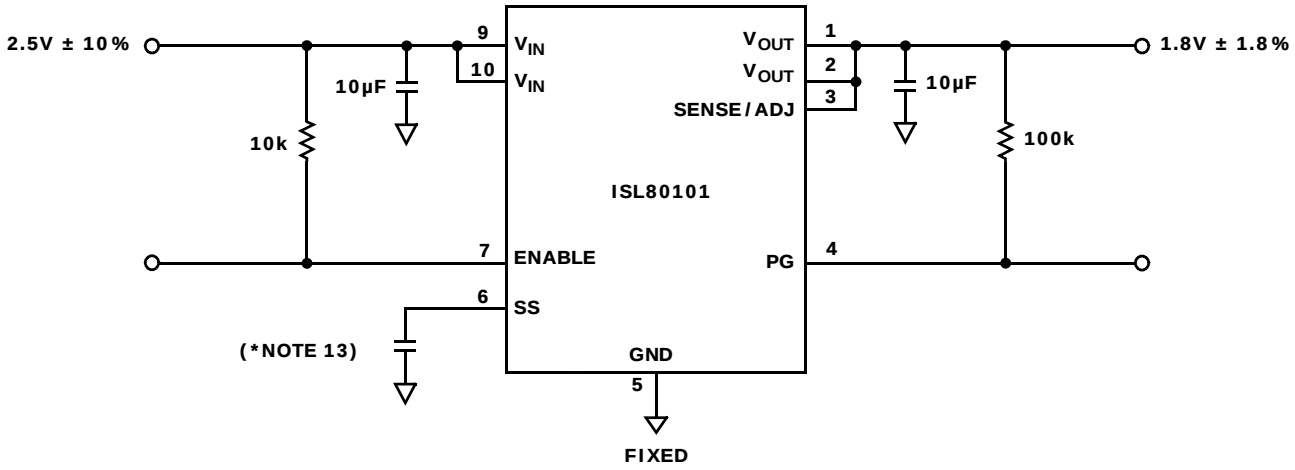


FIGURE 1. FIXED TYPICAL APPLICATION DIAGRAM

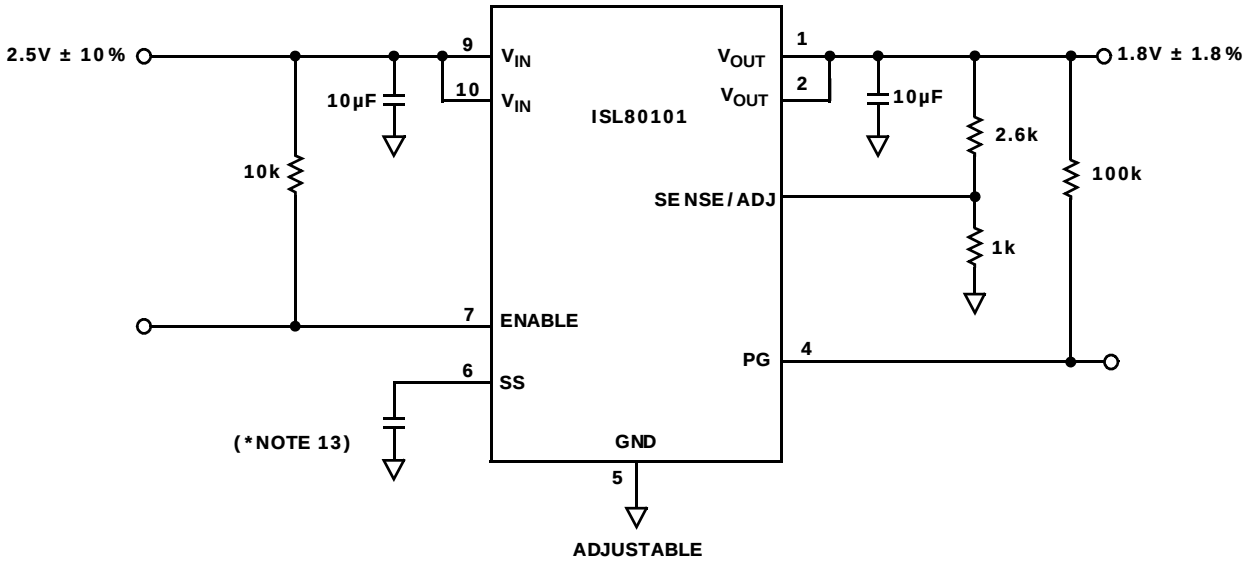
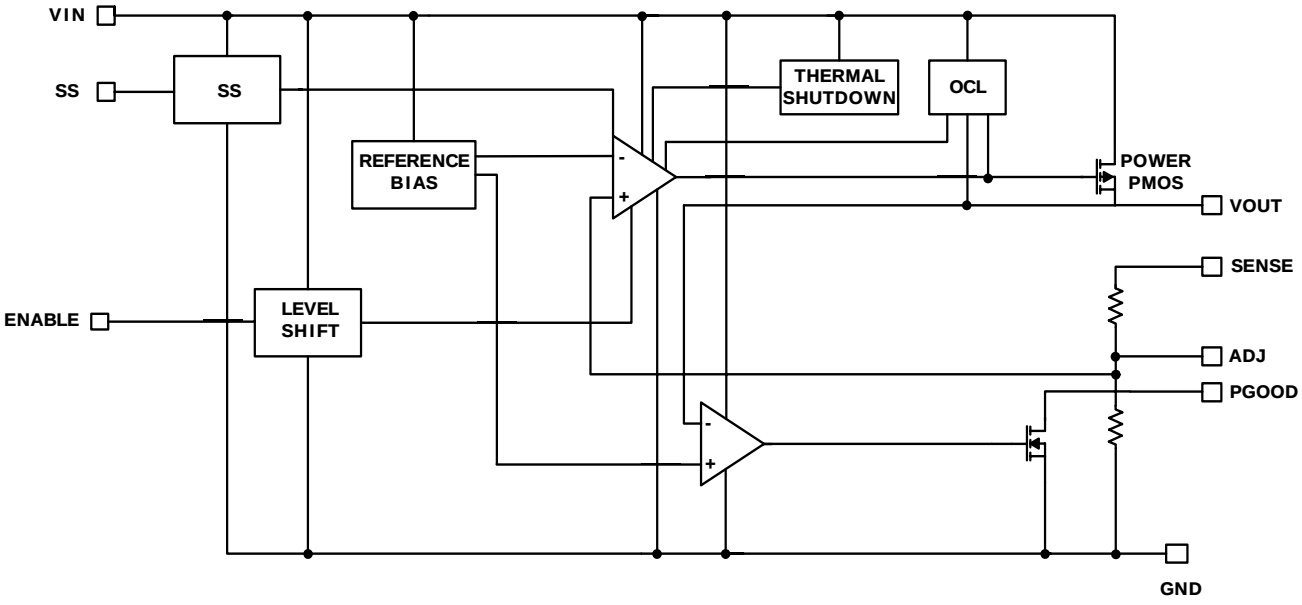


FIGURE 2. ADJUSTABLE TYPICAL APPLICATION DIAGRAM

NOTE:

13. Used when large bulk capacitance required on V_{OUT} for application.

ISL80101 Schematic Block Diagram



Application Section

Input Voltage Requirements

Despite other output voltages offered, this family of LDOs is optimized for a true 2.5V to 1.8V conversion where the input supply can have a tolerance of as much as ±10% for conditions noted in the “Electrical Specifications” table on page 3. Minimum guaranteed input voltage is 2.2V. However, due to the nature of an LDO, V_{IN} must be some margin higher than the output voltage plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The Dropout spec of this family of LDOs has been generously specified in order to allow applications to design for a level of efficiency that can accommodate the smaller outline package for those applications that cannot accommodate the profile of the TO220/263.

External Capacitor Requirements

GENERAL GUIDELINE

External capacitors are required for proper operation. Careful attention must be paid to layout guidelines and selection of capacitor type and value to ensure optimal performance.

OUTPUT CAPACITOR

The required minimum output capacitor is 10µF X5R/X7R to ensure stable operation. Additional capacitors of any value in Ceramic, POSCAP or Alum/Tantalum Electrolytic types may be placed in parallel to improve PSRR at higher frequencies and/or load transient AC output voltage tolerances. This minimum capacitor must be connected to V_{OUT} and Ground pins of the LDO with PCB traces no longer than 0.5cm.

INPUT CAPACITOR

The minimum input capacitor required for proper operation is 10µF having a ceramic dielectric. This minimum capacitor must be connected to V_{OUT} and Ground pins of the LDO with PCB traces no longer than 0.5cm.

Thermal Fault Protection

In the event the die temperature exceeds typically +160°C, then the output of the LDO will shut down until the die temperature can cool down to typically +130°C. The level of power combined with the thermal resistance of the package (+45°C/W for DFN) will determine if the junction temperature exceeds the thermal shutdown temperature specified in the “Electrical Specifications” table on page 3 (see thermal packaging guidelines).

Current Limit Protection

The ISL80101 LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The current limit circuit performs as a constant current source when the output current exceeds the current limit threshold noted in the “Electrical Specifications” table on page 3. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage mode regulation. In the event of an overload condition on the DFN package the LDO will begin to cycle on and off due to the die temperature exceeding thermal fault condition. The TO220/263 package will tolerate higher levels of power dissipation on the die which may never thermal cycle if the heatsink of this larger package can keep the die temperature below the specified typical thermal shutdown temperature.

Functional Description

Enable Operation

The Enable turn-on threshold is typically 0.8V with a hysteresis of 80mV. The Enable pin doesn't have an internal pull-up or pull-down resistor. As a result, this pin must not be left floating. This pin must be tied to V_{IN} if it is not used. A pull-up resistor (typically 1kΩ to 10kΩ) will be required for applications that use open collector or open drain outputs to control the Enable pin. The Enable pin may be connected directly to V_{IN} for applications that are always on.

Soft-Start Operation

The soft-start circuit controls the rate at which the output voltage comes up to regulation at power-up or coming out of a chip disable. A constant current charges an external soft-start capacitor. The external capacitor always gets discharged to 0V at start-up of after coming out of a chip disable. The discharge rate is the RC time constant of an internal resistance and C_{SS}. The soft-start function effectively limits the amount of in-rush current below the programmed current limit during start-up or an enable sequence to avoid an overcurrent fault condition. This can be an issue for applications that require large, external bulk capacitances on V_{OUT} where high levels of charging current can be seen for a significant period of time. High in-rush currents can cause V_{IN} to drop below minimum which could cause V_{OUT} to shutdown. Equation 3 can be used to calculate C_{SS} for a desired in-rush current. Where V_{OUT} is the output voltage, C_{OUT} is the total capacitance on the output and I_{INRUSH} is the desired in-rush current.

$$C_{SS} = \frac{(V_{OUT} x C_{OUT} x 2\mu A))}{I_{INRUSH} x 0.5V} \quad \text{(EQ. 1)}$$

The following scope in Figure 3 captures the response for the soft-start function.The output voltage is set to 1.8V.

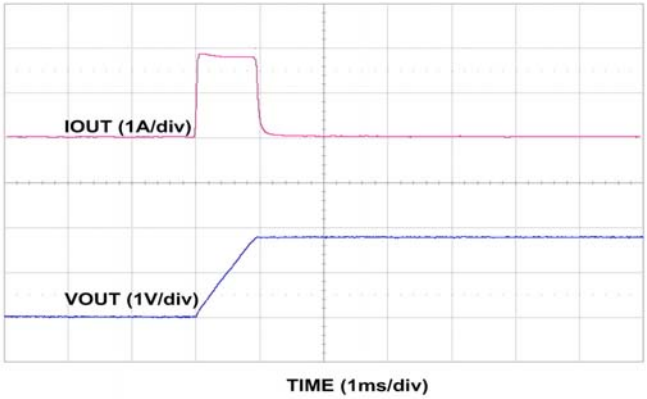


FIGURE 3. IN-RUSH CURRENT WITH NO C_{SS}, C_{OUT} = 1000µF, IN-RUSH CURRENT = 1.8A

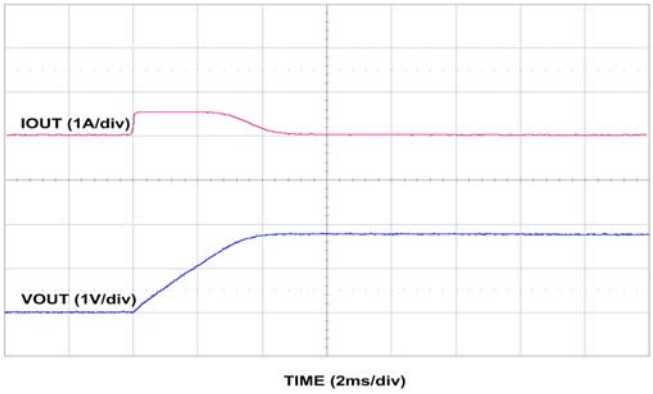


FIGURE 4. IN-RUSH CURRENT WITH C_{SS} = 15nF, C_{OUT} = 1000µF, IN-RUSH CURRENT = 0.5A

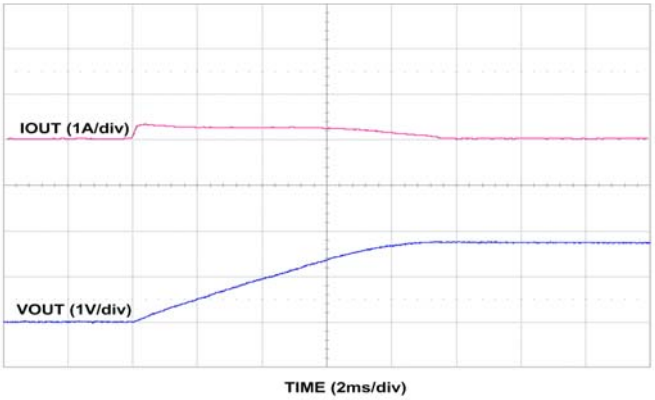


FIGURE 5. IN-RUSH CURRENT WITH C_{SS} = 33nF, C_{OUT} = 1000µF, IN-RUSH CURRENT = 0.2A

The rise time of the regulator output voltage for a given C_{SS} value can be calculated using Equation 2.

$$t_{RAMP} = \frac{C_{SS} x 0.5V}{2\mu A} \quad \text{(EQ. 2)}$$

Power-Good Operation

The PGOOD circuit monitors V_{OUT} and signals a fault condition when V_{OUT} is below 85% of the nominal output voltage. The PGOOD flag is an open-drain NMOS that can sink 10mA during a fault condition. The PGOOD pin requires an external pull up resistor which is typically connected to the VOUT pin. The PGOOD pin should not be pulled up to a voltage source greater than V_{IN}. During a fault condition, the PGOOD output is pulled low. The PGOOD fault can be caused by the current limit fault or low input voltage. The PGOOD does not function during thermal shutdown and when the part is disabled.

Output Voltage Selection

An external resistor divider is used to scale the output voltage relative to the internal reference voltage. This voltage is then fed back to the error amplifier. The output voltage can be programmed to any level between 0.8V and 5V. An external resistor divider, R_1 and R_2, is used to set the output voltage as shown in Equation 3. The recommended value for R_2 is 500Ω to 1kΩ. R_1 is then chosen according to Equation 4:

$$V_{OUT} = 0.5V \times \left(\frac{R_1}{R_2} + 1\right) \quad \text{(EQ. 3)}$$

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.5V} - 1\right) \quad \text{(EQ. 4)}$$

Power Dissipation

The junction temperature must not exceed the range specified in the Recommended Operating Conditions. The power dissipation can be calculated by using Equation 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 5)}$$

The maximum allowed junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ will determine the maximum allowed junction temperature rise (ΔT_J) as shown in Equation 6:

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad \text{(EQ. 6)}$$

To calculate the maximum ambient operating temperature, use the junction-to-ambient thermal resistance (θ_{JA}) for the DFN package with Equation 5:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 7)}$$

Substitute P_D for $P_{D(MAX)}$ and the maximum ambient operating temperature can be found by solving for T_A using Equation 8:

$$T_A = T_{JMAX} - P_{D(MAX)} \times \theta_{JA} \quad \text{(EQ. 8)}$$

Heatsinking The DFN Package

The DFN package uses the copper area on the PCB as a heat-sink. The EPAD of this package must be soldered to the copper plane (GND plane) for heat sinking. Figure 6 shows a curve for the θ_{JA} of the DFN package for different copper area sizes.

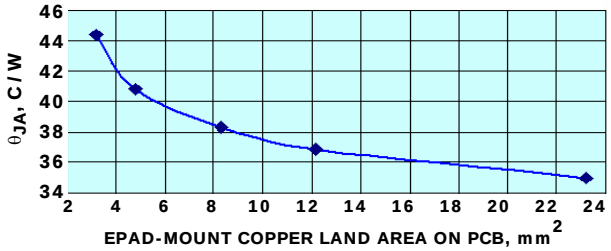


FIGURE 6. 3mmx3mm-10 PIN DFN ON 4-LAYER PCB WITH THERMAL VIAS θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A.

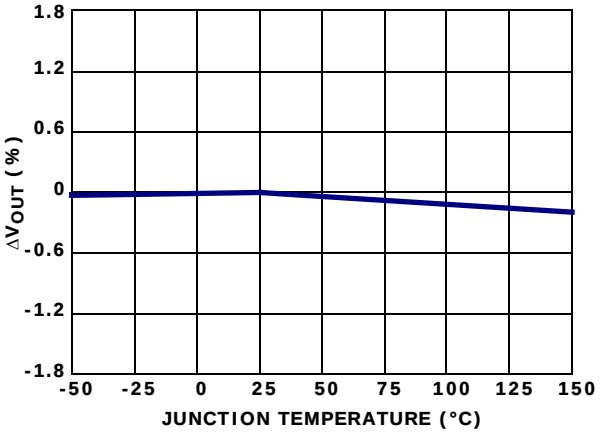


FIGURE 7. OUTPUT VOLTAGE vs TEMPERATURE

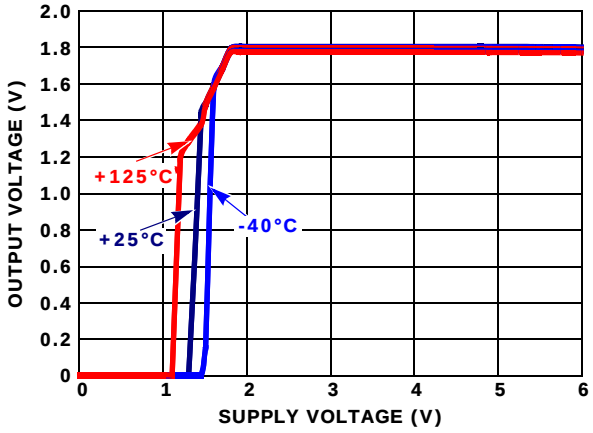


FIGURE 8. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

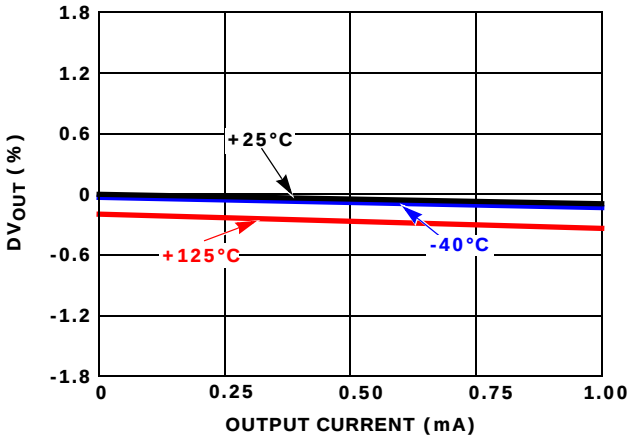


FIGURE 9. OUTPUT VOLTAGE vs OUTPUT CURRENT

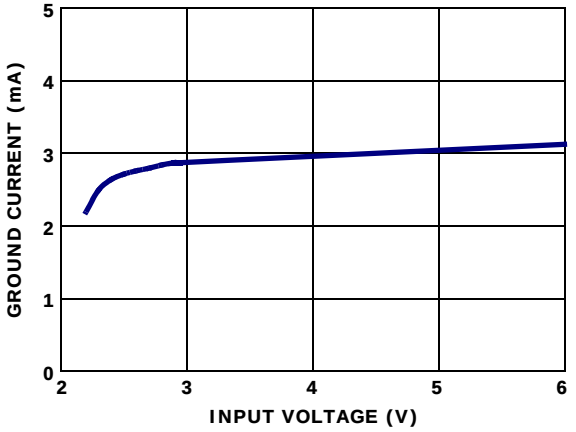


FIGURE 10. GROUND CURRENT vs SUPPLY VOLTAGE

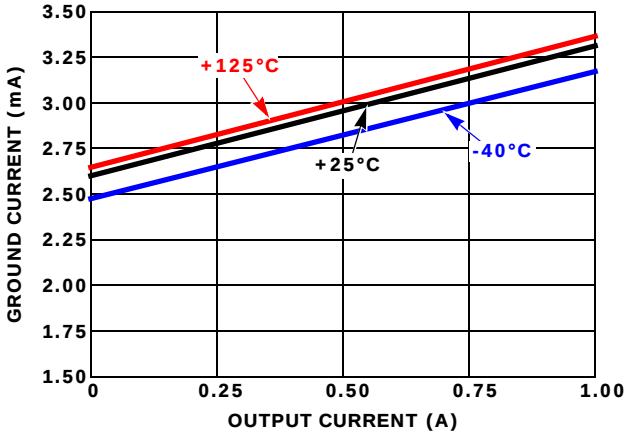


FIGURE 11. GROUND CURRENT vs OUTPUT CURRENT

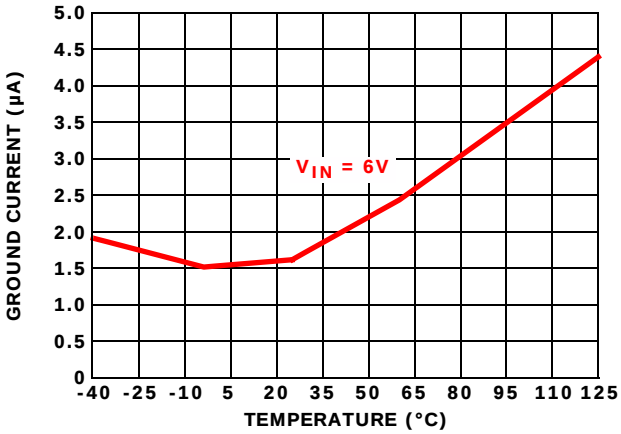


FIGURE 12. SHUTDOWN CURRENT vs TEMPERATURE

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

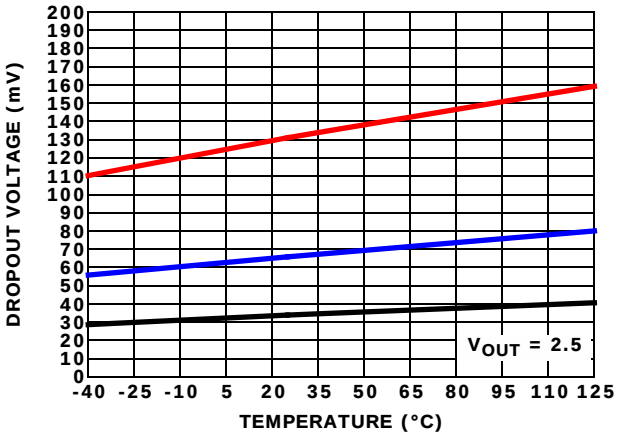


FIGURE 13. DROPOUT VOLTAGE vs TEMPERATURE

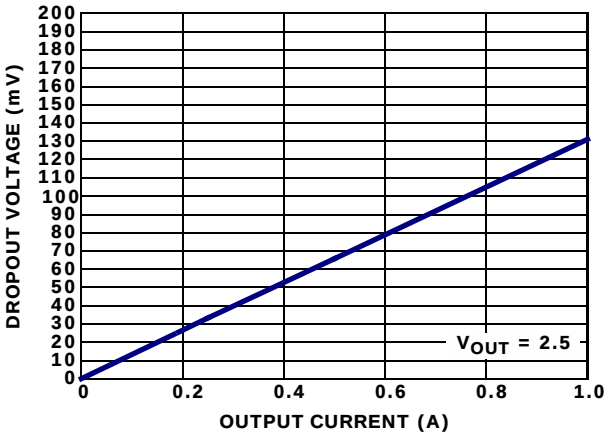


FIGURE 14. DROPOUT VOLTAGE vs OUTPUT CURRENT

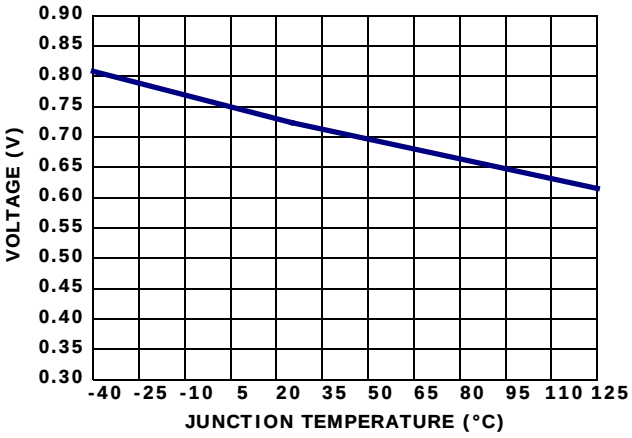


FIGURE 15. ENABLE THRESHOLD VOLTAGE vs TEMPERATURE

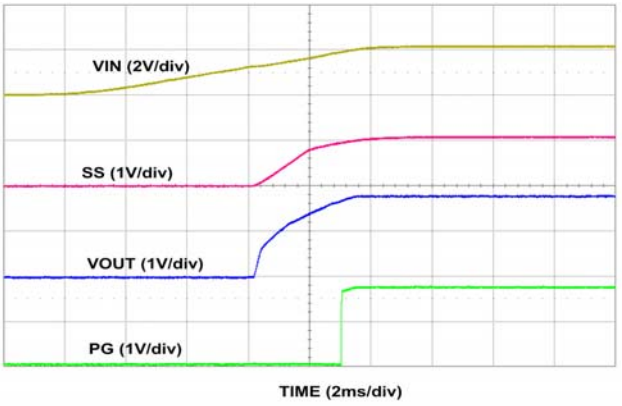


FIGURE 16. POWER-UP (V_{IN} = 2.2V)

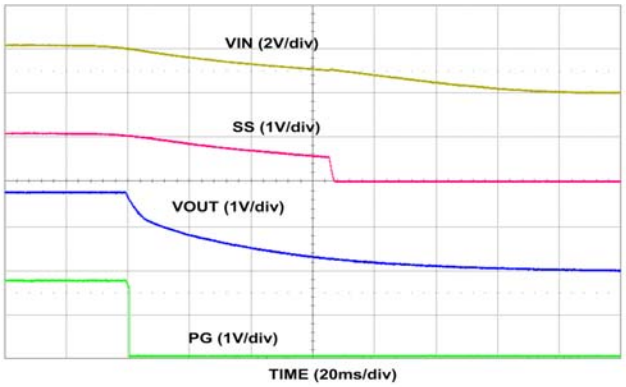


FIGURE 17. POWER-DOWN (V_{IN} = 2.2V)

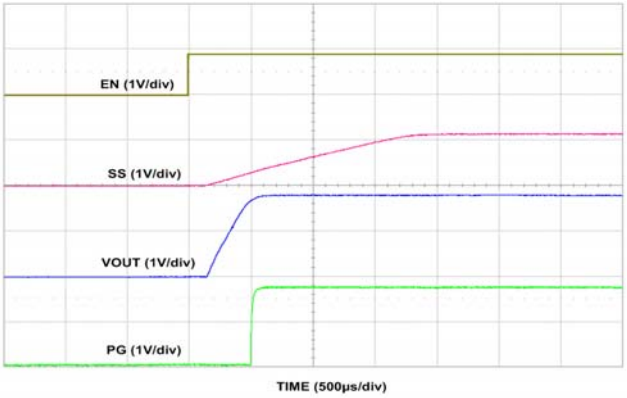


FIGURE 18. ENABLE START-UP

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

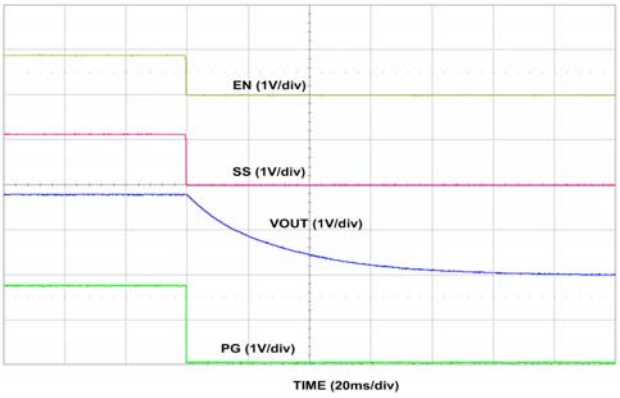


FIGURE 19. ENABLE SHUTDOWN

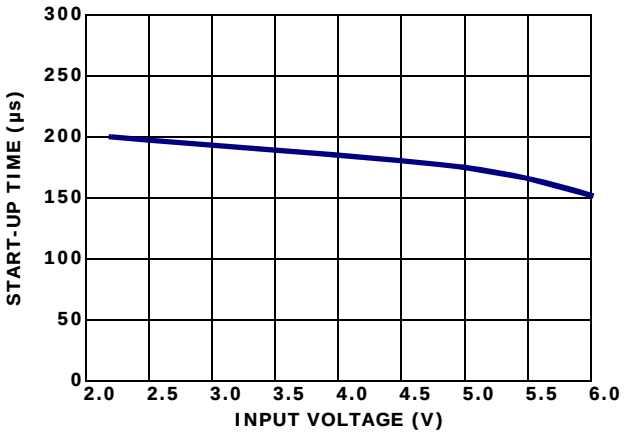


FIGURE 20. START-UP TIME vs SUPPLY VOLTAGE

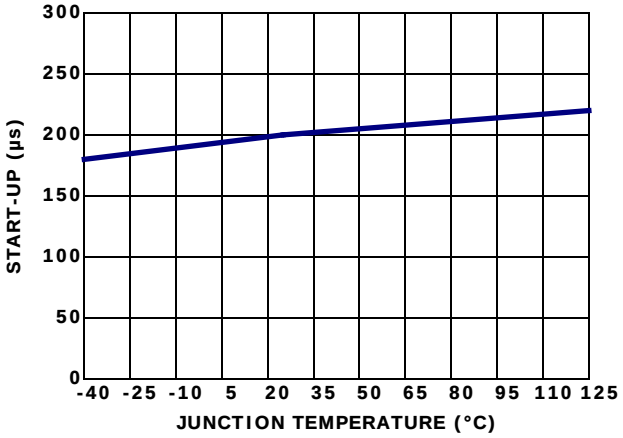


FIGURE 21. START-UP TIME vs TEMPERATURE

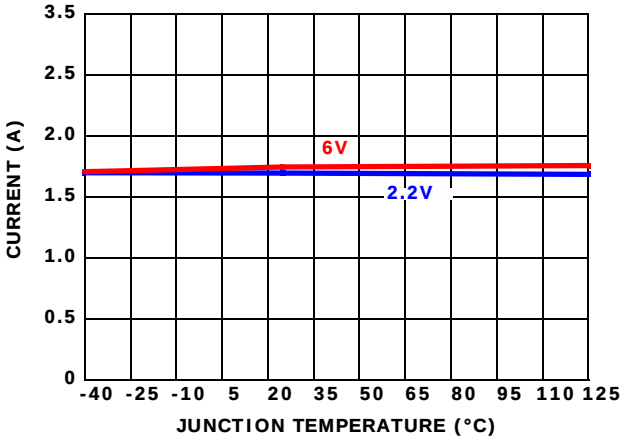


FIGURE 22. CURRENT LIMIT vs TEMPERATURE

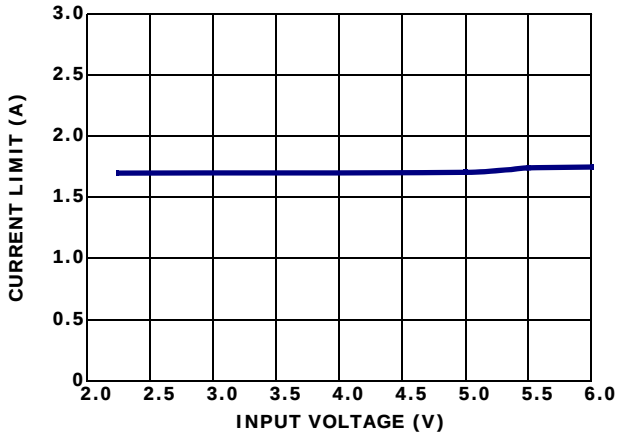


FIGURE 23. CURRENT LIMIT vs SUPPLY VOLTAGE

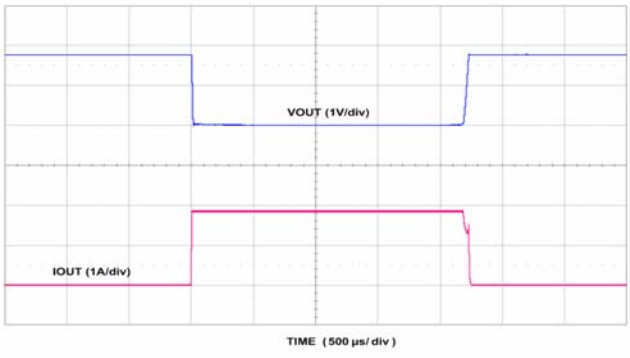


FIGURE 24. CURRENT LIMIT RESPONSE

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

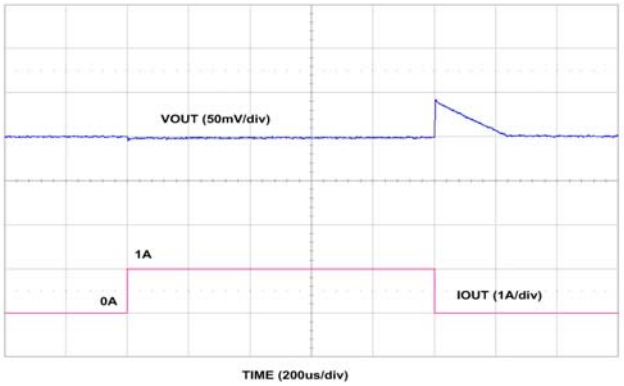


FIGURE 25. LOAD TRANSIENT 0A TO 1A, C_{OUT} = 10µF CERAMIC

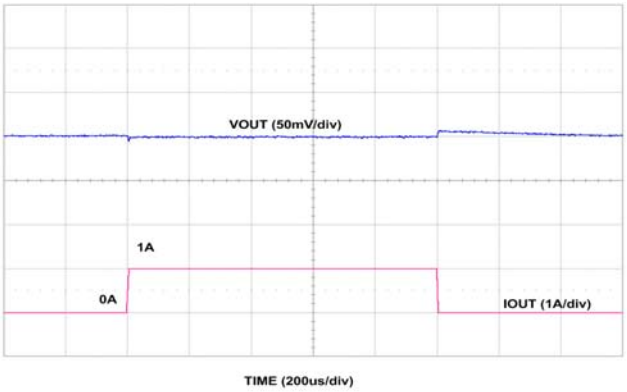


FIGURE 26. LOAD TRANSIENT 0A TO 1A, C_{OUT} = 100µF CERAMIC

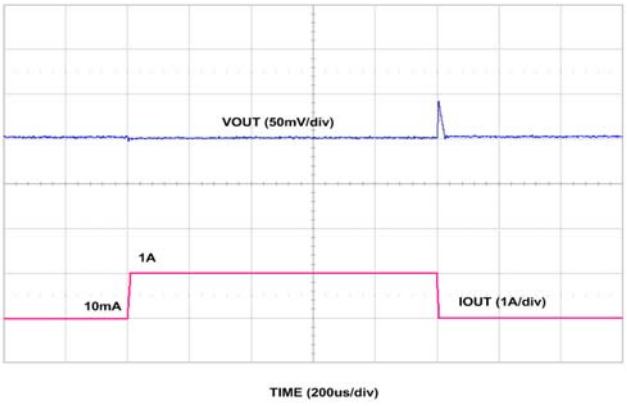


FIGURE 27. LOAD TRANSIENT 10mA TO 1A, C_{OUT} = 10µF CERAMIC

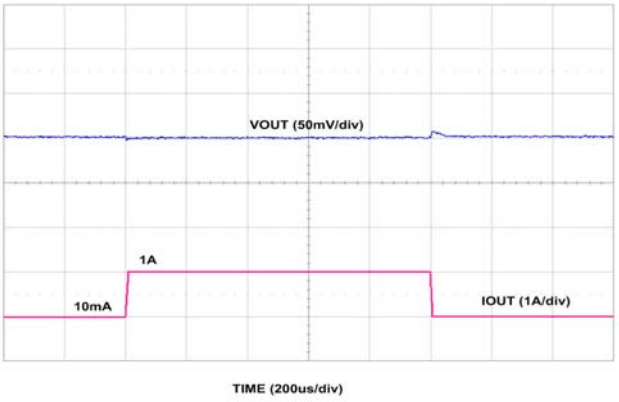


FIGURE 28. LOAD TRANSIENT 10mA TO 1A, C_{OUT} = 100µF CERAMIC

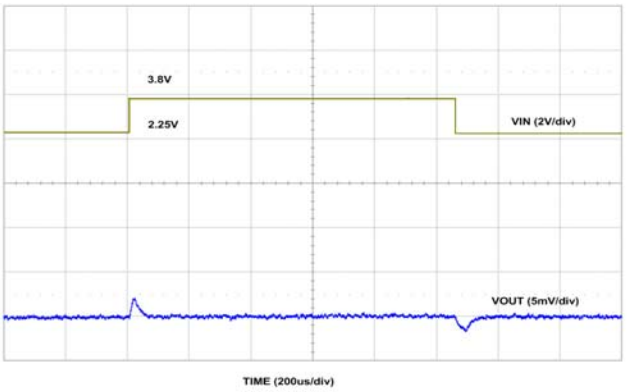


FIGURE 29. I_{LINE} TRANSIENT

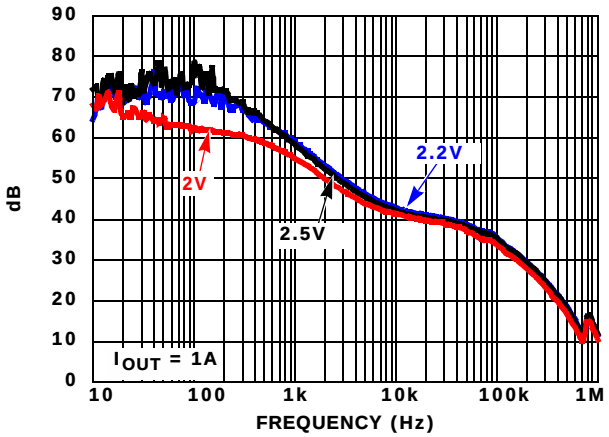


FIGURE 30. PSRR vs V_{IN}

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

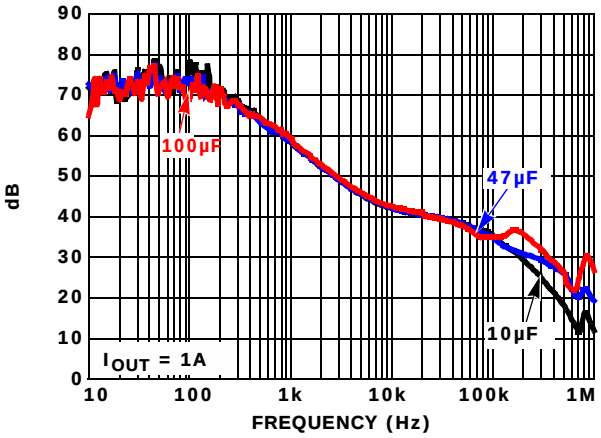


FIGURE 31. PSRR vs C_{OUT}

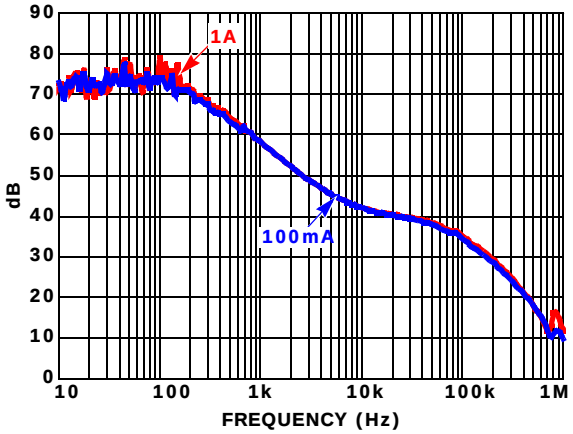


FIGURE 32. PSRR vs LOAD

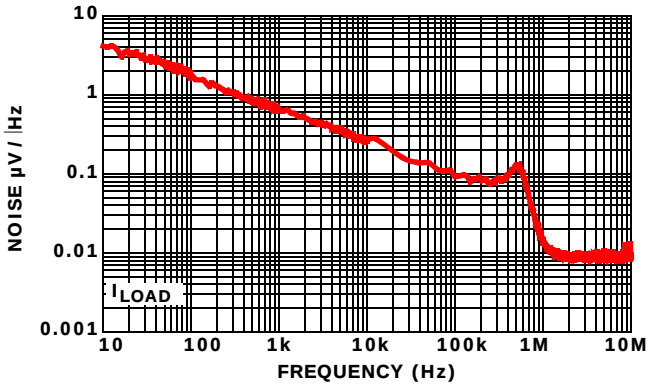


FIGURE 33. SPECTRAL NOISE DENSITY vs FREQUENCY

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
12/21/09	FN6931.0	Initial Release to web

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

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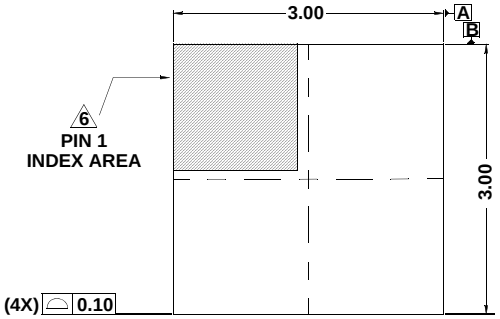
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

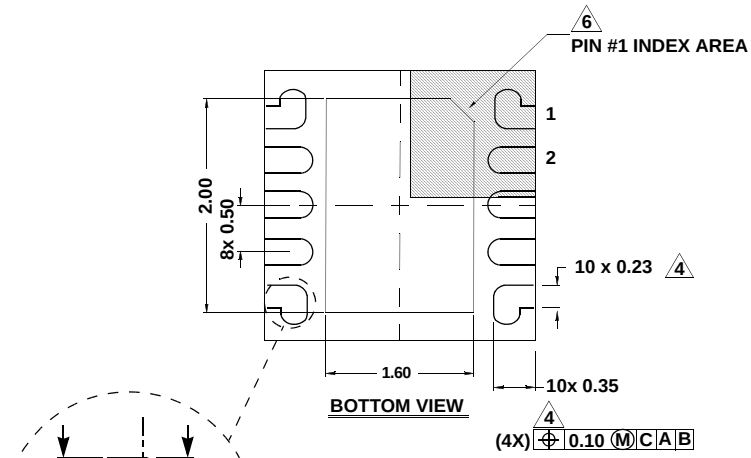
Package Outline Drawing

L10.3x3

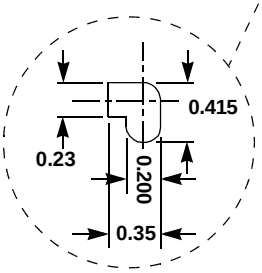
10 LEAD DUAL FLAT PACKAGE (DFN)
Rev 6, 09/09

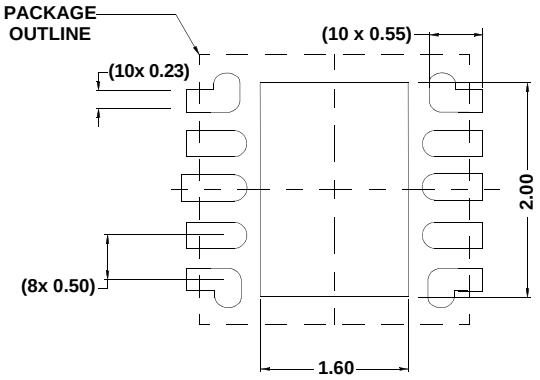


TOP VIEW

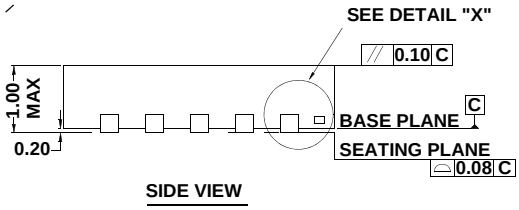


BOTTOM VIEW

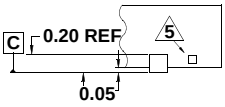




TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.