X-SP3T SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

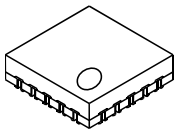
The NJG1655SCC is a GaAs X (Cross)-SP3T switch MMIC which is designed for switching of balanced triple-band filters.

This switch features very low phase error between on state paths, low insertion loss and low control voltage.

This switch integrates a logic decoder function and high ESD protection circuits.

The small PCSP20-CC package is adopted.

■ PACKAGE OUTLINE



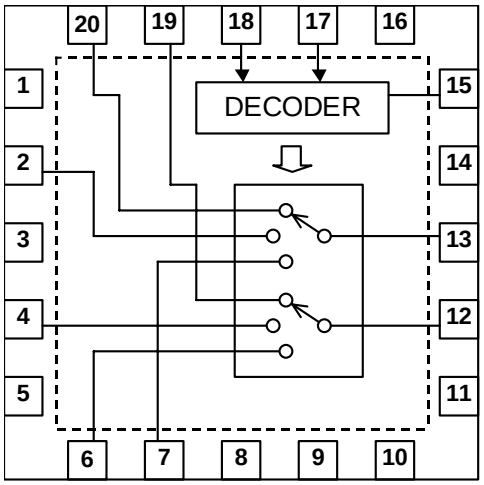
NJG1655SCC

■ FEATURES

● Low voltage operation	V_{DD}=+1.5~+4.5V
● Low voltage Logic control	$V_{CTL(H)}$=+1.3V min,
● Low insertion loss	0.4dB typ. @f=1.0GHz, P_{IN}=0dBm, V_{DD}=2.7V
	0.5dB typ. @f=2.0GHz, P_{IN}=0dBm, V_{DD}=2.7V
● Operating current consumption	20μA typ. @ V_{DD}=2.7V
● Control current consumption	5μA typ. @ $V_{CTL(H)}$=1.8V
● Small package	PCSP20-CC (Package size: 2.7x2.7x0.8mm)

■ PIN CONFIGURATION

(Top View)



Pin connection

1. GND	11. GND
2. P2A	12. PCB
3. GND	13. PCA
4. P2B	14. GND
5. GND	15. VDD
6. P1B	16. GND
7. P1A	17. CTL2
8. GND	18. CTL1
9. GND	19. P3B
10. GND	20. P3A

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

ON PATH	CTL1	CTL2
PCA-P1A PCB-P1B	H	L
PCA-P2A PCB-P2B	L	L
PCA-P3A PCB-P3B	L	H

X (Cross) -SP 3 T Switch : Switch that output port of two SP3T switches crosses internally.

NOTE: The information on this datasheet is subject to change without notice.

■ ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C, Z_s=Z_l=50Ω)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	V_{DD} =2.7V, VCTL=0V/1.8V	28	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	CTL terminal	5.0	V
Power Dissipation	P_D		500	mW
Operating Temp.	T_{opr}		-40~+85	°C
Storage Temp.	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω, V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		1.5	2.7	4.5	V
Operating Current	I_{DD}		-	20	40	μA
Control Voltage (LOW)	$V_{CTL(L)}$		0	-	0.4	V
Control Voltage (HIGH)	$V_{CTL(H)}$		1.3	1.8	4.5	V
Control Current	I_{CTL}		-	5	10	μA
Insertion Loss 1	LOSS1	f=1.0GHz, P_{IN}=0dBm	-	0.4	0.55	dB
Insertion Loss 2	LOSS2	f=2.0GHz, P_{IN}=0dBm	-	0.5	0.7	dB
Isolation 1	ISL1	f=1.0GHz, P_{IN}=0dBm PCA-P1A,P2A,P3A, PCB-P1B,P2B,P3B	24	26	-	dB
Isolation 2	ISL2	f=2.0GHz, P_{IN}=0dBm PCA-P1A,P2A,P3A, PCB-P1B,P2B,P3B	18	20	-	dB
Isolation 3	ISL3	f=2.0GHz, P_{IN}=0dBm PCA-PCB	15	17	-	dB
Phase Error	PE	f=2GHz	-3	-	3	deg
Input Power at 0.2dB Compression Point	$P_{-0.2dB}$	f=2GHz	18	23	-	dBm
VSWR	VSWR	f=2GHz, on state	-	1.1	1.3	
Switching Time	Tsw		-	2	5	μs

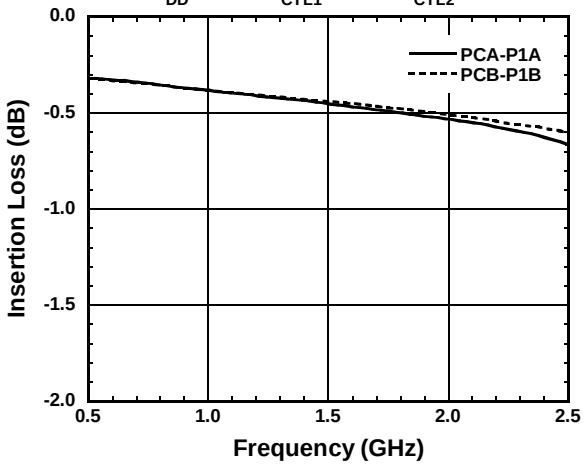
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
2	P2A	The 2nd RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P2B port at the same time. An external capacitor is required to block DC voltage.
4	P2B	The 2nd RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P2A port at the same time. An external capacitor is required to block DC voltage.
6	P1B	The 1st RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P1A port at the same time. An external capacitor is required to block DC voltage.
7	P1A	The 1st RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P1B port at the same time. An external capacitor is required to block DC voltage.
12	PCB	Common RF port of the 2nd switch. This port is connected with either of P1B, P2B, and P3B port. An external capacitor is required to block DC voltage.
13	PCA	Common RF port of the 1st switch. This port is connected with either of P1A, P2A, and P3A port. An external capacitor is required to block DC voltage.
15	VDD	Positive voltage supply terminal. The positive voltage (+1.5~+4.5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
17	CTL2	Control signal input terminal. This terminal is set to High-Level (+1.3V~4.5V) or Low-Level (0~+0.4V).
18	CTL1	Control signal input terminal. This terminal is set to High-Level (+1.3V~4.5V) or Low-Level (0~+0.4V).
19	P3B	The 3rd RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P3A port at the same time. An external capacitor is required to block DC voltage.
20	P3A	The 3rd RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P3B port at the same time. An external capacitor is required to block DC voltage.
1,3,5,8,9, 10,11,14, 16	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.

■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

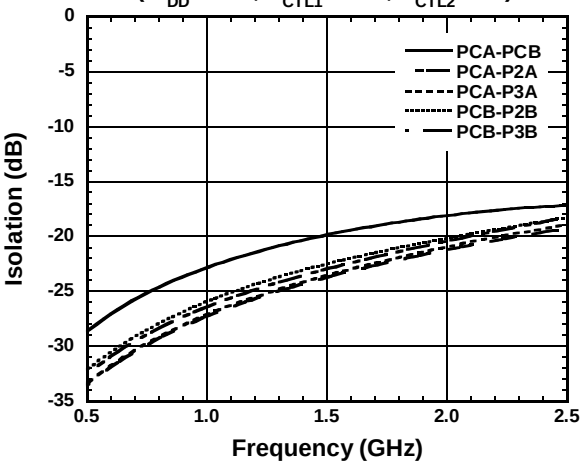
Insertion Loss vs. Frequency

(V_{DD}=2.7V, V_{CTL1}=1.8V, V_{CTL2}=0V)



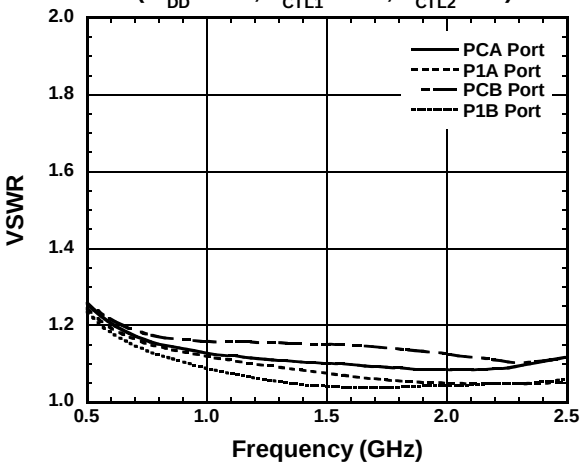
Isolation vs. Frequency

(V_{DD}=2.7V, V_{CTL1}=1.8V, V_{CTL2}=0V)



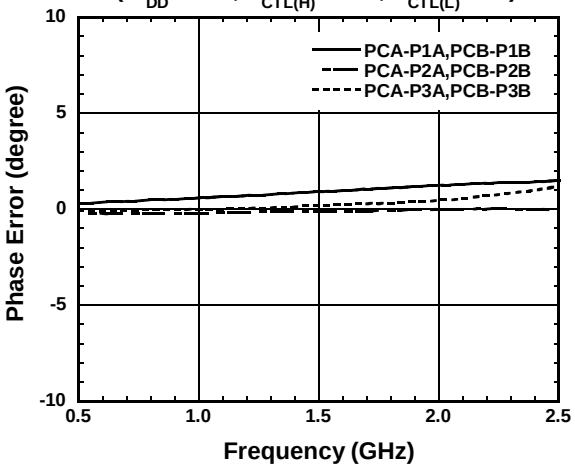
VSWR vs. Frequency

(V_{DD}=2.7V, V_{CTL1}=1.8V, V_{CTL2}=0V)



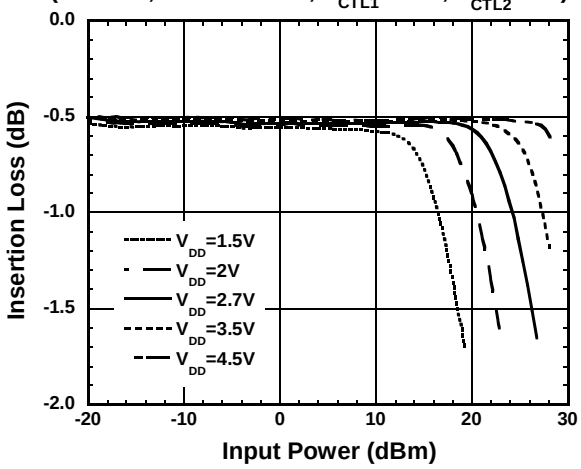
Phase Error vs. Frequency

(V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



Insertion Loss vs. Input Power

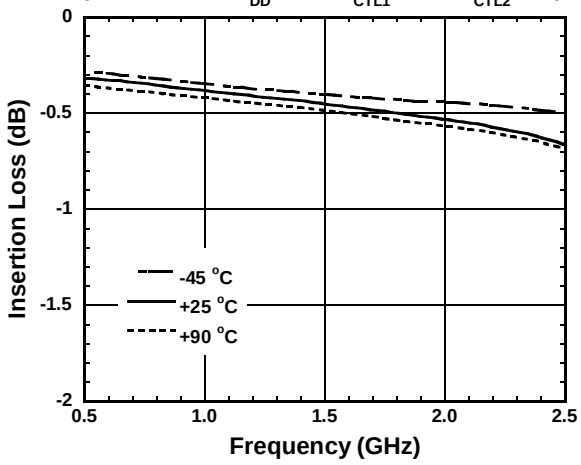
(f=2GHz, PCA-P1A ON, V_{CTL1}=1.8V, V_{CTL2}=0V)



■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

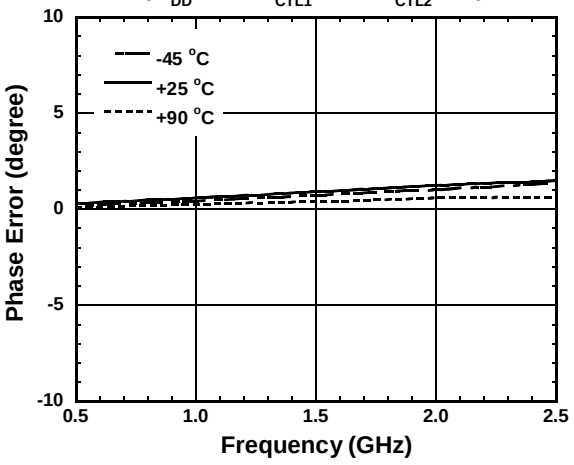
Insertion Loss vs. Frequency

(PCA-P1A ON, V_{DD}=2.7V, V_{CTL1}=1.8V, V_{CTL2}=0V)



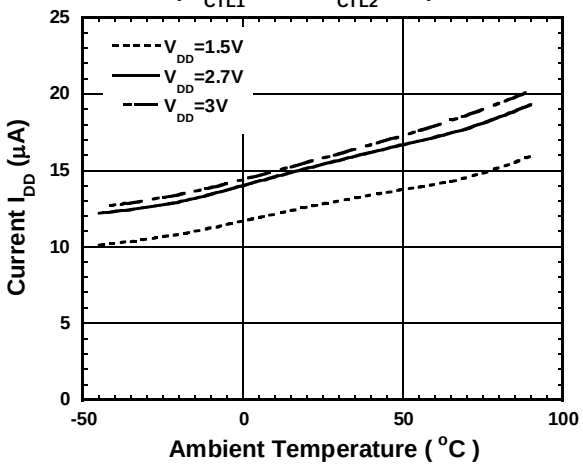
PCA-P1A, PCB-P1B Phase Error vs. Frequency

(V_{DD}=2.7V, V_{CTL1}=1.8V, V_{CTL2}=0V)

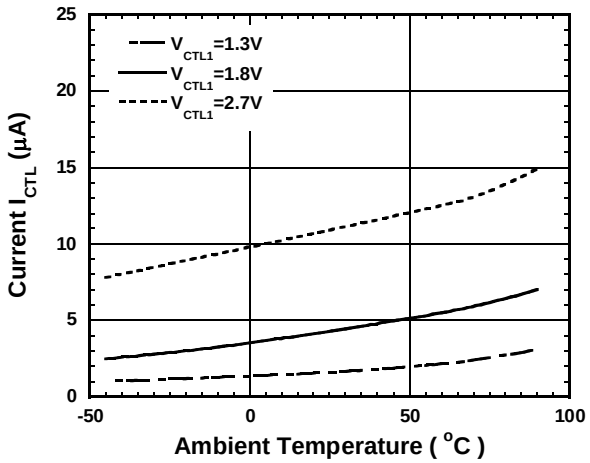


I_{DD} vs. Ambient Temperature

(V_{CTL1}=1.8V, V_{CTL2}=0V)

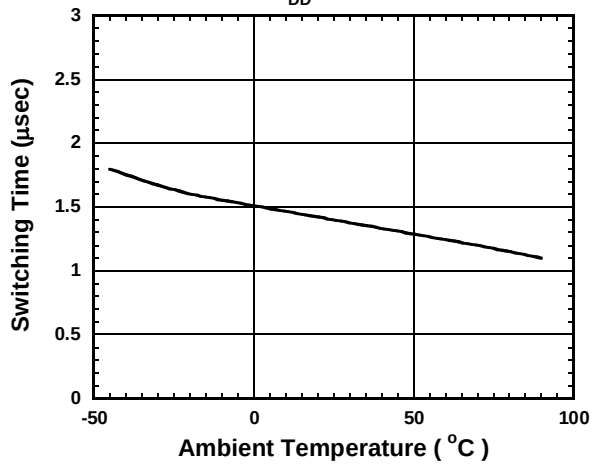


I_{CTL} vs. Ambient Temperature

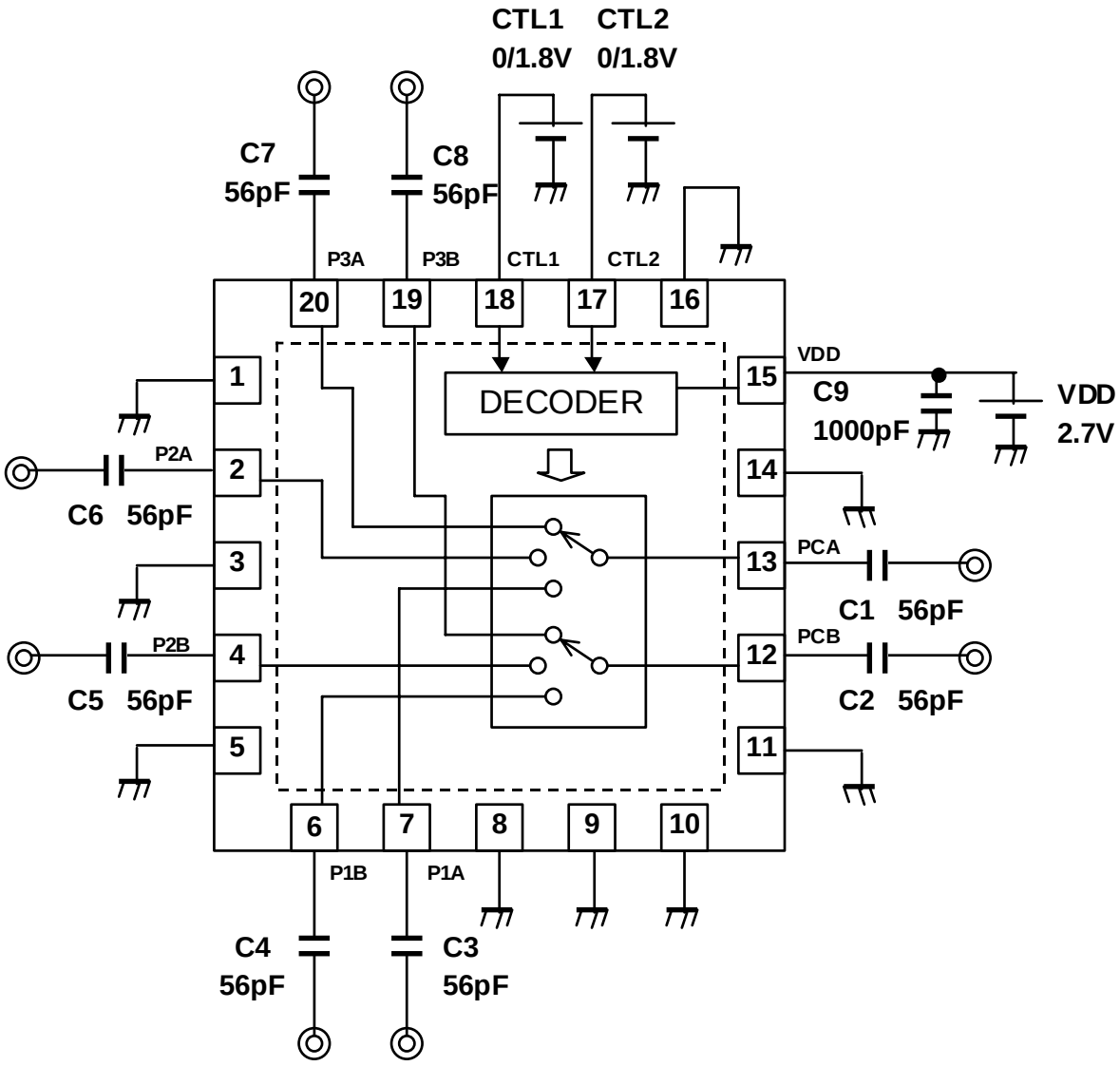


Switching Time vs. Ambient Temperature

(V_{DD}=2.7V)



■ APPLICATION CIRCUIT

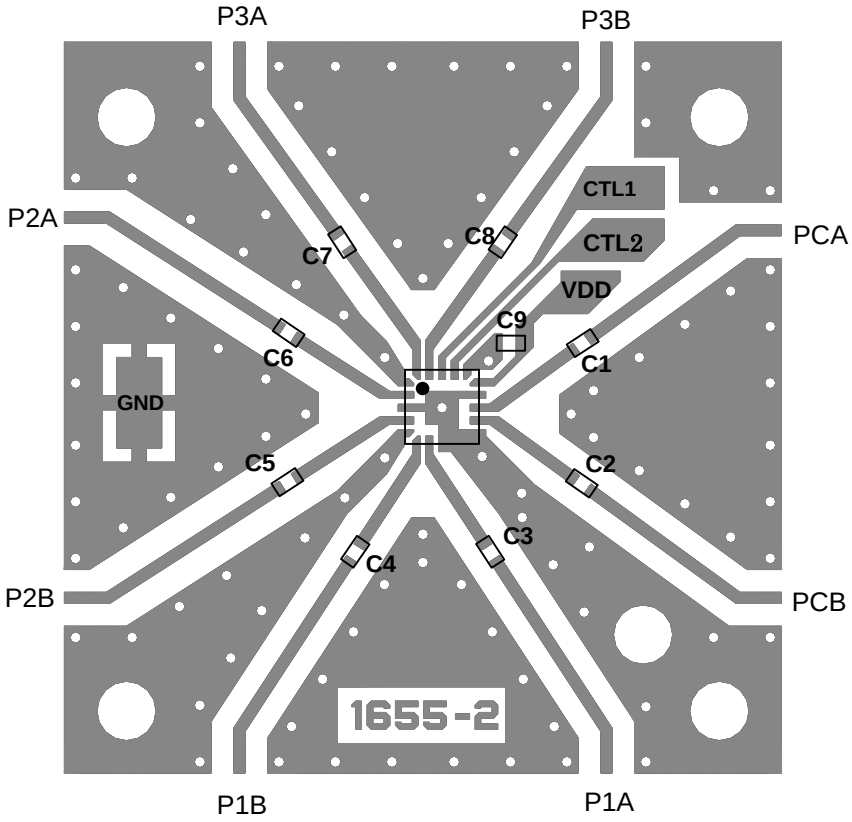


■ PARTS LIST

PART ID	Value	Notes
C1~C8	56pF	MURATA (GRM15)
C9	1000pF	

■ TEST PCB LAYOUT

(TOP VIEW)



Losses of PCB, capacitors and connectors

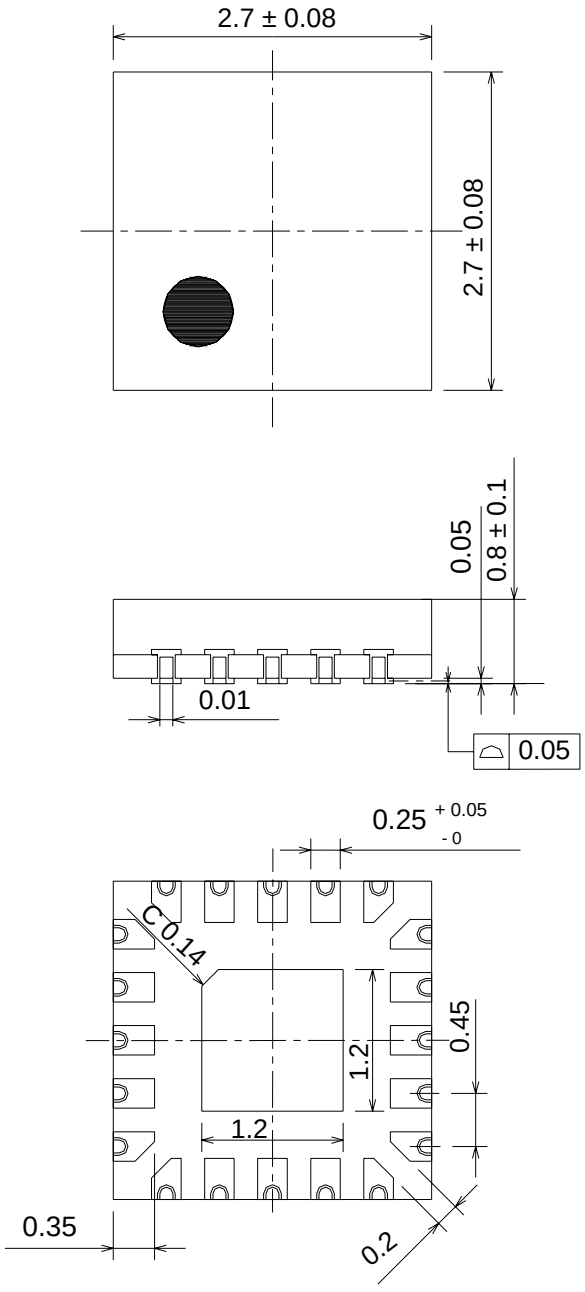
Frequency	Loss
1GHz	0.31dB
2GHz	0.53dB

PCB SIZE=26 x 26mm
PCB: FR-4, t=0.2mm
STRIPLINE WIDTH=0.4mm

PRECAUTIONS

[1] The DC blocking capacitors (C1~C8) must be placed at all RF terminals (PCA, PCB, P1A, P1B, P2A, P2B, P3A and P3B).
[2] The bypass capacitor (C9) should be placed as close as VDD terminal.
[3] Please layout ground pattern right under this IC to avoid degradation of isolation or high power characteristics..

■ PACKAGE OUTLINE (PCSP20-CC)



Terminal Treat	:Au
Substrate	:FR4
Molding Material	:Epoxy resin
Weight	:14.5mg
Unit	:mm

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.