

# DATA SHEET



## **TEA6845AH; TEA6845H** New In Car Entertainment (NICE) car radio

Product specification  
File under Integrated Circuits, IC01

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**New In Car Entertainment (NICE) car radio****TEA6845AH; TEA6845H**

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## New In Car Entertainment (NICE) car radio

## TEA6845AH; TEA6845H

**1 FEATURES**

- FM mixer for conversion of FM RF from 65 to 108 MHz to IF of 10.7 MHz; the mixer provides inherent image rejection
- FM RF mixer can be set to receive weather band radio up to 162.55 MHz; weather band radio flag output
- AM mixer 1 for conversion of AM RF to AM IF1 of 10.7 MHz
- LC tuner oscillator providing mixer frequencies for FM mixer and AM mixer 1
- AM mixer 2 for conversion of AM IF1 to AM IF2 of 450 kHz
- Crystal oscillator providing mixer frequencies for AM mixer 2 and reference for synthesizer PLL, IF count, timing for Radio Data System (RDS) update and reference frequency for car audio signal processor ICs
- Fast synthesizer PLL tuning system with local control for inaudible RDS updating
- Timing function for RDS update algorithm and control signal output for car audio signal processor ICs (TEA688x, SAA77xx) or car radio integrated signal processor IC (TEF6890H)
- Digital auto alignment circuit for conversion of LC oscillator tuning voltage to controlled alignment voltage of FM antenna tank circuit
- AGC PIN diode drive circuit for FM RF AGC; AGC detection at FM mixer input; the AGC PIN diode drive can be activated by the I<sup>2</sup>C-bus as a local or distance function; AGC threshold is a programmable and keyed function switchable via the I<sup>2</sup>C-bus
- FM IF linear amplifiers with high dynamic input range
- FM quadrature demodulator with automatic centre frequency adjustment and Total Harmonic Distortion (THD) compensation
- Level detector for AM and FM with temperature compensated output voltage; starting point and slope of level output is programmable via the I<sup>2</sup>C-bus
- AM RF PIN diode drive circuit; AGC threshold detection at AM mixer 1 and IF2 AGC input; threshold is programmable via the I<sup>2</sup>C-bus; AM IF2 AGC and demodulator
- AM AF output switchable to provide AM IF2 for AM stereo decoder
- AM noise blanker with blanking at AM IF2
- Several test modes available for fast IC and system tests.

**2 GENERAL DESCRIPTION**

The TEA6845 is a single IC with car radio tuner for AM and FM intended for microcontroller tuning with the I<sup>2</sup>C-bus. It provides the following functions:

- AM double conversion receiver for LW, MW and SW (31 m, 41 m and 49 m bands) with IF1 = 10.7 MHz and IF2 = 450 kHz
- FM single conversion receiver with integrated image rejection for IF = 10.7 MHz capable of selecting US FM, US weather, Europe FM, East Europe FM and Japan FM bands.

**3 ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6845AH	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-5
TEA6845H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

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## 4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDA(n)}$	analog supply voltage 1, 3, 4, 5 and 6		8	8.5	9	V
$I_{DDA(tot)}$	total analog supply current 1, 3, 4, 5 and 6	FM mode	45	56	67	mA
		AM mode	39	49	59	mA
$V_{DDA2}$	analog supply voltage 2		4.75	5	5.25	V
$I_{DDA2}$	analog supply current 2	FM mode	6.5	8.1	9.8	mA
		AM mode	4.7	5.9	7.1	mA
$V_{DDD}$	digital supply voltage		4.75	5	5.25	V
$I_{DDD}$	digital supply current	FM mode	18	23	28	mA
		AM mode	18	23	28	mA
$f_{AM(ant)}$	AM input frequency	LW	0.144	–	0.288	MHz
		MW	0.522	–	1.710	MHz
		SW	5.85	–	9.99	MHz
$f_{FM(ant)}$	FM input frequency		65	–	108	MHz
$f_{FM(WB)(ant)}$	FM weather band input frequency		162.4	–	162.55	MHz
$T_{amb}$	ambient temperature		–40	–	+85	°C
<b>AM overall system parameters (1 × SFE10.7MS3; 1 × SFR450H)</b>						
(S+N)/N	signal plus noise-to-noise ratio	$m = 0.3$	–	58	–	dB
THD	total harmonic distortion	$m = 0.8$	–	0.3	–	%
		$m = 0.9$	–	0.5	–	%
<b>FM overall system parameters (3 × SFE10.7MS3)</b>						
(S+N)/N	signal plus noise-to-noise ratio	$\Delta f = 22.5$ kHz; de-emphasis = 50 $\mu$ s	–	65	–	dB
THD	total harmonic distortion	$\Delta f = 75$ kHz	–	0.6	1	%

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5 BLOCK DIAGRAM

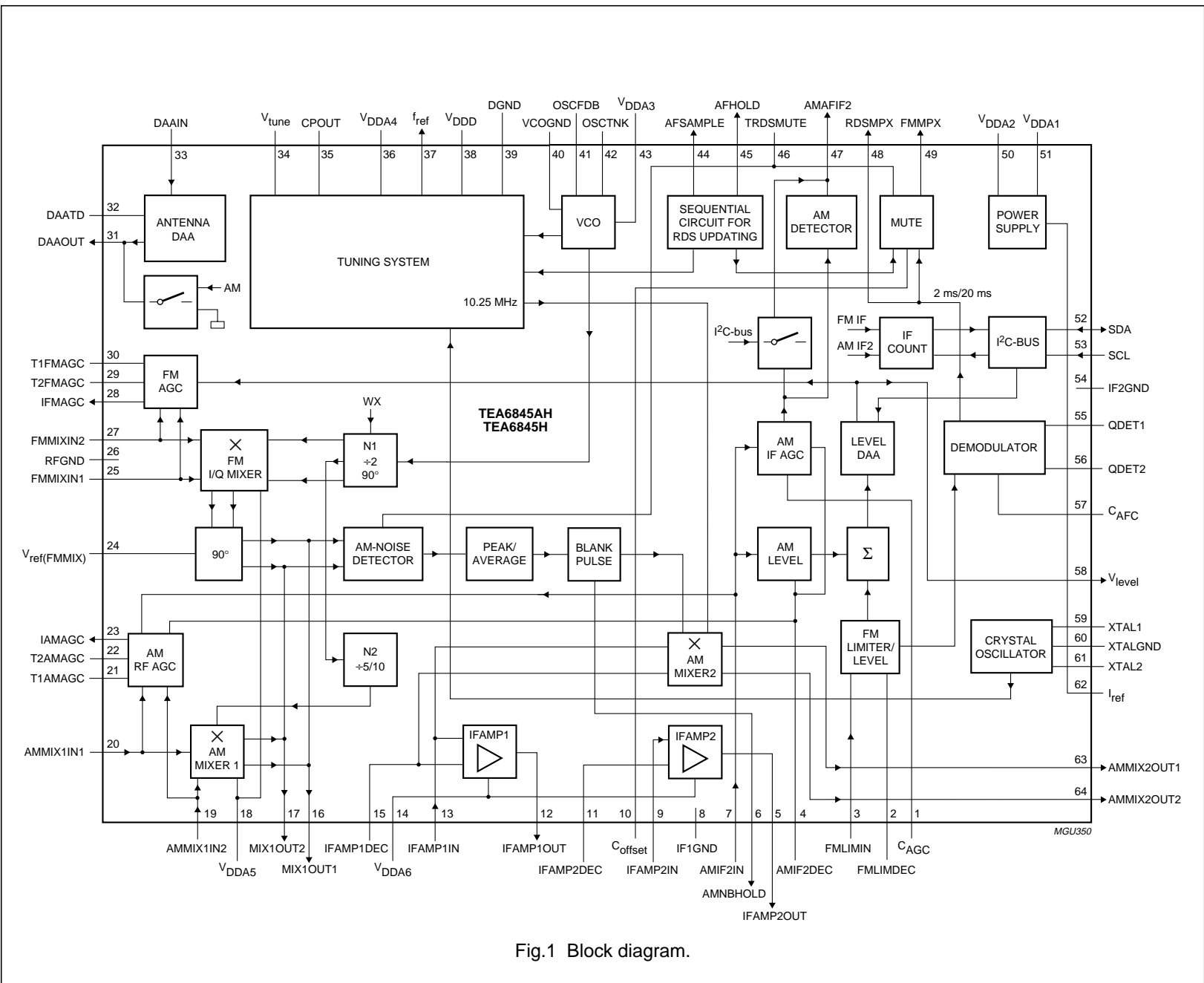


Fig.1 Block diagram.

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## 6 PINNING

SYMBOL	PIN	DESCRIPTION
C <sub>AGC</sub>	1	AMIFAGC capacitor
FMLIMDEC	2	FM limiter decoupling
FMLIMIN	3	FM limiter input (10.7 MHz)
AMIF2DEC	4	decoupling for AM IF2 input
IFAMP2OUT	5	IF amplifier 2 output (10.7 MHz)
AMNBHOLD	6	AM noise blanker hold output
AMIF2IN	7	AM IF2 input (450 kHz) for demodulator AGC and AM level detector
IF1GND	8	AM IF1 ground
IFAMP2IN	9	IF amplifier 2 input (10.7 MHz)
C <sub>offset</sub>	10	DC feedback for offset compensation RDS mute
IFAMP2DEC	11	IF amplifier 2 decoupling and AGC capacitor for AM noise blanker
IFAMP1OUT	12	IF amplifier 1 output (10.7 MHz)
IFAMP1IN	13	IF amplifier 1 and AM mixer 2 input (10.7 MHz)
V <sub>DDA6</sub>	14	analog supply voltage 6 (8.5 V) for IF amplifier 1 and 2
IFAMP1DEC	15	AM mixer 2 and FM IF amplifier 1 decoupling
MIX1OUT1	16	FM mixer and AM mixer 1 IF output high (10.7 MHz)
MIX1OUT2	17	FM mixer and AM mixer 1 IF output low (10.7 MHz)
V <sub>DDA5</sub>	18	analog supply voltage 5 (8.5 V) for FM mixer and AM mixer 1
AMMIX1IN2	19	AM mixer 1 input 2
AMMIX1IN1	20	AM mixer 1 input 1
T1AMAGC	21	1st time constant output of AM front-end AGC
T2AMAGC	22	2nd time constant of AM front-end AGC
IAMAGC	23	PIN diode drive current output of AM front-end AGC
V <sub>ref(FMMIX)</sub>	24	reference voltage for FM mixer
FMMIXIN1	25	input 1 of FM RF mixer
RFGND	26	RF ground
FMMIXIN2	27	input 2 of FM RF mixer
IFMAGC	28	PIN diode drive current output of FM front-end AGC
T2FMAGC	29	2nd time constant of FM front-end AGC
T1FMAGC	30	1st time constant of FM front-end AGC
DAAOUT	31	output of digital alignment circuit for antenna tank circuit
DAATD	32	temperature compensation diode of digital auto alignment circuit for antenna tank circuit
DAAIN	33	input of digital auto alignment circuit for antenna tank circuit
V <sub>tune</sub>	34	tuning voltage
CPOUT	35	charge pump output
V <sub>DDA4</sub>	36	analog supply voltage 4 (8.5 V) for tuning PLL
f <sub>ref</sub>	37	reference frequency output for signal processor IC
V <sub>DDD</sub>	38	digital supply voltage (5 V)
DGND	39	digital ground
VCOGND	40	VCO ground

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SYMBOL	PIN	DESCRIPTION
OSCFDB	41	VCO feedback
OSCTNK	42	VCO tank circuit
V <sub>DDA3</sub>	43	analog supply voltage 3 (8.5 V) for VCO
AFSAMPLE	44	AF sample flag output for car audio signal processor IC
AFHOLD	45	AF hold flag output for car audio signal processor IC
TRDSMUTE	46	time constant for RDS update mute
AMAFIF2	47	AM demodulator AF output or IF2 output for AM stereo (multiplexed by I <sup>2</sup> C-bus)
RDSMPX	48	MPX output for RDS decoder and signal processor (not muted)
FMMPX	49	FM demodulator MPX output
V <sub>DDA2</sub>	50	analog supply voltage 2 (5 V) for on-chip power supply
V <sub>DDA1</sub>	51	analog supply voltage 1 (8.5 V) for on-chip power supply
SDA	52	I <sup>2</sup> C-bus data line input and output
SCL	53	I <sup>2</sup> C-bus clock line input
IF2GND	54	AM IF2 ground
QDET1	55	quadrature demodulator tank 1
QDET2	56	quadrature demodulator tank 2
C <sub>AFC</sub>	57	FM demodulator AFC capacitor
V <sub>level</sub>	58	level voltage output for AM and FM
XTAL1	59	crystal oscillator 1
XTALGND	60	crystal oscillator ground
XTAL2	61	crystal oscillator 2
I <sub>ref</sub>	62	reference current for power supply
AMMIX2OUT1	63	AM mixer 2 output 1 (450 kHz)
AMMIX2OUT2	64	AM mixer 2 output 2 (450 kHz)

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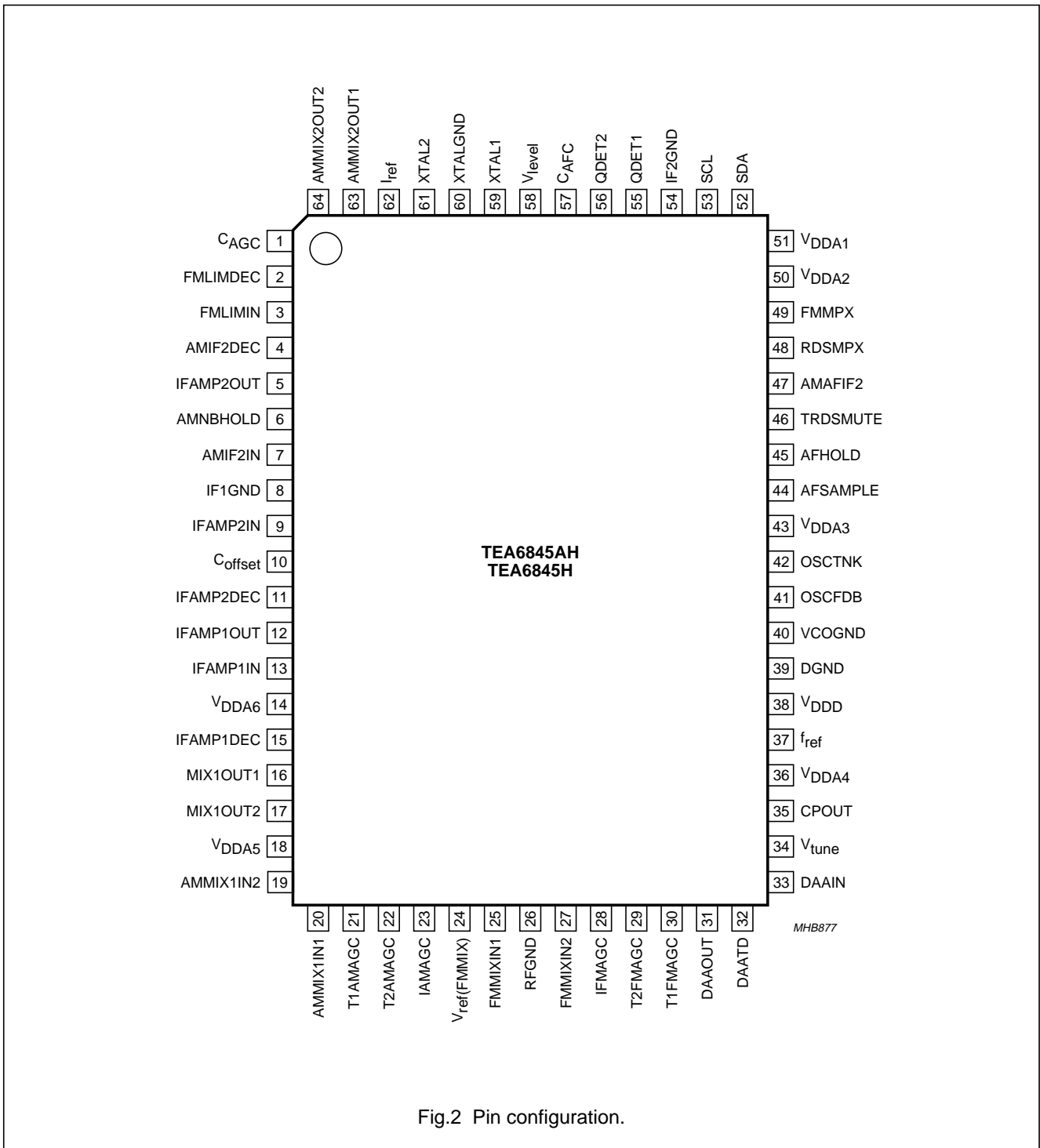


Fig.2 Pin configuration.



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### 7 FUNCTIONAL DESCRIPTION

#### 7.1 Oscillators

##### 7.1.1 VCO

The L and C tuned VCO provides the local oscillator signal for both FM and AM mixer 1. It has a frequency range of 151.2 to 248.2 MHz.

##### 7.1.2 CRYSTAL OSCILLATOR

The crystal oscillator provides a 20.5 MHz signal that is used for:

- Reference frequency for frequency synthesizer PLL
- Local oscillator for AM mixer 2
- Reference frequency for the IF counter
- Timing signal for the RDS update algorithm
- Reference frequency (75.4 kHz) for the TEA6880H (car audio signal processor - CASP) or TEF6890H (car radio integrated signal processor).

##### 7.1.3 PLL

Fast synthesizer PLL tuning system with local control for inaudible RDS updating.

#### 7.2 FM signal channel

##### 7.2.1 DAA

FM RF Digital Auto Alignment (DAA) circuitry for the conversion of the VCO tuning voltage to a controlled alignment voltage for the FM antenna tank circuit.

##### 7.2.2 FM I/Q MIXER

FM quadrature mixer converts FM RF (65 to 162.55 MHz) to IF of 10.7 MHz. The FM mixer provides inherent image rejection and high RF sensitivity.

It is capable of tuning the US FM, US weather, Europe FM, Japan FM and East Europe FM bands:

- US FM = 87.9 to 107.9 MHz
- US weather FM = 162.4 to 162.55 MHz
- Europe FM = 87.5 to 108 MHz
- Japan FM = 76.0 to 91 MHz
- East Europe FM = 65.8 to 74 MHz.

##### 7.2.3 FM KEYED AGC

FM contains keyed wide-band RF AGC. AGC detection occurs at the FM mixer. The wide-band RF signal switches a narrow band signal (IF) from the FM IF level detector circuitry that controls the FM RF AGC block.

It includes an AGC PIN diode drive circuit for the FM RF AGC. The PIN diode drive can be activated via the I<sup>2</sup>C-bus as a local or distance function.

The AGC threshold is programmable and the keyed AGC function is switchable via the I<sup>2</sup>C-bus.

##### 7.2.4 FM IF AMPLIFIERS

The two FM IF amplifiers provide 10 dB and 4 dB amplification with high linearity and dynamic range.

##### 7.2.5 FM DEMODULATOR

The FM quadrature demodulator includes automatic centre frequency adjustment and THD compensation.

#### 7.3 AM signal channel

##### 7.3.1 AM TUNER INCLUDING MIXER 1 AND MIXER 2

The AM tuner is realized in a double conversion technique and is capable of selecting LW, MW and SW bands.

AM mixer 1 converts AM RF to IF1 of 10.7 MHz, while AM mixer 2 converts IF1 of 10.7 MHz to IF2 of 450 kHz:

- LW = 144 to 288 kHz
- MW = 530 to 1710 kHz (US AM band)
- SW = 5.85 to 9.99 MHz (including the 31 m, 41 m and 49 m bands).

##### 7.3.2 AM RF AGC AND IF2 AGC

The AM RF includes a PIN diode drive circuit. The threshold detection points for AM AGC are performed at AM mixer 1 and AM IF2. AGC thresholds are programmable via the I<sup>2</sup>C-bus.

##### 7.3.3 AM DETECTOR

The AM detector provides AM level information and AM AF or AM IF2.

##### 7.3.4 AM AF OR IF2 SWITCH

The AM output provides either a detected AM AF or the corresponding AM IF2 signal. The IF2 signal can be used for AM stereo decoder processing.

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## 7.3.5 AM NOISE DETECTOR AND BLANKER

The detection point for the AM noise blanker is the output stage of AM mixer 1, while blanking is realized at the output of the mixer 2.

Trigger sensitivity can be modified by changing the resistor value at pin AMNBHOLD.

## 7.3.6 FM AND AM LEVEL DETECTOR

FM and AM level detectors provide the temperature compensated output voltage. The starting points and slopes of the level detector outputs are programmable via the I<sup>2</sup>C-bus.

## 7.4 Test mode

The test mode of the IC is activated by:

- Sending the test byte (byte 5) to the IC
- Connecting pin  $f_{ref}$  through a 100 k $\Omega$  resistor to  $V_{DDA1}$
- Applying 50  $\mu$ A to pin  $f_{ref}$ .

If the test mode is enabled by pin  $f_{ref}$ :

- The settling time of the AM IF2 AGC is reduced to less than 100 ms in the nominal application
- The digital-to-analog converters for the antenna DAA and the level DAA can be clocked directly by the SCL line of the I<sup>2</sup>C-bus
- The output at pin  $f_{ref}$  can be selected by the I<sup>2</sup>C-bus: TEA6880H or TEF6890H reference frequency, PLL reference frequency or PLL programmable divider output frequency
- The RDS update control circuit can be clocked directly via pin DAATD
- Pin T1AMAGC can be used to enable the load PLL circuit of the RDS update control circuit
- Charge pumps can be set into 3-state mode.

## 8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DDA1}$	analog supply voltage 1 for on-chip power supply		-0.3	+10	V
$V_{DDA2}$	analog supply voltage 2 for on-chip power supply		-0.3	+6.5	V
$V_{DDA3}$	analog supply voltage 3 for VCO		-0.3	+10	V
$V_{DDA4}$	analog supply voltage 4 for tuning PLL		-0.3	+10	V
$V_{DDA5}$	analog supply voltage 5 for FM and AM RF		-0.3	+10	V
$V_{DDA6}$	analog supply voltage 6 for IF amplifier 1 and 2		-0.3	+10	V
$V_{DDD}$	digital supply voltage		-0.3	+6.5	V
$\Delta V_{DD8.5-DD5}$	difference between any 8.5 V supply voltage and any 5 V supply voltage	note 1	-0.3	-	V
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$V_{es}$	electrostatic handling voltage	note 2	-200	+200	V
		note 3	-2000	+2000	V

## Notes

1. To avoid damages and wrong operation it is necessary to keep all 8.5 V supply voltages at a higher level than any 5 V supply voltage. This is also necessary during power-on and power-down sequences. Precautions have to be provided in such a way that interferences can not pull down the 8.5 V supply below the 5 V supply.
2. Machine model ( $R = 0 \Omega$ ,  $C = 200 \text{ pF}$ ).
3. Human body model ( $R = 1.5 \text{ k}\Omega$ ,  $C = 100 \text{ pF}$ ).

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## 9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TEA6845AH		46	K/W
	TEA6845H		48	K/W

## 10 DC CHARACTERISTICS

$V_{DDA1} = V_{DDA3} = V_{DDA4} = V_{DDA5} = V_{DDA6} = 8.5$  V;  $V_{DDA2} = 5$  V;  $V_{DDD} = 5$  V;  $T_{amb} = 25$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply voltage</b>						
$V_{DDA(n)}$	analog supply voltage 1, 3, 4, 5 and 6		8	8.5	9	V
$V_{DDA2}$	analog supply voltage 2		4.75	5	5.25	V
$V_{DDD}$	digital supply voltage		4.75	5	5.25	V
<b>Supply current in FM mode</b>						
$I_{DDD}$	digital supply current		18	23	28	mA
$I_{DDA1}$	analog supply current 1 for on-chip power supply		–	15	–	mA
$I_{DDA2}$	analog supply current 2 for on-chip power supply		6.5	8.1	9.8	mA
$I_{DDA3}$	analog supply current 3 for VCO		–	6.5	–	mA
$I_{DDA4}$	analog supply current 4 for tuning PLL	test mode; bit TMS3 = 1	–	2.9	–	mA
$I_{DDA5}$	analog supply current 5 for FM RF		–	5	–	mA
$I_{DDA6}$	analog supply current 6 for FM IF amplifier 1 and 2		10	12	14	mA
$I_{MIX1OUT1}$	bias current of FM mixer output 1		4.8	6	7.2	mA
$I_{MIX1OUT2}$	bias current of FM mixer output 2		4.8	6	7.2	mA
<b>Supply current in AM mode</b>						
$I_{DDD}$	digital supply current		18	23	28	mA
$I_{DDA1}$	analog supply current 1 for on-chip power supply		–	17.5	–	mA
$I_{DDA2}$	analog supply current 2 for on-chip power supply		4.7	5.9	7.1	mA
$I_{DDA3}$	analog supply current 3 for VCO		–	6.5	–	mA
$I_{DDA4}$	analog supply current 4 for tuning PLL	test mode; bit TMS3 = 1	–	1.6	–	mA
$I_{DDA5}$	analog supply current 5 for RF		–	1.8	–	mA
$I_{MIX1OUT1}$	bias current of AM mixer 1 output 1		4.8	6	7.2	mA
$I_{MIX1OUT2}$	bias current of AM mixer 1 output 2		4.8	6	7.2	mA
$I_{AMMIX2OUT1}$	bias current of AM mixer 2 output 1		3.6	4.5	5.4	mA
$I_{AMMIX2OUT2}$	bias current of AM mixer 2 output 2		3.6	4.5	5.4	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>On-chip power supply reference current generator: pin I<sub>ref</sub></b>						
V <sub>o(ref)</sub>	output reference voltage		4	4.25	4.5	V
R <sub>o</sub>	output resistance		8	11	13	kΩ
I <sub>o(max)</sub>	maximum output current		-100	-	+100	nA

**11 AC CHARACTERISTICS**

V<sub>DDA1</sub> = V<sub>DDA3</sub> = V<sub>DDA4</sub> = V<sub>DDA5</sub> = V<sub>DDA6</sub> = 8.5 V; V<sub>DDA2</sub> = 5 V; V<sub>DDD</sub> = 5 V; T<sub>amb</sub> = 25 °C; see Figs 9 and 10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Voltage controlled oscillator</b>						
f <sub>osc</sub>	oscillator frequency		151.2	-	248.2	MHz
C/N	carrier-to-noise ratio	f <sub>osc</sub> = 200 MHz; Δf = 10 kHz	-	101	-	$\frac{\text{dBc}}{\sqrt{\text{Hz}}}$
RR	ripple rejection	f <sub>ripple</sub> = 100 Hz; V <sub>DDA3(ripple)</sub> = 100 mV (RMS)	-	97	-	dB
		f <sub>osc</sub> = 250 MHz	-	99	-	dB
		f <sub>osc</sub> = 200 MHz	-		-	
<b>FEEDBACK INPUT: PIN OSCFDB</b>						
V <sub>i(bias)</sub>	input bias voltage		2.2	2.8	3.4	V
<b>TANK CIRCUIT OUTPUT: PIN OSCTNK</b>						
V <sub>O</sub>	DC output voltage		5	6.1	7.2	V
V <sub>o(rms)</sub>	AC output voltage (RMS value)	f <sub>osc</sub> = 200 MHz	-	1.5	-	V
<b>Crystal oscillator</b>						
f <sub>xtal</sub>	crystal frequency		20.4996	20.5	20.5004	MHz
R <sub>xtal</sub>	crystal motional resistance	start of operating	-	-	500	Ω
C <sub>xtal</sub>	crystal shunt capacitance		-	-	18	pF
C/N	carrier-to-noise ratio	f <sub>xtal</sub> = 20.5 MHz (10.25 MHz); Δf = 10 kHz	-	112	-	$\frac{\text{dBc}}{\sqrt{\text{Hz}}}$
<b>CIRCUIT INPUTS: PINS XTAL1, XTAL2 AND XTALGND</b>						
V <sub>xtal(rms)</sub>	crystal voltage (RMS value)	note 2	-	350	-	mV
V <sub>XTAL1</sub> , V <sub>XTAL2</sub>	DC bias voltage		1.7	2.1	2.5	V
R <sub>i</sub>	real part of input impedance	V <sub>XTAL1</sub> - V <sub>XTAL2</sub> = 1 mV; note 1	-500	-	-	Ω
C <sub>i</sub>	input capacitance	note 1	8	10	12	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>XTALGND</sub>	crystal oscillator circuit current	start-up at V <sub>XTAL1</sub> = V <sub>XTAL2</sub> = 2.1 V	–	9	–	mA
		operating at V <sub>XTAL1</sub> – V <sub>XTAL2</sub> = ±400 mV	–	1.5	–	mA
<b>Oscillator divider N1</b>						
N1	oscillator divider ratio	FM mode: standard, Europe and local weather band (WX)	– –	2 1	– –	
<b>Oscillator divider N2</b>						
N2	oscillator divider ratio	AM mode SW LW and MW	– –	10 5	– –	
<b>Synthesizer</b>						
PROGRAMMABLE DIVIDER						
N <sub>prog</sub>	programmable divider ratio		512	–	32767	
ΔN <sub>step</sub>	programmable divider step size		–	1	–	
REFERENCE FREQUENCY DIVIDER						
N <sub>ref</sub>	crystal oscillator divider ratio	f <sub>xtal</sub> = 20.5 MHz f <sub>ref</sub> = 100 kHz f <sub>ref</sub> = 50 kHz f <sub>ref</sub> = 25 kHz f <sub>ref</sub> = 20 kHz f <sub>ref</sub> = 10 kHz	– – – – –	205 410 820 1025 2050	– – – – –	
CHARGE PUMP: PIN CPOUT						
I <sub>sink(cp1)l</sub>	low charge pump 1 peak sink current	FM weather band mode; 0.4 V < V <sub>CPOUT</sub> < 7.6 V	200	300	400	μA
I <sub>source(cp1)l</sub>	low charge pump 1 peak source current	FM weather band mode; 0.4 V < V <sub>CPOUT</sub> < 7.6 V	–400	–300	–200	μA
I <sub>sink(cp1)h</sub>	high charge pump 1 peak sink current	AM stereo mode; N2 = 10 (LW and MW); 0.4 V < V <sub>CPOUT</sub> < 7.6 V	0.7	1	1.3	mA
I <sub>source(cp1)h</sub>	high charge pump 1 peak source current	AM stereo mode; N2 = 10 (LW and MW); 0.4 V < V <sub>CPOUT</sub> < 7.6 V	–1.3	–1	–0.7	mA
I <sub>sink(cp2)</sub>	charge pump 2 peak sink current	FM standard mode; 0.3 V < V <sub>CPOUT</sub> < 7.1 V	100	130	160	μA
I <sub>source(cp2)</sub>	charge pump 2 peak source current	FM standard mode; 0.3 V < V <sub>CPOUT</sub> < 7.1 V	–160	–130	–100	μA
I <sub>Z(cp1)</sub> , I <sub>Z(cp2)</sub>	charge pump 1 or 2 current in 3-state	0 < V <sub>CPOUT</sub> < 8.5 V	–5	–	+5	nA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHARGE PUMP: PIN $V_{\text{tune}}$						
$I_{\text{sink(cp3)}}$	charge pump 3 peak sink current	FM standard mode; $0.4 \text{ V} < V_{\text{tune}} < 7.6 \text{ V}$	2.1	3	3.9	mA
$I_{\text{source(cp3)}}$	charge pump 3 peak source current	FM standard mode; $0.4 \text{ V} < V_{\text{tune}} < 7.6 \text{ V}$	-3.9	-3	-2.1	mA
$I_{\text{Z(cp3)}}$	charge pump 3 current in 3-state	$0 < V_{\text{tune}} < 8.5 \text{ V}$	-5	-	+5	nA
<b>Antenna Digital Auto Alignment (DAA)</b>						
DAA INPUT: PIN DAAIN						
$I_{\text{bias(cp)}}$	charge pump buffer input bias current	FM mode; $0.4 \text{ V} < V_{\text{DAAIN}} < 8.0 \text{ V}$	-10	-	+10	nA
		AM mode; $0 \text{ V} < V_{\text{DAAIN}} < 8.5 \text{ V}$	-10	-	+10	nA
$V_{\text{i(cp)}}$	charge pump buffer input voltage		0	-	8.5	V
DAA OUTPUT: PIN DAAOUT; note 2						
$V_{\text{o(AM)}}$	DAA output voltage in AM mode		-	-	0.3	V
$V_{\text{o(FM)}}$	DAA output voltage in FM mode	$V_{\text{DAAIN}} = 4.0 \text{ V};$ $V_{\text{DAAATD}} = 0.7 \text{ V}$ minimum value	-	-	0.5	V
		bits DAA[6:0] set to logic 0	1.5	1.65	1.8	V
		value: data byte 3 = 10101011	3.8	4	4.2	V
		maximum value; bits DAA[6:0] set to logic 1	8	-	8.5	V
		$V_{\text{DAAIN}} = 3.0 \text{ V};$ $V_{\text{DAAATD}} = 0.7 \text{ V};$ bits DAA[6:0] set to logic 1	6.2	6.5	6.8	V
		$V_{\text{DAAIN}} = 2 \text{ V}$ data byte 3 = 11010101	3	3.3	3.6	V
		data byte 3 = 10101010	1.8	2	2.2	V
$V_{\text{o(n)}}$	DAA output noise voltage	FM mode; $V_{\text{DAAIN}} = 4 \text{ V};$ data byte 3: bit 6 = 1, bits 5 to 0 = 0; $B = 300 \text{ Hz to } 15 \text{ kHz}$	-	30	100	$\mu\text{V}$
$\Delta V_{\text{o}}(\text{T})$	DAA output voltage variation with temperature	$T_{\text{amb}} = -40 \text{ to } +85 \text{ }^\circ\text{C};$ data byte 3 = 10101011; $V_{\text{DAAATD}} = 0.7 \text{ V}$	-8	-	+8	mV
$\Delta V_{\text{o}}(\text{step})$	DAA step accuracy	FM mode; $V_{\text{DAAOUT}} < 8.0 \text{ V};$ $n = 0 \text{ to } 127$	$0.5V_{\text{LSB}}$	$V_{\text{LSB}}$	$1.5V_{\text{LSB}}$	mV
$I_{\text{o(sink)}}$	DAA output sink current	$0.2 \text{ V} < V_{\text{DAAOUT}} < 8.25 \text{ V}$	50	-	-	$\mu\text{A}$
$I_{\text{o(source)}}$	DAA output source current		-	-	-50	$\mu\text{A}$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{st}$	DAA output settling time	$0.2\text{ V} < V_{DAAOUT} < 8.25\text{ V}$ ; $C_L = 270\text{ pF}$	–	–	30	$\mu\text{s}$
RR	ripple rejection	$f_{ripple} = 100\text{ Hz}$ ; $V_{DDA4} = 1\text{ mV}$	–	50	–	dB
$C_L$	DAA output load capacitance	$V_{DAAOUT} < 8.0\text{ V}$ ; FM mode	–	–	270	pF
<b>DAA TEMPERATURE COMPENSATION: PIN DAATD</b>						
$I_{source}$	compensation diode source current	$0.2\text{ V} < V_{DAATD} < 1.5\text{ V}$	–50	–40	–30	$\mu\text{A}$
$TC_{source}$	temperature coefficient of compensation diode source current	$0.2\text{ V} < V_{DAATD} < 1.5\text{ V}$ ; $T_{amb} = -40\text{ to }+85\text{ }^\circ\text{C}$	$-3 \times 10^{-10}$	–	$+3 \times 10^{-10}$	$\text{K}^{-1}$
<b>IF counter (FM IF or AM IF2 counter)</b>						
$N_{IF}$	IF counter length for AM and FM		–	8	–	bit
$T_{count(IF)}$	IF counter period	data byte 4: bit 7 = 1	–	2	–	ms
		data byte 4: bit 7 = 0	–	20	–	ms
$R_{precount}$	FM IF counter prescaler ratio	data byte 4: bit 3 = 1	–	10	–	
		data byte 4: bit 3 = 0	–	100	–	
<b>Reference frequency for car sound processor IC; note 3</b>						
REFERENCE FREQUENCY DIVIDER						
$N_{ref}$	crystal oscillator divider ratio		–	272	–	
$f_{ref}$	reference frequency	$f_{xtal} = 20.5\text{ MHz}$	–	75.368	–	kHz
VOLTAGE GENERATOR; PIN $f_{ref}$						
$V_{o(p-p)}$	AC output voltage (peak-to-peak value)		60	100	170	mV
$V_O$	DC output voltage		3.2	3.4	3.9	V
$R_o$	output resistance		–	–	50	$\text{k}\Omega$
$R_{L(min)}$	minimum load resistance		1	–	–	$\text{M}\Omega$
<b>AM signal channel</b>						
AM RF AGC STAGE INPUTS: PINS AMMIX1IN1 AND AMMIX1IN2						
$V_{i(p)}$	RF input voltage for AGC start level (peak value)	data byte 5: bit 5 = 0, bit 6 = 0	–	150	–	mV
		data byte 5: bit 5 = 1, bit 6 = 0	–	275	–	mV
		data byte 5: bit 5 = 0, bit 6 = 1	–	400	–	mV
		data byte 5: bit 5 = 1, bit 6 = 1	–	525	–	mV
AM IF AGC STAGE INPUTS: PINS AMIF2IN AND AMIF2DEC						
$V_{i(p)}$	IF2 input voltage (peak value)	AGC start level	0.20	0.27	0.35	V
AM RF AGC CURRENT GENERATOR OUTPUT: PIN IAMAGC						
$I_{sink(max)}$	maximum AGC sink current	$V_{AMMIX1IN1} > 500\text{ mV}$ (peak value)	–	15	–	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R <sub>o</sub>	output resistance	I <sub>IAMAGC</sub> = 1 μA	1	–	–	MΩ
C <sub>o</sub>	output capacitance		–	5	7	pF
<b>AM RF AGC PEAK DETECTOR: PIN T2AMAGC</b>						
I <sub>att</sub>	attack current AGC peak detector	data byte 5: bit 5 = 1, bit 6 = 1; AM mixer 1 input V <sub>i</sub> = 1 V; V <sub>T2AMAGC-GND</sub> = 3 V; V <sub>AMIF2IN-AMIF2DEC</sub> = 0 V	–	3.15	–	mA
I <sub>dec</sub>	decay current AGC peak detector	data byte 5: bit 5 = 1, bit 6 = 1; AM mixer 1 input V <sub>i</sub> = 0 V; V <sub>T2AMAGC-AMMIN1IN2</sub> = 0.25 V; V <sub>T2AMAGC-GND</sub> = 3 V; V <sub>AMIF2IN-AMIF2DEC</sub> = 0 V	–	2.6	–	μA
<b>AM MIXER 1 (IF1 = 10.7 MHz)</b>						
<i>Mixer inputs: pins AMMIX1IN1 and AMMIX1IN2</i>						
R <sub>i</sub>	input resistance	note 4	50	70	100	kΩ
C <sub>i</sub>	input capacitance	note 4	–	5	7	pF
V <sub>I</sub>	DC input voltage		2.3	2.7	3.1	V
V <sub>i(max)</sub>	maximum voltage on pin AMMIX1IN1	1 dB compression point of AM mixer 1 output (peak-to-peak)	500	–	–	mV
<i>Mixer outputs: pins MIX1OUT1 and MIXOUT2</i>						
R <sub>o</sub>	output resistance	note 5	100	–	–	kΩ
C <sub>o</sub>	output capacitance	note 5	–	5	7	pF
V <sub>o(max)(p-p)</sub>	maximum output voltage (peak-to-peak value)		12	15	–	V
I <sub>bias</sub>	mixer bias current	AM mode	4.8	6	7.2	mA
<b>Mixer</b>						
g <sub>m(conv)</sub>	conversion transconductance $\frac{I_{MIXOUT1}}{V_{FMMIXIN1 - FMMIXIN2}}$		2.0	2.55	3.2	$\frac{\text{mA}}{\text{V}}$
g <sub>m(conv)(T)</sub>	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$		–	$-9 \times 10^{-4}$	–	K <sup>-1</sup>
IP3	3rd-order intermodulation	R <sub>L</sub> = 2.8 kΩ (AC load between output pins)	135	138	–	dBμV
IP2	2nd-order intermodulation	R <sub>L</sub> = 2.8 kΩ (AC load between output pins)	–	170	–	dBμV



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(n)(eq)}$	equivalent input noise voltage	band limited noise; $R_{gen} = 750 \Omega$ ; $R_L = 2.8 \text{ k}\Omega$ (AC load between output pins)	–	5.8	–	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
F	noise figure of AM mixer 1		–	4.5	7.1	dB
WEATHER BAND FLAG: PIN T1AMAGC						
$I_{L(max)}$	maximum load current		–5	–	+5	$\mu\text{A}$
$V_{o(max)}$	maximum output voltage for FM mode	measured with respect to pin RFGND	0	–	0.5	V
$V_{o(min)}$	minimum output voltage for WX mode	measured with respect to pin RFGND	5.1	6.0	6.9	V
AM MIXER 2 (IF2 = 450 kHz)						
<i>Mixer inputs: pins IFAMP1IN and IFAMP1DEC</i>						
$R_i$	input resistance	note 6	270	330	390	$\Omega$
$C_i$	input capacitance	note 6	–	5	7	pF
$V_I$	DC voltage		2.4	2.7	3	V
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of AM mixer 2 output (peak-to-peak)	1.1	–	–	V
<i>Mixer outputs: pins AMMIX2OUT1 and AMMIXOUT2</i>						
$R_0$	output resistance	note 7	100	–	–	k $\Omega$
$C_o$	output capacitance	note 7	–	5	7	pF
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)	$V_{DDA} = 8.5 \text{ V}$	12	15	–	V
$I_{bias}$	mixer bias current	AM mode	3.6	4.5	5.4	mA
<i>Mixer</i>						
$g_{m(conv)}$	conversion transconductance $\frac{I_{AMMIX2OUT1}}{V_{IFAMP1IN}}$		1.3	1.6	1.9	$\frac{\text{mA}}{\text{V}}$
$g_{m(conv)(T)}$	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$		–	$-9 \times 10^{-4}$	–	K $^{-1}$
IP3	3rd-order intermodulation	$R_L = 4 \text{ k}\Omega$ (AC load between output pins)	134	137	–	dB $\mu\text{V}$
IP2	2nd-order intermodulation	$R_L = 4 \text{ k}\Omega$ (AC load between output pins)	–	170	–	dB $\mu\text{V}$
$V_{i(n)(eq)}$	equivalent input noise voltage	$R_{gen} = 330 \Omega$ ; $R_L = 4 \text{ k}\Omega$ (AC load between output pins)	–	15	22	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
F	noise figure of AM mixer 2		–	16	19.5	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM IF2 AGC STAGE: PINS AMIF2IN AND AMIF2DEC; note 8						
V <sub>i</sub>	input voltage	for $\alpha = -10$ dB audio attenuation				
		AM soft mute on	–	75	120	$\mu$ V
		AM soft mute off	–	6	10	$\mu$ V
V <sub>AGC(start)</sub>	AGC start voltage	input carrier voltage	–	14	30	$\mu$ V
V <sub>AGC(stop)</sub>	AGC stop voltage	maximum input peak voltage	1	–	–	V
V <sub>AGC(ctrl)</sub>	AGC control voltage	V <sub>i</sub> = 1 mV	4.1	4.3	4.7	V
$\Delta$ AGC	AGC range	between start and stop of AGC; m = 0.8	–	89	–	dB
R <sub>i</sub>	input resistance		1.8	2	2.2	k $\Omega$
C <sub>i</sub>	input capacitance		–	–	5	pF
AM DETECTOR						
V <sub>sens(rms)</sub>	sensitivity voltage (RMS value)	m = 0.3; f <sub>mod</sub> = 400 Hz; B <sub>AF</sub> = 2.5 kHz; R <sub>gen</sub> = 2 k $\Omega$ ; note 8				
		(S+N)/N = 26 dB	–	45	65	$\mu$ V
		(S+N)/N = 46 dB	–	600	900	$\mu$ V
(S+N)/N	maximum signal plus noise-to-noise ratio	m = 0.3; f <sub>mod</sub> = 400 Hz; B <sub>AF</sub> = 2.5 kHz; R <sub>gen</sub> = 2 k $\Omega$	54	60	–	dB
THD	total harmonic distortion	B <sub>AF</sub> = 2.5 kHz; C <sub>AGC</sub> = 22 $\mu$ F; AM IF2 AGC input V <sub>i</sub> = 100 $\mu$ V to 500 mV (RMS)				
		m = 0.8; f <sub>mod</sub> = 400 Hz	–	0.5	1	%
		m = 0.9; f <sub>mod</sub> = 400 Hz	–	1	2	%
		m = 0.8; f <sub>mod</sub> = 100 Hz	–	1.25	2.5	%
		m = 0.9; f <sub>mod</sub> = 100 Hz	–	1.75	3.5	%
RR	ripple rejection	V <sub>DDA2(ripple)</sub> = 100 mV (RMS); f <sub>ripple</sub> = 100 Hz;	30	40	–	dB
t <sub>sw</sub>	FM to AM switching time	C <sub>AGC</sub> = 22 $\mu$ F	–	1000	1500	ms
t <sub>settle</sub>	AM AGC settling time	C <sub>AGC</sub> = 22 $\mu$ F				
		normal operation	–	–	1800	ms
		test mode	–	–	180	ms
<i>Output: pin AMAFIF2</i>						
V <sub>o(rms)</sub>	AM IF2 output voltage (RMS value)	AM stereo; m = 0				
		minimum at V <sub>i</sub> = 14 $\mu$ V	1.5	3	4.5	mV
		maximum at V <sub>i</sub> = 5.0 mV	130	180	230	mV
		AM mono; m = 0.3; f <sub>mod</sub> = 400 Hz; V <sub>i</sub> = 100 $\mu$ V to 500 mV (RMS)	240	290	340	mV
R <sub>o</sub>	output resistance	AM stereo	–	–	500	$\Omega$
		AM mono	–	–	500	$\Omega$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$C_o$	output capacitance	AM mono	–	5	7	pF
AM IF2 LEVEL DETECTOR OUTPUT: PIN $V_{level}$ ; see Fig.3						
$V_{level}$	DC output voltage	$V_i = 10 \mu\text{V}$ to 1 V	0	–	7	V
		$V_i < 1 \mu\text{V}$ ; standard setting of level DAA and level slope	0.1	0.5	0.9	V
		$V_i = 1.4 \text{ mV}$ ; standard setting of level DAA	1.6	2.2	2.8	V
$\Delta V_{level}$	step size for adjustment of level starting point	standard setting of level slope	30	40	50	mV
$V_{level(slope)}$	slope of level voltage	standard setting of level slope	650	800	950	$\frac{\text{mV}}{20 \text{ dB}}$
$\Delta V_{step}$	step size for adjustment of level starting point	$V_i = 1.4 \text{ mV}$	45	60	75	$\frac{\text{mV}}{20 \text{ dB}}$
$B_{level}$	bandwidth of level output voltage		200	300	–	mV
$R_o$	output resistance		–	–	500	$\Omega$
RR	ripple rejection	$V_{DDA1(ripple)} = 100 \text{ mV (RMS)}$ ; $f_{ripple} = 100 \text{ Hz}$ ;	–	40	–	dB
AM NOISE BLANKER; see Fig.4						
<i>Threshold: pin AMNBHOLD</i>						
$V_O$	DC output voltage		4.3	4.6	5.1	V
$t_{sup}$	suppression time		6	7.5	10	$\mu\text{s}$
$f_{trigger}$	trigger sensitivity frequency	$V_p = 200 \text{ mV (peak)}$ ; $V_{level} < 1.8 \text{ V}$	–	1000	–	Hz
		$V_p = 200 \text{ mV (peak)}$ ; $V_{level} > 2.2 \text{ V}$	–	–	100	Hz
		$V_p = 20 \text{ mV (peak)}$	–	–	100	Hz
<i>Noise detector output: pin TRDSMUTE</i>						
$I_{sink(AGC)}$	AM noise blanker AGC sink current	$V_{TRDSMUTE} = 3 \text{ V}$	35	50	65	$\mu\text{A}$
$V_{AGC}$	AM noise blanker AGC voltage	AM mixer 1 input $V_i = 0 \text{ V}$	1.9	2.2	2.5	V
<b>FM signal channel</b>						
FM RF AGC						
<i>Inputs: pins FMMIXIN1 and FMMIXIN2; note 9</i>						
$V_{i(RF)(rms)}$	RF input voltage for start of wide-band AGC (RMS value)	data byte 5: bit 5 = 0, bit 6 = 0	–	4	–	mV
		data byte 5: bit 5 = 1, bit 6 = 0	–	8	–	mV
		data byte 5: bit 5 = 0, bit 6 = 1	–	12	–	mV
		data byte 5: bit 5 = 1, bit 6 = 1	–	16	–	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<i>AGC peak detector output: pin T1FMAGC</i>						
$I_{ch}$	charge current		-350	-600	-850	$\mu\text{A}$
$I_{dis}$	discharge current		15	25	35	$\mu\text{A}$
<i>PIN diode drive output: pin IFMAGC</i>						
$I_{drive}$	drive current	$V_o = 0.5$ to $4.0$ V	8	11.5	15	mA
<i>Level voltage output: pin <math>V_{level}</math></i>						
$V_{th}$	threshold voltage for narrow-band AGC	data byte 5: bit 7 = 1; standard setting of level DAA	500	950	1400	mV
FM RF MIXER						
<i>Reference voltage: pin <math>V_{ref(FMMIX)}</math></i>						
$V_{ref}$	reference voltage	FM mode	6.5	7.1	7.9	V
		AM mode	2.7	3.1	3.4	V
<i>Inputs: pins FMMIXIN1 and FMMIXIN2; note 9</i>						
$V_{i(RF)(max)}$	maximum RF input voltage	1 dB compression point of FM mixer output voltage (peak-to-peak value)	70	100	–	mV
$V_{i(n)(eq)}$	equivalent input noise voltage	$R_{gen} = 600 \Omega$ ; $R_L = 2.8 \text{ k}\Omega$ ; noise of $R_{gen}$ not included	–	2.6	3.1	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
$R_i$	input resistance		–	1.4	–	$\text{k}\Omega$
$C_i$	input capacitance		–	5	7	pF
<i>Outputs: pins MIX1OUT1 and MIX1OUT2; note 5</i>						
$R_o$	output resistance		100	–	–	$\text{k}\Omega$
$C_o$	output capacitance		–	5	7	pF
$I_{bias}$	mixer bias current	FM mode	4.8	6	7.2	mA
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)		3	–	–	V
FM mixer						
$g_{m(conv)}$	conversion transconductance		8.5	12.5	18	$\frac{\text{mA}}{\text{V}}$
$g_{m(conv)(T)}$	conversion transconductance variation with temperature		–	$-1 \times 10^{-3}$	–	$\text{K}^{-1}$
F	noise figure		–	3	4.6	dB
IP3	3rd-order intermodulation		116	119	–	$\text{dB}\mu\text{V}$
IRR	image rejection ratio		25	30	–	dB
IF AMPLIFIER 1						
G	gain	$R_L = 330 \Omega$ ; $V_i = 1$ mV; note 10	13.5	15.5	17.5	dB
F	noise figure		–	10	13	dB
IP3	3rd-order intermodulation		117	120	–	$\text{dB}\mu\text{V}$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<i>Inputs: pins IFAMP1IN and IFAMP1DEC; note 10</i>						
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of IF amplifier 1 output voltage (peak value)	200	–	–	mV
$V_{i(n)(eq)}$	equivalent input noise voltage	$R_{gen} = 330 \Omega$ ; $R_L = 330 \Omega$ ; noise of $R_{gen}$ not included	–	8	10	$\frac{nV}{\sqrt{Hz}}$
$R_i$	input resistance		270	330	390	$\Omega$
$C_i$	input capacitance		–	5	7	pF
<i>Output: pin IFAMP1OUT</i>						
$R_o$	output resistance		270	330	390	$\Omega$
$C_o$	output capacitance		–	5	7	pF
$V_{o(max)(p)}$	maximum output voltage (peak value)		1.2	1.5	–	V
<b>IF AMPLIFIER 2</b>						
G	gain	$R_L = 330 \Omega$ ; $V_i = 1 \text{ mV}$ ; note 11	6.5	8.5	10.5	dB
F	noise figure		–	13	15	dB
IP3	3rd-order intermodulation		127	130	–	dB $\mu$ V
<i>Inputs: pins IFAMP2IN and IFAMP2DEC; note 11</i>						
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of IF amplifier 2 output voltage (peak value)	500	–	–	mV
$V_{i(n)(eq)}$	equivalent input noise voltage	$R_{gen} = 330 \Omega$ ; $R_L = 330 \Omega$ ; noise of $R_{gen}$ not included	–	10	13	$\frac{nV}{\sqrt{Hz}}$
$R_i$	input resistance		270	330	390	$\Omega$
$C_i$	input capacitance		–	5	7	pF
<i>Output: pin IFAMP2OUT</i>						
$R_o$	output resistance		270	330	390	$\Omega$
$C_o$	output capacitance		–	5	7	pF
$V_{o(max)(p)}$	maximum output voltage (peak value)		1.2	1.5	–	V
<b>FM demodulator and level detector; see Figs 5 and 6</b>						
<b>FM LIMITER</b>						
<i>Inputs: pins FMLIMIN and FMLIMDEC; note 12</i>						
G	gain	$R_{gen} = 50 \Omega$	74	80	–	dB
$R_i$	input resistance		270	330	390	k $\Omega$
$C_i$	input capacitance		–	5	7	pF
<i>Outputs: pins QDET1 and QDET2</i>						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	measured between output pins	500	700	–	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM DEMODULATOR						
<i>Limiter decoupling: pin FMLIMDEC</i>						
$R_L$	load resistance		20	–	–	k $\Omega$
$C_L$	load capacitance		–	–	50	pF
<i>RDS MPX inputs: pins FMLIMIN and FMLIMDEC; note 12</i>						
$V_{\text{start(lim)(rms)}}$	start of limiting of RDS MPX output voltage (RMS value)	$\alpha_{AF} = -3$ dB	–	10	15	$\mu$ V
<i>RDS MPX output: pin QRDSMPX</i>						
$V_{o(\text{rms})}$	RDS MPX output voltage (RMS value)	$\Delta f = 22.5$ kHz; $f_{\text{mod}} = 57$ kHz; $V_i = 20$ $\mu$ V to 1 V; note 12	180	230	280	mV
$I_{o(\text{max})}$	maximum RDS MPX output current		–	–	100	$\mu$ A
$R_o$	output resistance		–	–	500	$\Omega$
B	bandwidth RDS MPX output	$C_L = 0$ ; $R_L > 20$ k $\Omega$	200	300	–	kHz
PSRR	power supply ripple rejection	$f_{\text{ripple}} = 100$ Hz to 20 kHz	–	40	–	dB
<i>FM RDS inputs: pins FMLIMIN and FMLIMDEC; note 12</i>						
$V_{\text{start(lim)(rms)}}$	start of limiting of MPX output voltage (RMS value)	$\alpha_{AF} = -3$ dB	–	10	15	$\mu$ V
$V_{o(\text{sens})(\text{rms})}$	sensitivity for MPX output voltage (RMS value)	$\Delta f = 22.5$ kHz; $f_{\text{mod}} = 1$ kHz; de-emphasis = 75 $\mu$ s (S+N)/N = 26 dB (S+N)/N = 46 dB	– –	10 50	15 75	$\mu$ V $\mu$ V
<i>FM MPX output: pin FMMPX; note 12</i>						
$V_{o(\text{rms})}$	MPX output voltage (RMS value)	$\Delta f = 22.5$ kHz; $f_{\text{mod}} = 1$ kHz; de-emphasis = 75 $\mu$ s; $V_i = 20$ $\mu$ V to 1 V;	180	230	280	mV
$\alpha_{AM}$	AM suppression of MPX output	$\Delta f = 22.5$ kHz; $f_{\text{mod}} = 1$ kHz; $m = 0.3$ ; de-emphasis = 75 $\mu$ s $V_i = 500$ $\mu$ V to 300 mV $V_i = 20$ to 500 $\mu$ V $V_i = 300$ mV to 1 V	50 – –	60 40 40	– – –	dB dB dB
$I_{o(\text{max})}$	maximum MPX output current		–	–	100	$\mu$ A
(S+N)/N	maximum signal plus noise-to-noise ratio of MPX output voltage	$\Delta f = 22.5$ kHz; $f_{\text{mod}} = 1$ kHz; de-emphasis = 75 $\mu$ s; $V_i = 10$ mV;	67	70	–	dB
THD	total harmonic distortion of MPX output voltage	$\Delta f = 75$ kHz; $f_{\text{mod}} = 1$ kHz; de-emphasis = 75 $\mu$ s; $V_i = 200$ $\mu$ V to 800 mV	–	0.35	0.7	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B	bandwidth MPX output	$C_L = 0$ ; $R_L > 20 \text{ k}\Omega$	200	–	–	kHz
PSRR	power supply ripple rejection	$f_{\text{ripple}} = 100 \text{ Hz to } 20 \text{ kHz}$	–	40	–	dB
$R_{L(\text{min})}$	minimum load resistance		20	–	–	$\text{k}\Omega$
$R_{o(\text{max})}$	maximum output resistance		–	–	500	$\Omega$
$C_{L(\text{max})}$	maximum load capacitance		–	–	50	pF
<b>MPX MUTE</b>						
$\alpha_{\text{mute}}$	muting depth	during RDS update	60	80	–	dB
$t_{\text{att}}$	attack time MPX mute	$C_{\text{TRDSMUTE}} = 10 \text{ nF}$	0.75	1	1.25	ms
$t_{\text{decay}}$	decay time MPX mute	$C_{\text{TRDSMUTE}} = 10 \text{ nF}$	0.75	1	1.25	ms
<i>RDS update: pin TRDSMUTE</i>						
$I_{\text{dis}}$	discharge current	$V_o = 3 \text{ V}$ ; audio output muted	24	32	38	$\mu\text{A}$
$I_{\text{ch}}$	charge current	$V_o = 3 \text{ V}$ ; audio output not muted	–24	–32	–38	$\mu\text{A}$
<b>DEMODULATOR AFC</b>						
$G_{\text{AFC}}$	AFC gain	$\Delta f = 100 \text{ kHz}$	28	32	–	dB
<i>RDS MPX output: pin RDSMPX; note 12</i>						
$V_{\text{offset(DC)}}$	residual DC offset voltage	$L_{\text{demod}} = \text{typical value}$	–	0.1	1	V
		$V_i = 10 \text{ to } 80 \mu\text{V}$	–	10	30	mV
		$V_i = 80 \mu\text{V to } 800 \text{ mV}$	–	–	–	–
		$L_{\text{demod}} = \pm 6\%$	–	0.240	1	V
		$V_i = 10 \text{ to } 80 \mu\text{V}$	–	25	500	mV
		$V_i = 80 \mu\text{V to } 800 \text{ mV}$	–	–	–	–
<b>FM IF LEVEL DETECTOR OUTPUT: PIN <math>V_{\text{level}}</math>; note 12</b>						
$V_{\text{level}}$	DC output voltage	$V_i = 10 \mu\text{V to } 1 \text{ V}$	0	–	7	V
		$V_i < 1 \mu\text{V}$ ; standard setting of level DAA	0.2	0.6	1.1	V
		$V_i = 1 \text{ mV}$ ; standard setting of level DAA	1.4	1.9	2.5	V
$\Delta V_{\text{level}}$	level starting point for adjustment of step size	standard setting of level slope	30	40	50	mV
$V_{\text{level(slope)}}$	slope of level voltage	standard setting of level slope	650	800	950	$\frac{\text{mV}}{20 \text{ dB}}$
$\Delta V_{\text{step}}$	level slope adjustment of step size	$V_i = 1 \text{ mV}$	45	50	75	$\frac{\text{mV}}{20 \text{ dB}}$
$V_{\text{level(B)}}$	bandwidth of level output voltage	$V_i = 10 \text{ mV}$ ; $f_{\text{mod}} = 22.5 \text{ kHz}$ ; standard setting of DAA	200	300	–	mV
$R_o$	output resistance		–	–	500	$\Omega$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RR	ripple rejection	$V_{DDA1(\text{ripple})} = 100 \text{ mV (RMS)}$ ; $f_{\text{ripple}} = 100 \text{ Hz}$	–	40	–	dB
<b>RDS update</b>						
<i>Output: pin AFHOLD</i>						
$I_{\text{sink(max)}}$	maximum sink current	after first bus transmission with $AF = 1$ (start of RDS update); $V_o = 0.5 \text{ V}$	1.0	1.2	1.4	mA
<i>Output: pin AFSAMPLE</i>						
$I_{\text{sink(max)}}$	maximum sink current	no RDS update in progress; $V_o = 0.5 \text{ V}$	1.0	1.2	1.4	mA
<b>Test mode; note 3</b>						
<i>Temperature compensation diode: pin DAATD</i>						
$V_{i(\text{ext})}$	external input voltage to clock state machine	$V_{\text{DAATD(L)}} = 2.5 \text{ V}$ ; $V_{\text{DAATD(H)}} = 3.5 \text{ V}$	2.5	–	3.5	V
<i>Clock input: pin SCL</i>						
$V_{i(\text{ext})}$	external input voltage to clock DAA	$V_{\text{SCL(L)}} = 0 \text{ V}$ ; $V_{\text{SCL(H)}} = 5 \text{ V}$	0	–	5	V
<i>Time constant output: pin T1AMAGC</i>						
$V_{\text{pulse}}$	enabling voltage of load PLL signal	pin $f_{\text{ref}}$ in test mode	5.1	6	6.9	V

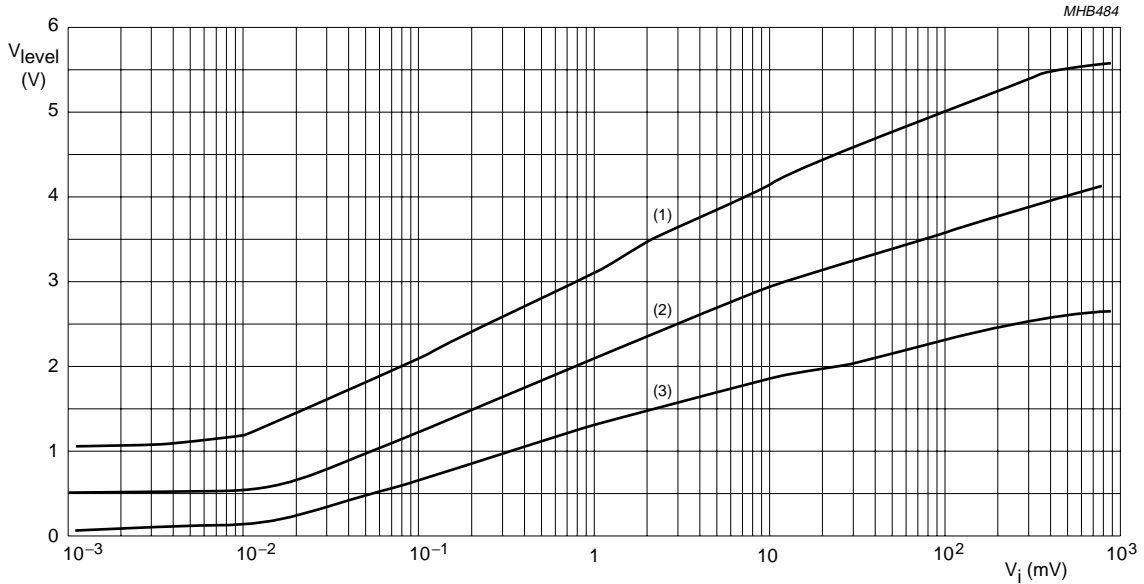
**Notes**

- Measured between pins XTAL1 and XTAL2.
- DAA conversion gain formula:  $V_{\text{DAAOUT}} = \left[ 2 \times \left( 0.75 \times \frac{n}{128} + 0.25 \right) \times (V_{\text{DAAIN}} + V_{\text{DAATD}}) \right] - V_{\text{DAATD}}$   
where  $n = 0$  to 127.
- Reference frequency pin  $f_{\text{ref}}$ :
  - $R_{\text{ext}} = 68 \text{ k}\Omega$  connected to ground, activates the 2nd I<sup>2</sup>C-bus address
  - $R_{\text{ext}} = 100 \text{ k}\Omega$  connected to  $V_{\text{DDA1}}$ , sets the IC into test mode.
- Input parameters of AM mixer 1 measured between pins AMMIX1IN1 and AMMIX1IN2.
- Output parameters of FM mixer and AM mixer 1 measured between pins MIX1OUT1 and MIX1OUT2.
- Input parameters of AM mixer 2 measured between pins IFAMP1IN and IFAMP1DEC.
- Output parameters of AM mixer 2 measured between pins AMMIX2OUT1 and AMMIX2OUT2.
- Input parameters of AM IF2 measured between pins AMIF2IN and AMIF2DEC.
- Input parameters of FM mixer measured between pins FMMIXIN1 and FMMIXIN2.
- Input parameters of IF amplifier 1 measured between pins IFAMP1IN and IFAMP1DEC.
- Input parameters of IF amplifier 2 measured between pins IFAMP2IN and IFAMP2DEC.
- Input parameters of FM limiter measured between pins FMLIMIN and FMLIMDEC.



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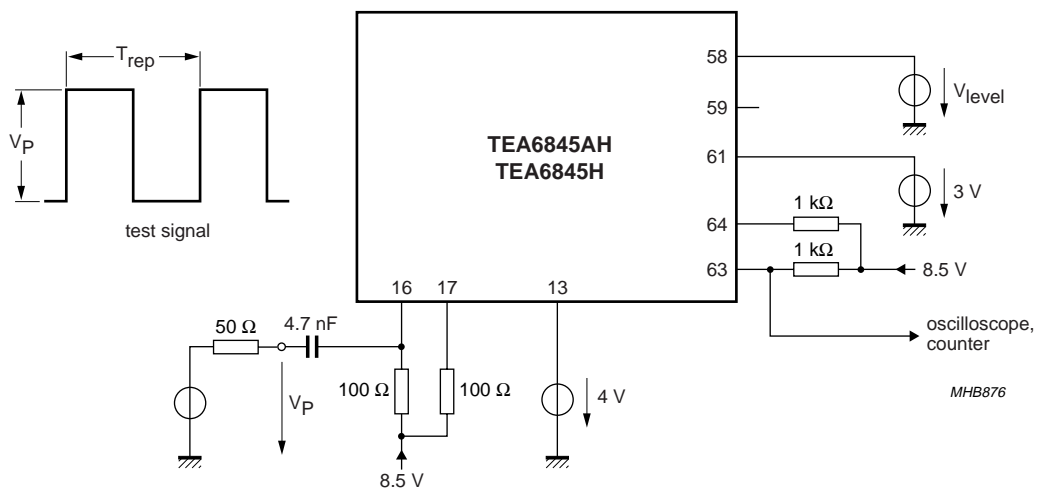
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- (1) Level DAA setting byte 6 = FFH.
- (2) Level DAA setting byte 6 = 84H (standard setting).
- (3) Level DAA setting byte 6 = 00H.

$$V_i = V_{AMIF2IN} - V_{AMIF2DEC}$$

Fig.3 AM level output voltage (DAA) as a function of AM level circuit input voltage.

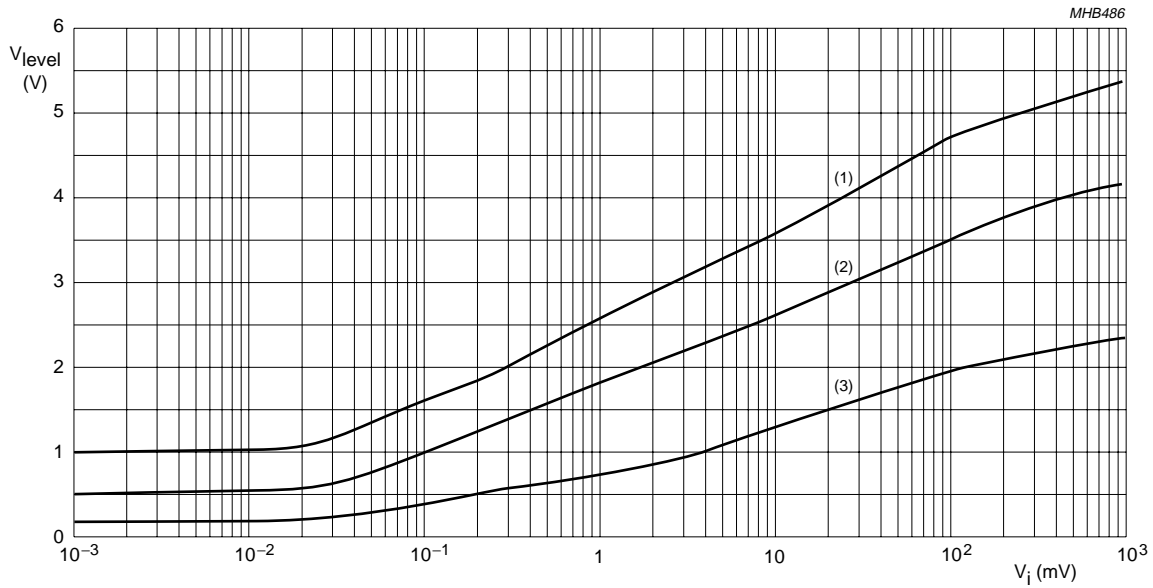


Test signal:  $T_{rep} = 2 \text{ ms}$ ,  $t_r < 50 \text{ ns}$ ,  $t_f < 50 \text{ ns}$ , and duty factor 50%.

Fig.4 Test circuit for AM noise blanker.

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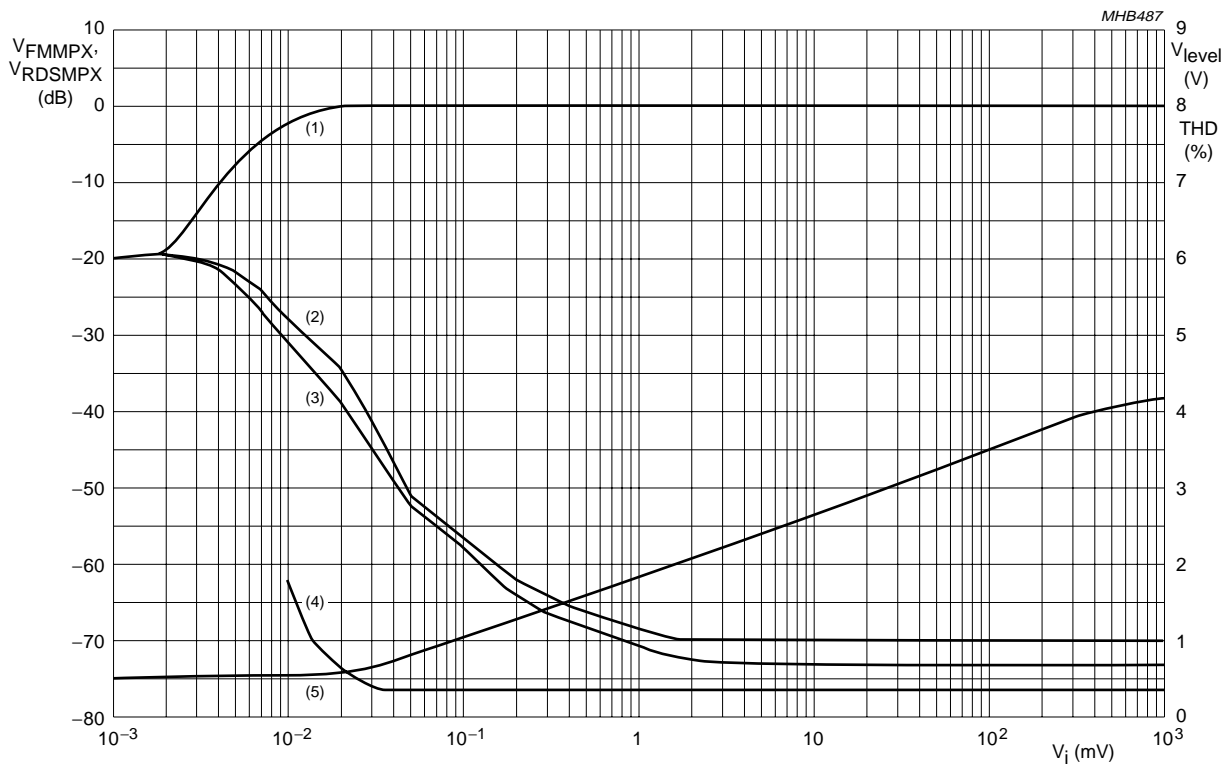
- (1) Level DAA setting byte 6 = FFH.
- (2) Level DAA setting byte 6 = 84H (standard setting).
- (3) Level DAA setting byte 6 = 00H.

$$V_i = V_{FMLIMIN} - V_{FMLIMDEC}$$

Fig.5 FM level output voltage (DAA) as a function of FM limiter and level circuit input voltage.

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- (1) Output voltage for FMMPX and RDSMPX:  $f_{IF} = 10.7$  MHz;  $\Delta f = 22.5$  kHz;  $f_{mod} = 1$  kHz.
- (2) Noise: unweighted B = 250 Hz to 15 kHz with de-emphasis 50  $\mu$ s for FMMPX.
- (3) Noise: unweighted B = 250 Hz to 15 kHz with de-emphasis 50  $\mu$ s for RDSMPX.
- (4) THD for FMMPX and RDSMPX.
- (5) Level for standard setting of level DAA, byte 6 = 84H.

$$V_i = V_{FMLIMIN} - V_{FMLIMDEC}$$

Fig.6 (S+N)/N, THD and level output voltage for FM mode as a function of FM demodulator input voltage.

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**12 I<sup>2</sup>C-BUS PROTOCOL****12.1 I<sup>2</sup>C-bus specification**

Information about the I<sup>2</sup>C-bus can be found in the brochure "The I<sup>2</sup>C-bus and how to use it" (order number 9398 393 40011).

The standard I<sup>2</sup>C-bus specification is expanded by the following definitions.

IC addresses:

- 1st IC address C2: 1100001
- 2nd IC address C0: 1100000.

Structure of the I<sup>2</sup>C-bus logic: slave transceiver with auto increment.

Subaddresses are not used.

**12.1.1 TEST MODE**

Connecting pin  $f_{ref}$  to  $V_{DDA1}$  via a 100 k $\Omega$  resistor or feeding 50  $\mu$ A into that pin switches the IC into the test mode.

During test mode the digital-to-analog converters of the level and antenna DAA functions can be sequenced by the I<sup>2</sup>C-bus SCL line.

During test mode either the TEA6880H or TEF6890H reference frequency, the PLL reference frequency divider or the programmable divider output can be switched to pin  $f_{ref}$ .

**12.1.2 DATA TRANSFER FOR THE TEA6845**

Data sequence: address, byte 1, byte 2, byte 3, byte 4, byte 5, and byte 6. The data transfer has to be in this order. The LSB = 0 indicates a WRITE operation to the TEA6845.

Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.

The data becomes valid at the output of the internal latches with the acknowledge of each byte. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, this byte is lost and the previous information is available.

In byte 5, 4 bits are reserved for test mode purposes. Those can only be used when the test mode is activated by the select pin  $f_{ref}$ .

**12.1.3 I<sup>2</sup>C-bus PULL-UP RESISTORS**

When the IC is used together with the TEA6880H or TEF6890H and both SCL and SDA lines are connected via the I<sup>2</sup>C-bus to the TEA6880H or TEF6890H, the pull-up resistors of the tuner IC should be connected to the digital supply voltage of the TEA6880H or TEF6890H. Otherwise an I<sup>2</sup>C-bus pull-down can occur switching off the tuner IC supply when the I<sup>2</sup>C-bus buffer interface of the TEA6880H or TEF6890H is enabled for data transfer to the tuner IC.

**12.1.4 FREQUENCY SETTING**

For new frequency setting, in both AM and FM mode, the programmable divider is enabled by setting bit MUTE = 1. To select an FM frequency, two I<sup>2</sup>C-bus transmissions are necessary:

- First: bit MUTE = 1
- Second: bit MUTE = 0.

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**12.2 I<sup>2</sup>C-bus protocol**

## 12.2.1 DATA TRANSFER MODE AND IC ADDRESS

**Table 1** Write mode

S <sup>(1)</sup>	address (write)	A <sup>(2)</sup>	data byte(s)	A <sup>(2)</sup>	P <sup>(3)</sup>
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**Table 2** Read mode

S <sup>(1)</sup>	address (read)	A <sup>(2)</sup>	data byte 1
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**Notes to Tables 1 and 2**

1. S = START condition.
2. A = acknowledge.
3. P = STOP condition.

**Table 3** IC address byte

IC ADDRESS							MODE
1	1	0	0	0	0	0/1 <sup>(1)</sup>	R/W <sup>(2)</sup>

**Notes**

1. Defined by address pin  $f_{ref}$ :
  - a) 1 = 1st IC address
  - b) 0 = 2nd IC address.
2. Read or write mode:
  - a) 0 = write operation to TEA6840H
  - b) 1 = read operation from TEA6840H.

## 12.2.2 WRITE MODE: DATA BYTE 1

**Table 4** Format of data byte 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AF	PCA6	PCA5	PCA4	PCA3	PCA2	PCA1	PCA0

**Table 5** Description of data byte 1 bits

BIT	SYMBOL	DESCRIPTION
7	AF	<b>Alternative frequency.</b> If AF = 0, then normal operation. If AF = 1, then AF (RDS) update mode.
6 to 0	PCA[6:0]	<b>Setting of programmable counter of synthesizer PLL.</b> Upper byte of PLL divider word.

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## 12.2.3 WRITE MODE: DATA BYTE 2

**Table 6** Format of data byte 2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PCB7	PCB6	PCB5	PCB4	PCB3	PCB2	PCB1	PCB0

**Table 7** Description of data byte 2 bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PCB[7:0]	<b>Setting of programmable counter of synthesizer PLL.</b> Lower byte of PLL divider word.

## 12.2.4 WRITE MODE: DATA BYTE 3

**Table 8** Format of data byte 3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MUTE	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0

**Table 9** Description of data byte 3 bits

BIT	SYMBOL	DESCRIPTION
7	MUTE	<b>FM audio mute.</b> If MUTE = 0, then FM audio not muted. If MUTE = 1, then FM audio muted; writing to programmable divider enabled.
6 to 0	DAA[6:0]	<b>Setting of antenna digital auto alignment.</b>

## 12.2.5 WRITE MODE: DATA BYTE 4

**Table 10** Format of data byte 4

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IFMT	RFS2	RFS1	RFS0	IFPR	BND1	BND0	AMFM

**Table 11** Description of data byte 4 bits

BIT	SYMBOL	DESCRIPTION
7	IFMT	<b>IF measuring time.</b> If IFMT = 0, then IF measuring time is 20 ms. If IFMT = 1, then IF measuring time is 2 ms.
6 to 4	RFS[2:0]	<b>Reference frequency for synthesizer.</b> These 3 bits determine the reference frequency, see Table 12.
3	IFPR	<b>IF counter prescaler ratio.</b> If IFPR = 0, then IF prescaler ratio is 100. If IFPR = 1, then IF prescaler ratio is 10.
2 and 1	BND[1:0]	<b>Band switch.</b> These 2 bits select in FM mode band and local or distant, see Table 13; in AM mode band and AM stereo, see Table 14.
0	AMFM	<b>AM or FM switch.</b> If AMFM = 0, then FM mode. If AMFM = 1, then AM mode

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**Table 12** Reference frequency setting

RFS2	RFS1	RFS0	f <sub>ref</sub> (kHz)
0	0	0	100
1	0	0	50
0	1	0	25
1	1	0	20
0	0	1	10
1	0	1	10
0	1	1	10
1	1	1	10

**Table 13** FM mode

BND1	BND0	SELECTION
0	0	FM standard: dead zone high current charge pump active, FM AGC defined by RF level and threshold level setting by I <sup>2</sup> C-bus
0	1	FM local: dead zone high current charge pump active, FM AGC source current set to maximum
1	0	FM East Europe: dead zone high current charge pump switched off, current of low current charge pump set to 1 mA
1	1	FM weather band: N1 divider set to 1 and I and Q phase shift network switched on, WX flag signal activated

**Table 14** AM mode; note 1

BND1	BND0	SELECTION
0	0	AM mono; N2 divider set to 5 (SW)
0	1	AM stereo; N2 divider set to 5 (SW)
1	0	AM mono; N2 divider set to 10 (LW, MW)
1	1	AM stereo; N2 divider set to 10 (LW, MW)

**Note**

1. In AM mode dead zone high current charge pump switched off, current of low current charge pump set to 1 mA.

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## 12.2.6 WRITE MODE: DATA BYTE 5

**Table 15** Format of data byte 5

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
KAGC	WBA1	WBA0	AMSM	TMS3	TMS2	TMS1	TMS0

**Table 16** Description of data byte 5 bits

BIT	SYMBOL	DESCRIPTION
7	KAGC	<b>Keyed FM AGC.</b> If KAGC = 0, then keyed FM AGC is off. If KAGC = 1, then keyed FM AGC is on.
6 and 5	WBA[1:0]	<b>Wide band AGC.</b> These 2 bits set the start value of wide band AGC. For AM, see Table 17 and for FM, see Table 18.
4	AMSM	<b>AM soft mute.</b> If AMSM = 0, then AM soft mute is off. If AMSM = 1, then AM soft mute is on.
3	TMS3	<b>In test mode charge pump 3-state.</b> If TMS3 = 0, then 3-state off. If TMS3 = 1, then 3-state on.
2	TMS2	<b>In test mode external clock for level and antenna DAA.</b> If TMS2 = 0, then external clock disabled. If TMS2 = 1, then external clock enabled.
1 and 0	TMS[1:0]	<b>In test mode setting of pin <math>f_{ref}</math>.</b> These 2 bits define the function of pin $f_{ref}$ , see Table 19.

**Table 17** Setting of wide band AGC for AM

WBA1	WBA0	AM MIXER 1 INPUT VOLTAGE (PEAK VALUE) (mV)
0	0	150
0	1	275
1	0	400
1	1	525

**Table 18** Setting of wide band AGC for FM

WBA1	WBA0	FM RF MIXER 1 INPUT VOLTAGE (RMS VALUE) (mV)
1	1	4
1	0	8
0	1	12
0	0	16

**Table 19** Setting function of pin  $f_{ref}$  in test mode

TMS1	TMS0	OUTPUT AT PIN $f_{ref}$
0	0	reference frequency of TEA6880H or TEF6890H
0	1	tuner oscillator frequency divided by division ratio of programmable divider
1	0	PLL synthesizer reference frequency
1	1	not used (no output)



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## 12.2.7 WRITE MODE: DATA BYTE 6

**Table 20** Format of data byte 6

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0

**Table 21** Description of data byte 6 bits

BIT	SYMBOL	DESCRIPTION
7 to 3	LST[4:0]	<b>Setting of level DAA starting point.</b> These 5 bits determine the offset of the level detector output voltage.
2 to 0	LSL[2:0]	<b>Setting of level DAA slope.</b> These 3 bits determine the steepness of the level detector output voltage.

**Table 22** Standard setting of data byte 6 bits

SETTING OF LEVEL DAA STARTING POINT					SETTING OF LEVEL DAA SLOPE		
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0
1	0	0	0	0	1	0	0

## 12.2.8 READ MODE: DATA BYTE 1

**Table 23** Format of 1st data byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IFC7	IFC6	IFC5	IFC4	IFC3	IFC2	IFC1	IFC0

**Table 24** Description of data byte 1 bits

BIT	SYMBOL	DESCRIPTION
7 to 0	IFC[7:0]	<b>IF counter result.</b> These bits contain the last eight bits of the IF counter result.

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13 TEST AND APPLICATION INFORMATION

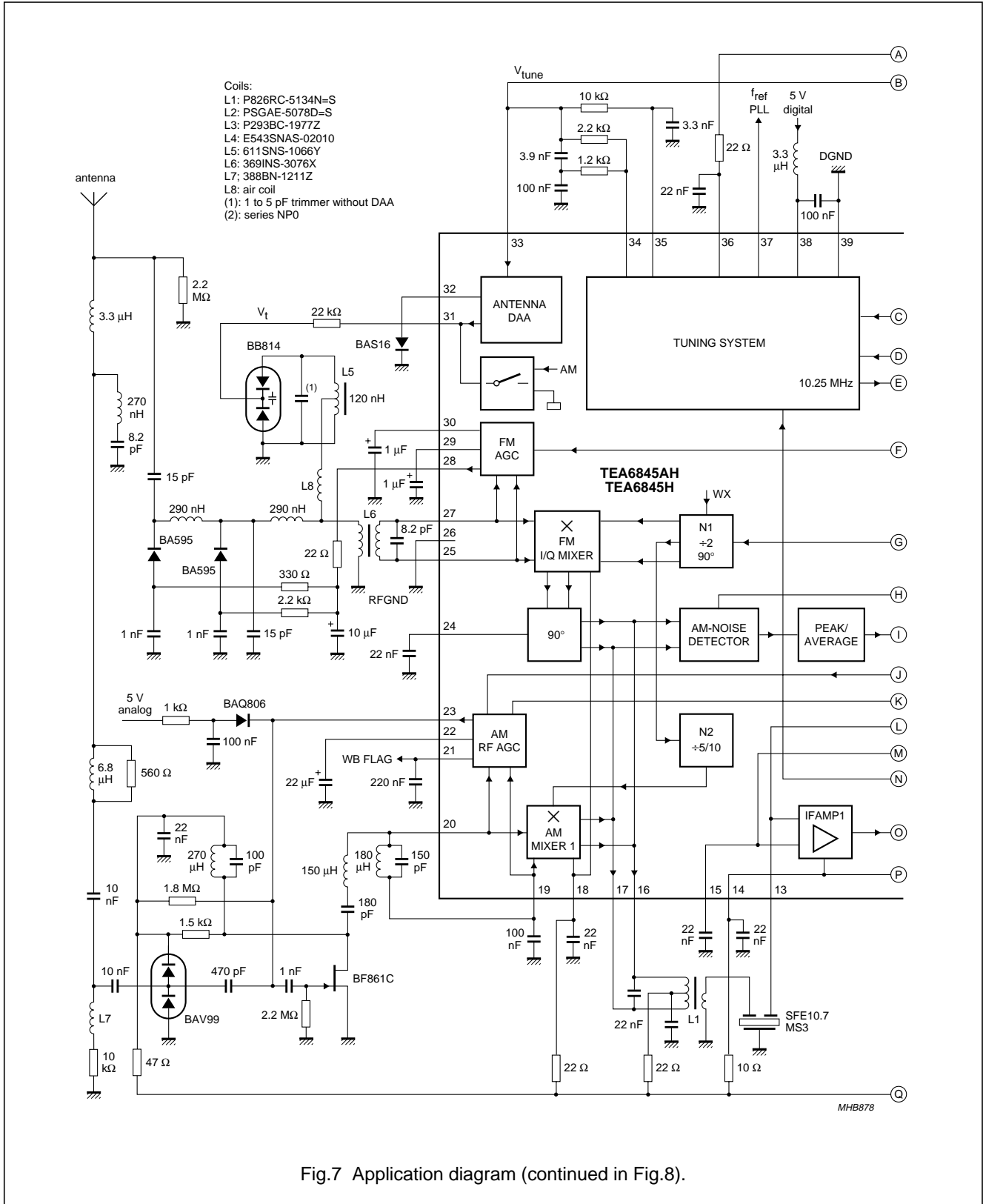


Fig.7 Application diagram (continued in Fig.8).

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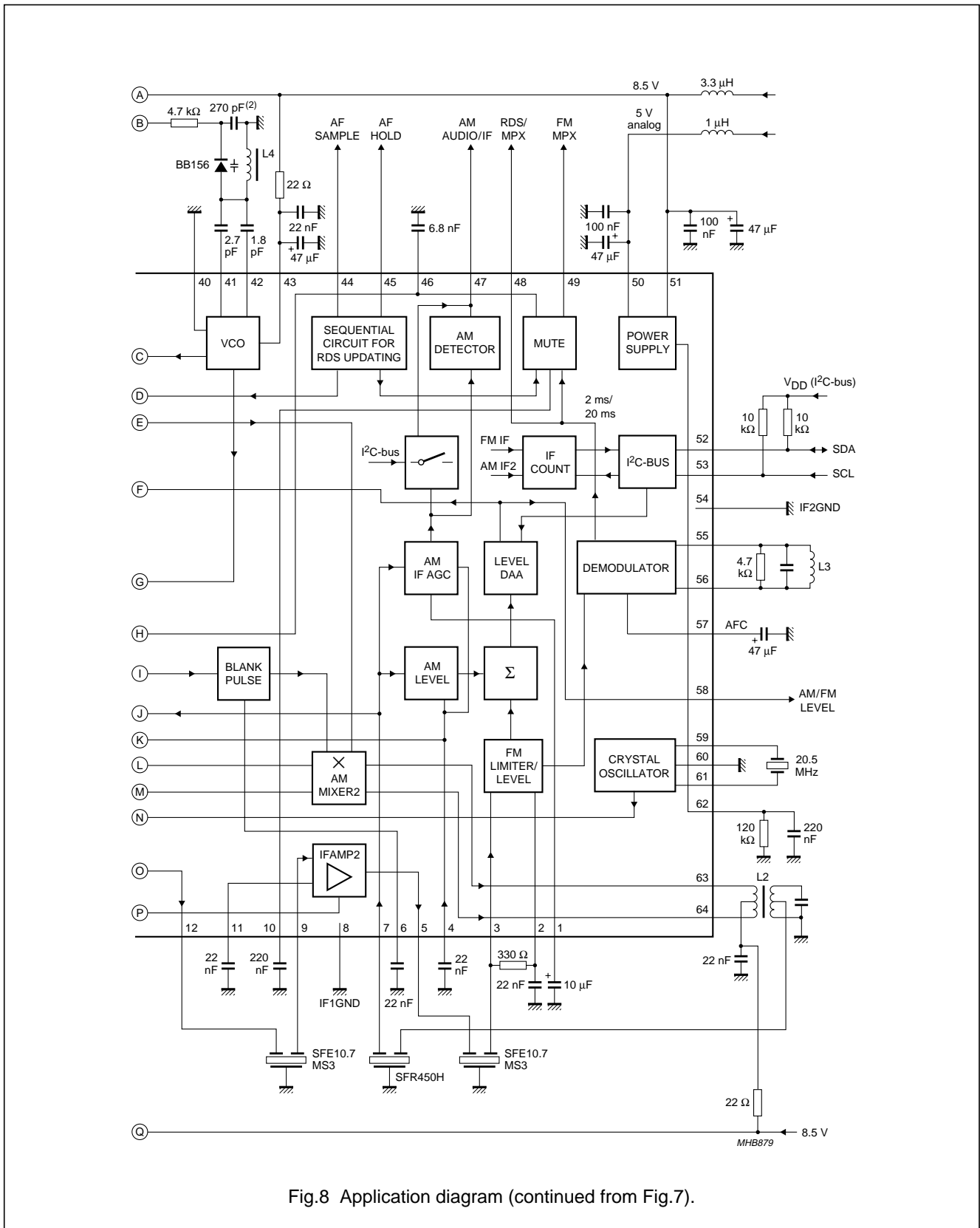


Fig.8 Application diagram (continued from Fig.7).

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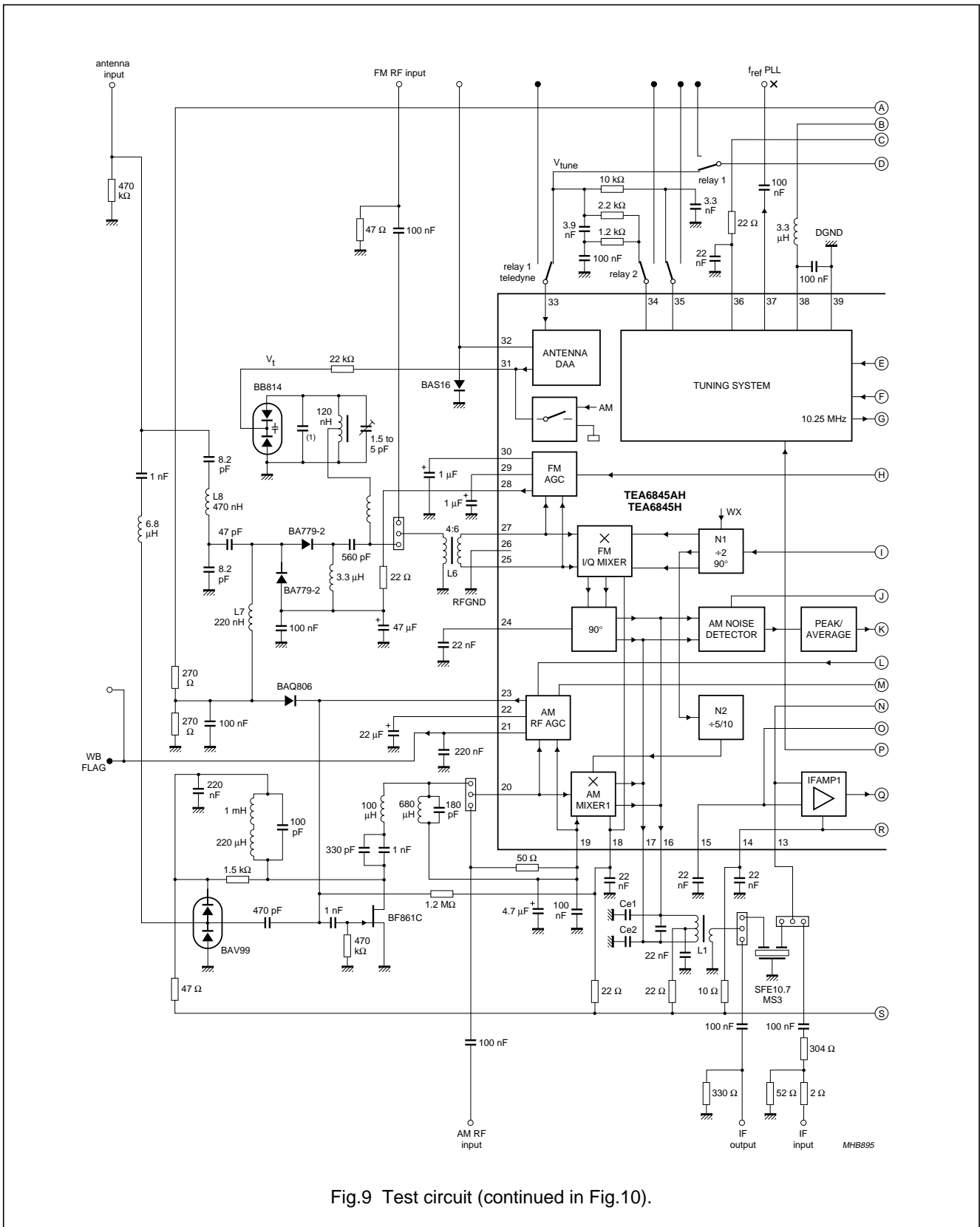


Fig.9 Test circuit (continued in Fig.10).

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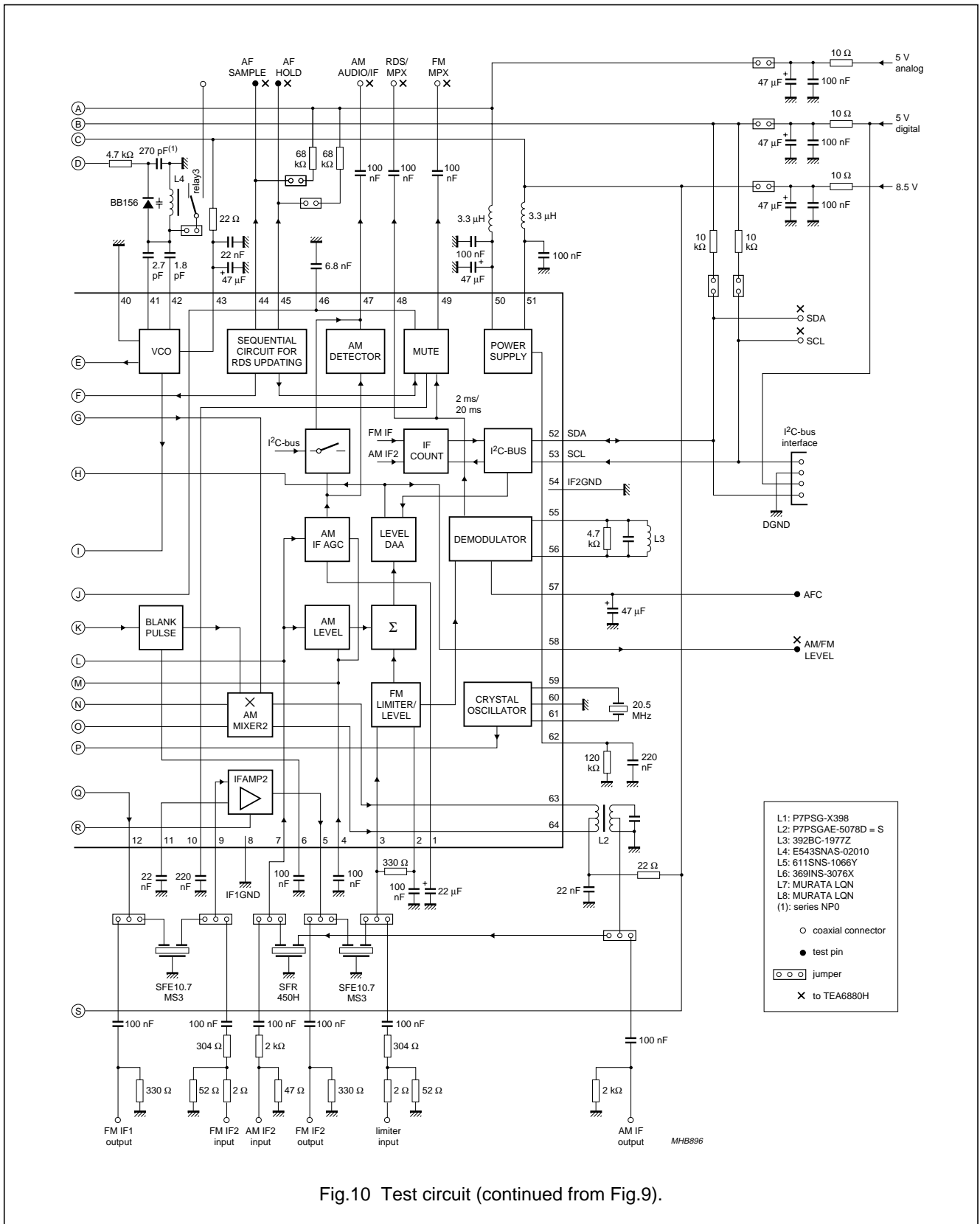


Fig.10 Test circuit (continued from Fig.9).

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Table 25 DC operating points

SYMBOL	PIN	UNLOADED DC VOLTAGE (V)					
		AM MODE			FM MODE		
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
C <sub>AGC</sub>	1	3.6	4.3	4.8	4.1	4.6	5.1
FMLIMDEC	2	2.5	3	3.5	2.5	2.8	3.1
FMLIMIN	3	2.5	3	3.5	2.5	2.8	3.1
AMIF2DEC	4	2.4	2.7	3.2	floating		
IFAMP2OUT	5	7.2	7.9	–	3.4	3.9	4.4
AMNBHOLD	6	4.3	4.6	5.1	8	8.4	–
AMIF2IN	7	2.4	2.7	3.2	floating		
IF1GND	8	external 0			external 0		
IFAMP2IN	9	3	4	5	2.7	3.1	3.5
C <sub>offset</sub>	10	floating			3	3.5	4
IFAMP2DEC	11	3	4	5	2.7	3.1	3.5
IFAMP1OUT	12	7.2	7.9	–	3.6	4	4.4
IFAMP1IN	13	2.4	2.7	3	2.3	2.7	3.1
V <sub>DDA6</sub>	14	external 8.5			external 8.5		
IFAMP1DEC	15	2.4	2.7	3	2.3	2.7	3.1
MIX1OUT1	16	external 8.5			external 8.5		
MIX1OUT2	17	external 8.5			external 8.5		
V <sub>DDA5</sub>	18	external 8.5			external 8.5		
AMMIX1IN1	19	2.3	2.75	3.1	floating		
AMMIX1IN2	20	2.3	2.75	3.1	floating		
T1AMAGC	21	0	2.8	4.6	0 (no WX)	0.3 (no WX)	0.5 (no WX)
T2AMAGC	22	2.5	2.8	3.1	floating		
IAMAGC	23	open-collector			open-collector		
V <sub>ref(FMMIX)</sub>	24	2.7	3.1	3.4	6.5	7.1	7.9
FMMIXIN1	25	1	1.3	1.6	2.3	2.8	3.3
RFGND	26	external 0			external 0		
FMMIXIN2	27	1	1.3	1.6	2.3	2.8	3.3
IFMAGC	28	floating			1.5 (external biasing)	–	4 (external biasing)
T2FMAGC	29	7.5	8	8.3	3.9	4.6	5.3
T1FMAGC	30	floating			1	–	7
DAAOUT	31	–	0.2	0.3	0.2	–	8.25
DAATD	32	floating			0.2	–	1.5
DAAIN	33	0	–	8.5	0	–	8.5
V <sub>tune</sub>	34	0	–	8.5	0	–	8.5
CPOUT	35	0	–	8.5	0	–	8.5
V <sub>DDA4</sub>	36	external 8.5			external 8.5		

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SYMBOL	PIN	UNLOADED DC VOLTAGE (V)					
		AM MODE			FM MODE		
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
$f_{ref}$	37	3.2	3.4	3.7	3.2	3.4	3.7
$V_{DDD}$	38	external 5			external 5		
DGND	39	external 0			external 0		
VCOGND	40	external 0			external 0		
OSCFDB	41	2.2	2.8	3.4	2.2	2.8	3.4
OSCTNK	42	5	6.1	7.2	5	6.1	7.2
$V_{DDA3}$	43	external 8.5			external 8.5		
AFSAMPLE	44	0	0.2	0.5	0	0.2	0.5
AFHOLD	45	open-collector			open-collector		
TRDSMUTE	46	1.9	2.2	2.5	0.7 (muted)	1.2 (muted)	1.7 (muted)
					5.2 (not muted)	5.7 (not muted)	6.2 (not muted)
AMAFIF2	47	4	4.3	4.6	floating		
RDSMPX	48	floating			2.6	3.1	3.3
FMMPX	49	floating			3	3.5	4
$V_{DDA2}$	50	external 5			external 5		
$V_{DDA1}$	51	external 8.5			external 8.5		
SDA	52	4.8	5	5.2	4.8	5	5.2
SCL	53	4.8	5	5.2	4.8	5	5.2
IF2GND	54	external 0			external 0		
QDET1	55	floating			3.6	4.1	4.6
QDET2	56	floating			3.6	4.1	4.6
$C_{AFC}$	57	floating			1.2	3.4	4.1
$V_{level}$	58	0.05	–	7	0	–	7
XTAL1	59	1.7	2.1	2.5	1.7	2.1	2.5
XTALGND	60	external 0			external 0		
XTAL2	61	1.7	2.1	2.5	1.7	2.1	2.5
$I_{ref}$	62	4	4.25	4.5	4	4.25	4.5
AMMIX2OUT1	63	external 8.5			external 8.5		
AMMIX2OUT2	64	external 8.5			external 8.5		

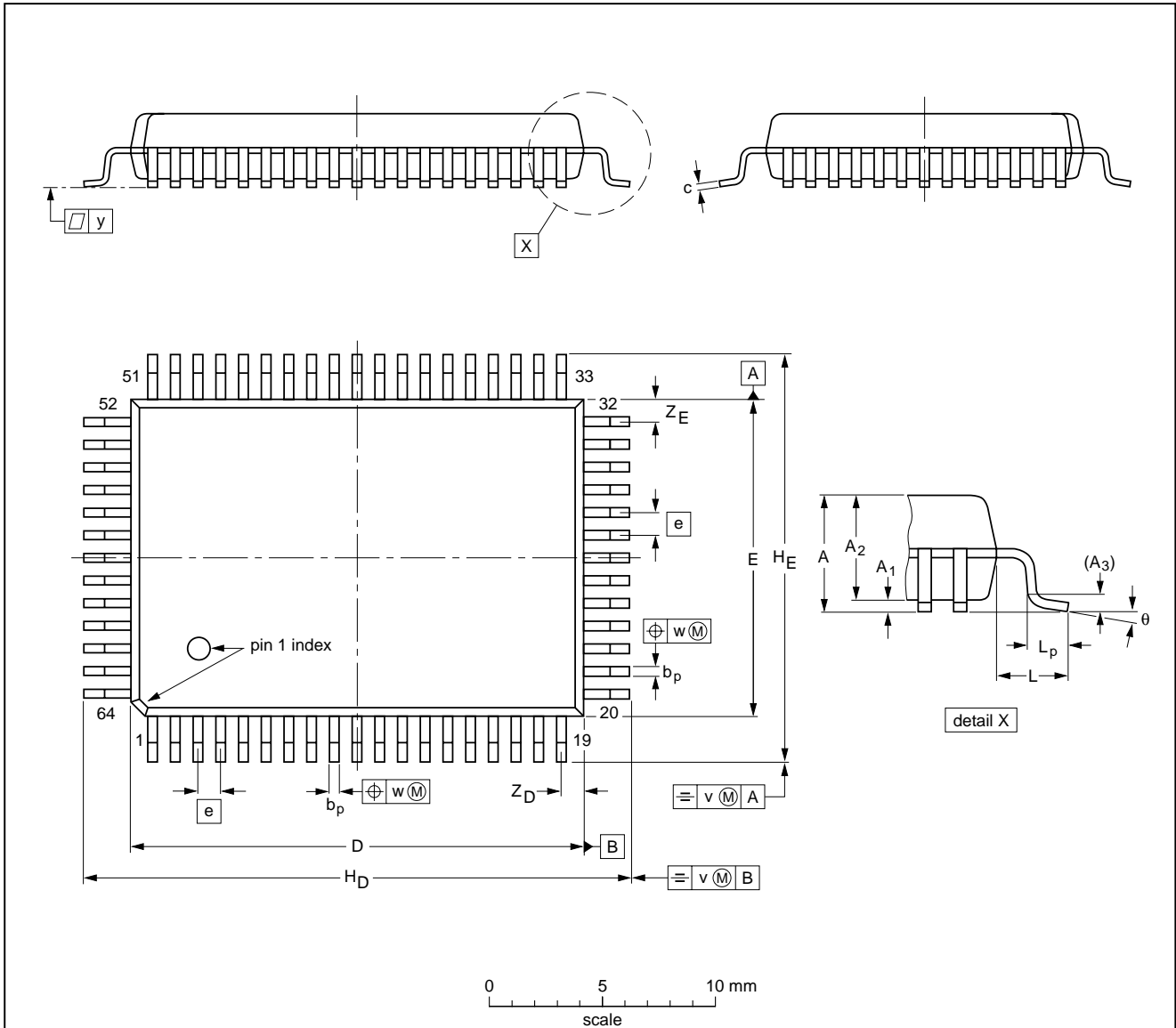
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14 PACKAGE OUTLINES

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm

SOT319-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2		MO-112				97-08-01 99-12-27

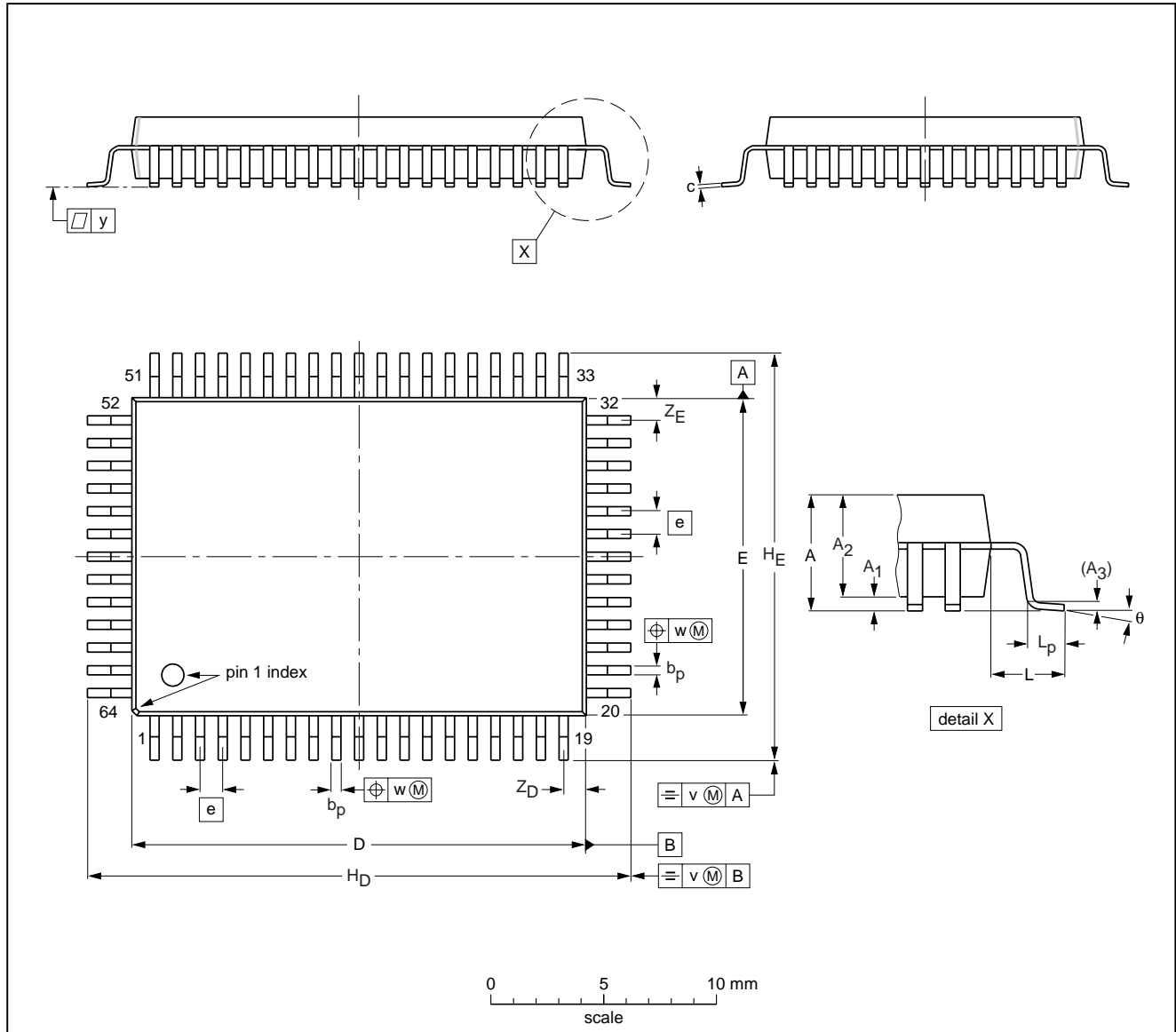


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QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm

SOT319-5



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	3.40	0.60 0.25	3.05 2.55	0.25	0.50 0.35	0.23 0.11	20.1 19.9	14.1 13.9	1.0	24.2 23.6	18.2 17.6	1.95	1.03 0.73	0.20	0.2	0.10	1.23 0.78	1.23 0.78	7° 0°

**Note**  
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-5		MO-112CA1				99-06-03

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**15 SOLDERING****15.1 Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

**15.2 Reflow soldering**

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

**15.3 Wave soldering**

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

**15.4 Manual soldering**

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## 15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

## Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## 16 DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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## Notes

- Please consult the most recently issued data sheet before initiating or completing a design.
- The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**17 DEFINITIONS**

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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