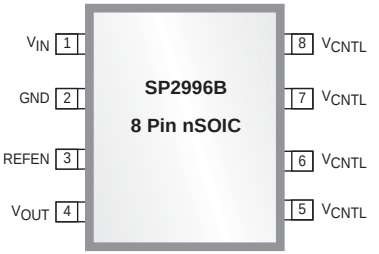
2A Bus Termination Regulator

FEATURES

- Capable of sourcing and sinking 2A Continuous current
- Supports both DDR1 ($1.25V_{TT}$) and DDR2 ($0.9V_{TT}$) requirements
- Low Output Voltage Offset, ± 20mV
- Thermal and Current Limit Protection
- Integrated Power MOSFETs
- Generates Termination for SSTL-2
- High Accuracy Output at Full Load
- Adjustable V_{OUT} by External Resistors
- Minimal External Components
- Available in 8 pin NSOIC package



Now Available in Lead Free Packaging

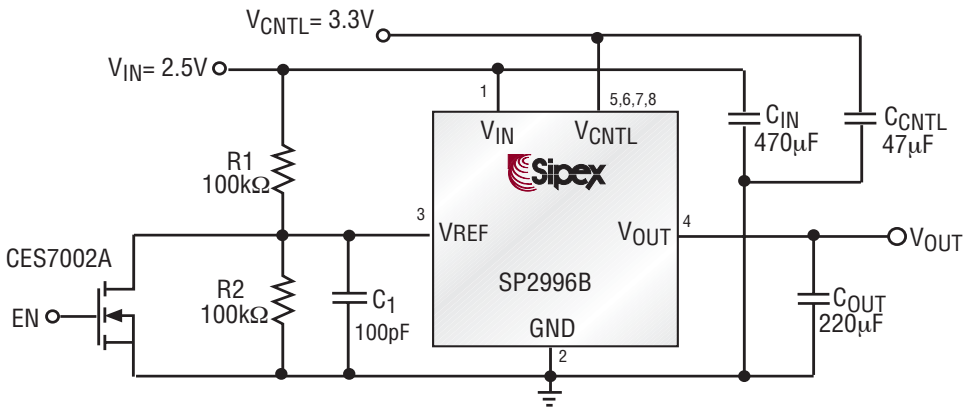
APPLICATIONS

- DDR Memory Termination
- Active Bus Termination
- Supply Splitter

DESCRIPTION

The SP2996B voltage regulator is designed to convert voltage supplies ranging from 1.6V to 6V into a desired output voltage which is adjusted by an external resistor divider. The regulator is capable of sourcing or sinking up to 2A of Continuous current while regulating an output voltage to within 20mV. The SP2996B provides an excellent voltage source for active termination schemes of high speed transmission lines such as those seen in high speed memory buses and distributed backplane designs when used in conjunction with series termination resistors. The voltage output of the regulator can be used as a termination voltage for DDR SDRAM, and it meets the JEDEC SSTL-2 and SSTL-3 specifications . Current limits in both sourcing and sinking mode, plus on-chip thermal shutdown make the circuit tolerant of output fault conditions.

TYPICAL APPLICATIONS CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... -0.4V to 7V
Operating Temperature Range.....-40°C to +85°C
Junction Temperature ....125°C
Storage Temperature Range.....-65°C to +150°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 2.5V, V_{CTRL} = 3.3V, V_{REF} = 0.5V_{IN}, C_{OUT} = 10µF (Ceramic), T_A = 25ºC, unless otherwise specified. (Note 1)

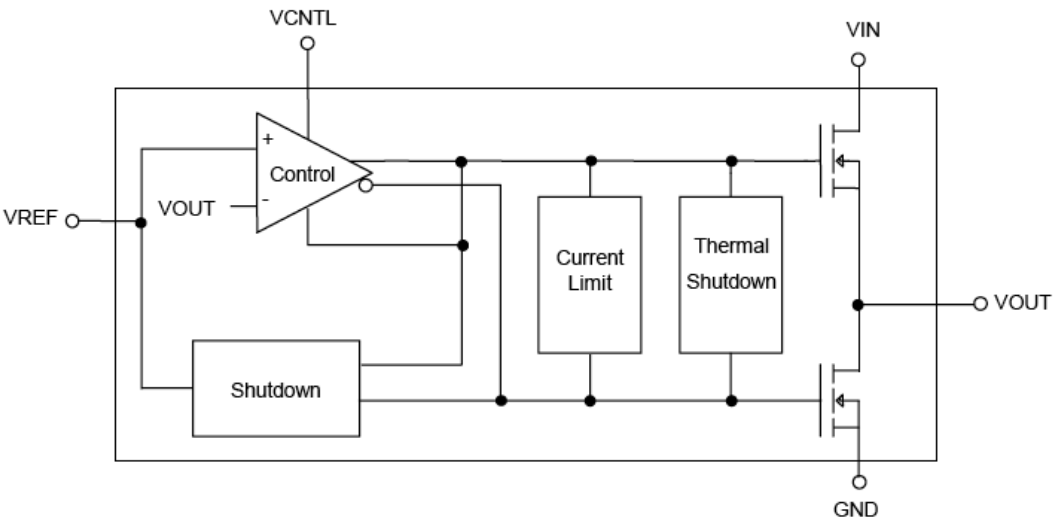
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage Range (DDR 1/2) (Note 5)	V_{IN}	Keep $V_{CTRL} \geq V_{IN}$ on operation power on and power off sequences	1.6	2.5/1.8	-	V
	V_{CNTL}	I_{OUT} = 0mA	3.0	3.3	6	
Output Voltage	V_{OUT}	I_{OUT} = 0mA		V_{REF}		V
Output Offset Voltage	V_{OS}	No Load	-20	-	20	mV
Load Regulation (DDR 1/2)	ΔV_{LOR}	I_{OUT} = 0.1mA to +2A	-	10	25	mV
		I_{OUT} = 0.1mA to -2A	-	10	25	
Quiescent Current	I_Q	V_{REF} < 0.2V, V_{OUT} = OFF	-	8	30	µA
Operating Current of V_{CNTL}	I_{CNTL}	No Load	-	3	10	mA
Bias Current of V_{REF}		V_{REF} = 1.25V	-	-	1	µA
Current Limit	I_{IL}	Note 4	2.2	3	4.5	A
Thermal Protection						
Thermal Shutdown Temperature (Note 5)	T_{SD}	3.3V ≤ V_{CNTL} ≤ 5V Guaranteed by design	125	150	-	ºC
Thermal Shutdown Hysteresis		Guaranteed by design	-	30	-	ºC
Shutdown Specifications						
Shutdown Threshold	$V_{TRIGGER}$	Output ON (V_{REF} = ZeroV ---->1 .25V)	0.8	-	-	V
Shutdown Threshold	$V_{TRIGGER}$	Output OFF (V_{REF} = 1.25V ----> ZeroV)	-	-	0.2	

Note 1 . Specifications are tested for production at T_A = 25ºC . Specifications over the -40ºC to 85ºC operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).
Note 2. V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REF}.
Note 3. Load regulation is measured at constant junction temperature, using pulse testing with a low ON time.
Note 4. Current limit is measured by pulsing a short time.
Note 5. In order to safely operate your system, V_{CTRL} must be > V_{IN}.

PIN DESCRIPTIONS

Pin Name	Pin Number	Description (8 pin NSOIC)
V_{IN}	1	Power Input Voltage
GND	2	Ground
REFEN	3	Reference Voltage Input
V_{OUT}	4	Output Voltage
V_{CNTL}	5	Voltage for the driver circuit and all analog blocks
V_{CNTL}	6	Voltage for the driver circuit and all analog blocks
V_{CNTL}	7	Voltage for the driver circuit and all analog blocks
V_{CNTL}	8	Voltage for the driver circuit and all analog blocks

BLOCK DIAGRAM



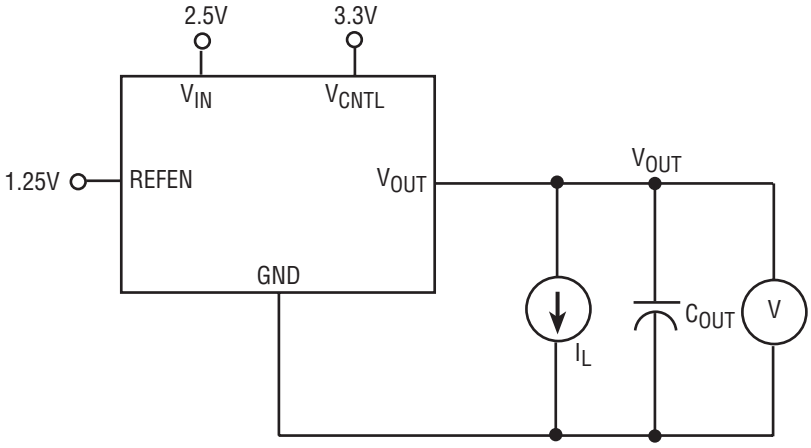


Figure 1. Output Voltage Tolerance, ΔV_{LOAD}

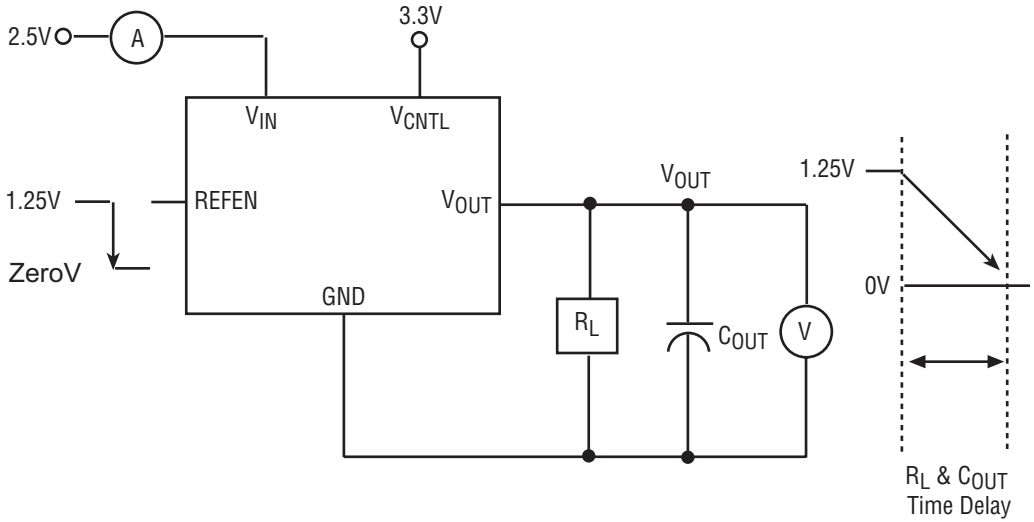


Figure 2. Current in Shutdown Mode, I_{SHDN}

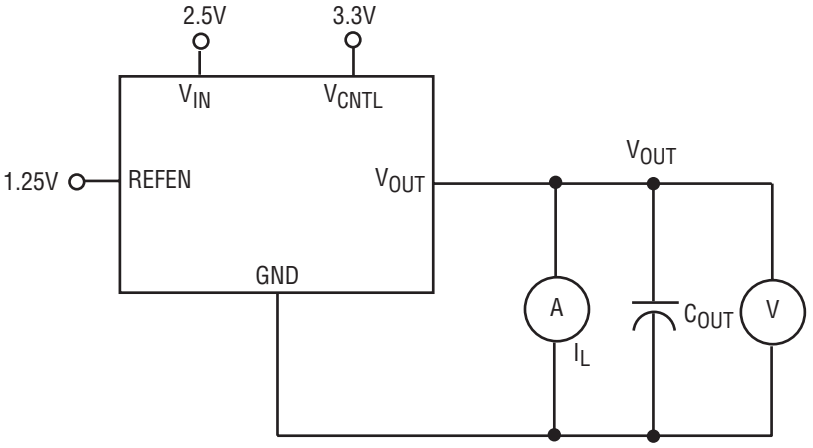


Figure 3. Current Limit for High Side, I_{LIMIT}

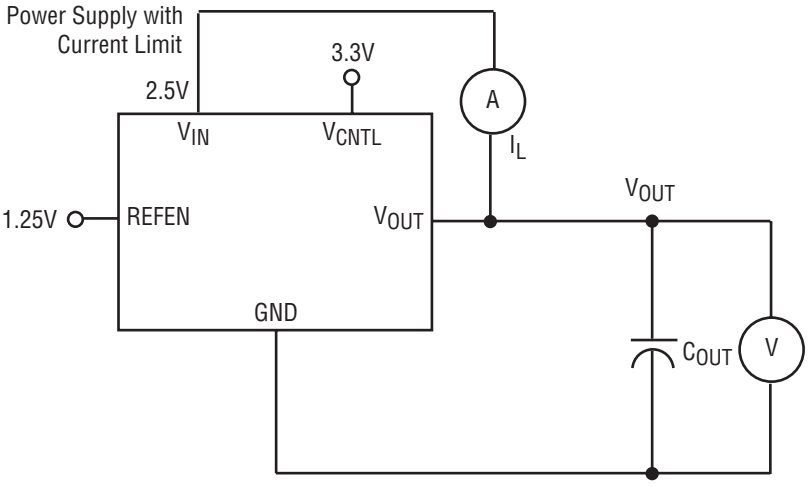


Figure 4. Current Limit for Low Side, I_{LIMIT}

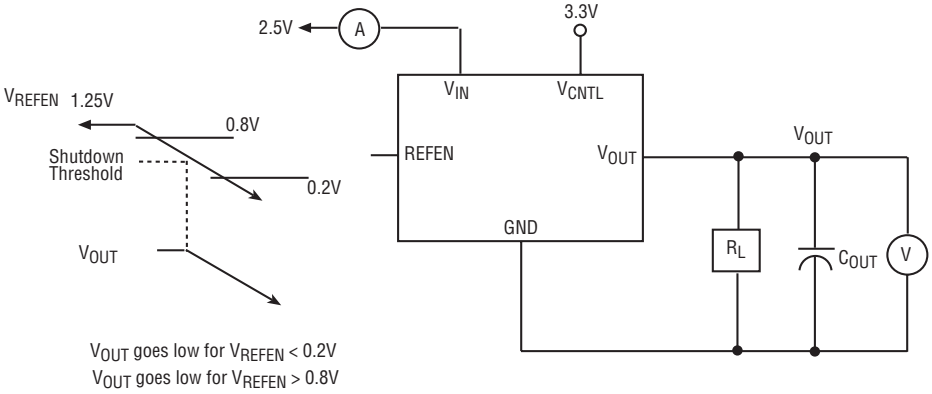
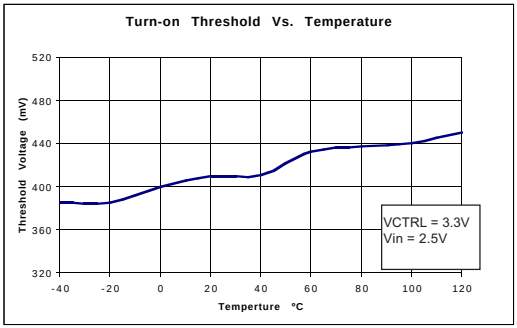
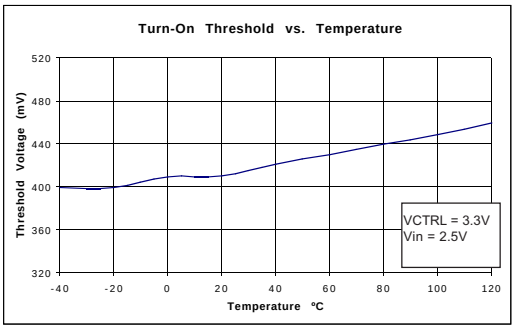
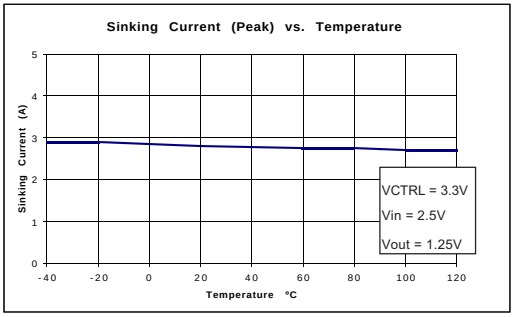


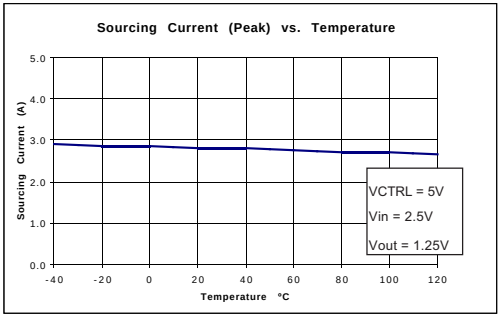
Figure 5. REFEN Pin Shutdown Threshold, , $V_{TRIGGER}$

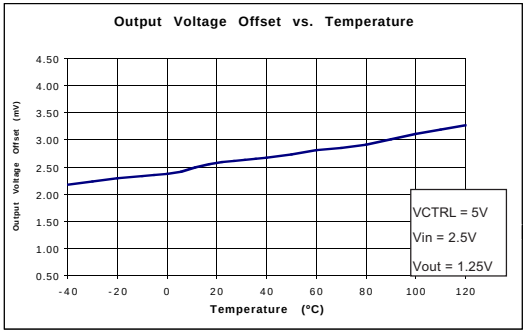
TYPICAL PERFORMANCE CHARACTERISTICS









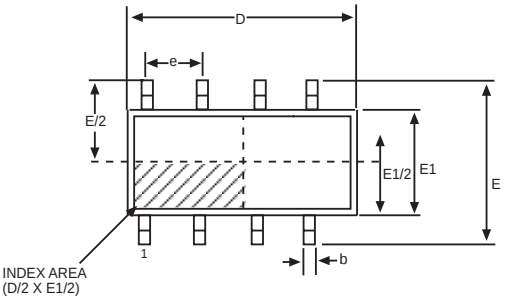


Internal parasitic diode

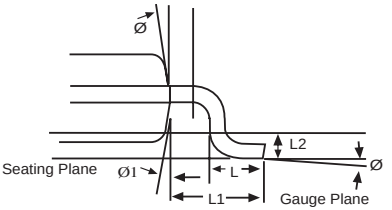
Avoid forward-biasing the internal parasitic diode, V_{OUT} to $V_{CNTL,}$ and V_{OUT} to V_{IN}. Positive voltage should not be applied to the output if V_{IN} and V_{CNTL} are not present.

Considerations for designing, resistance of voltage divider

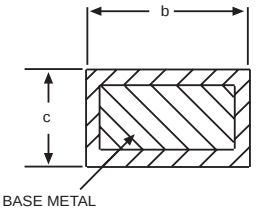
When the reference voltage is programmed below 0.2V the pulldown capability of the internal NMOS transistor is limited. It is recommened to place a filter capacitor from V_{RE} to ground in order to reduce sensitivity to noise and improve power up characteristics (soft start).



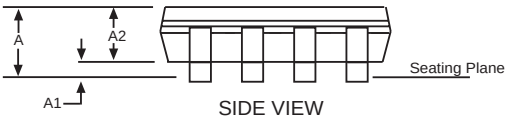
TOP VIEW



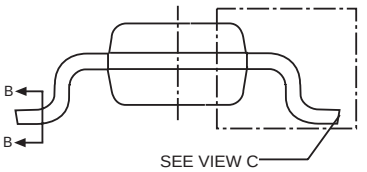
VIEW C



SECTION B-B
WITH PLATING



SIDE VIEW



8 Pin NSOIC JEDEC MS-012 (AA) Variation			
SYMBOL	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
c	0.17	-	0.25
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.04 REF		
L2	0.25 BSC		
ø	0º	-	8º
ø1	5º	-	15º

Note: Dimensions in (mm)
Controlling Dimension

8 Pin NSOIC JEDEC MS-012 (AA) Variation			
SYMBOL	MIN	NOM	MAX
A	0.053	-	0.069
A1	0.004	-	0.010
A2	0.049	-	0.065
b	0.012	-	0.020
c	0.007	-	0.010
D	0.193 BSC		
E	0.236 BSC		
E1	0.154 BSC		
e	0.050 BSC		
L	0.016	-	0.050
L1	0.04 REF		
L2	0.010 BSC		
ø	0º	-	8º
ø1	5º	-	15º

Note: Dimensions in (inches)
Conversion Factor: 1 Inch = 25.40 mm

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SP2996BEN	-40ºC to 85ºC	8 Lead NSOIC
SP2996BEN /TR .	-40ºC to 85ºC	8 Lead NSOIC

Available in lead free packaging. To order add "-L" suffix to part number.
Example: SP2996BEN/TR = standard; SP2996BEN-L-/TR = lead free.

/TR = Tape and Reel
Pack quantity is 2,500 NSOIC.

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