AVERLOGIC

AL440B

4M-Bit High Speed FIFO Field Memory

Applications

- Multimedia systems
- Video capture or editing systems for NTSC/PAL or SVGA resolution
- Security systems
- Scan rate converter
- PIP(Picture In Picture) video display
- TBC(Time Base Correction)
- Frame Synchronizer
- Digital Video Camera
- Hard Disk cache memory
- Buffer for Communication System

* 80MHz High-Speed Version

- DTV/HDTV video stream buffer

Features

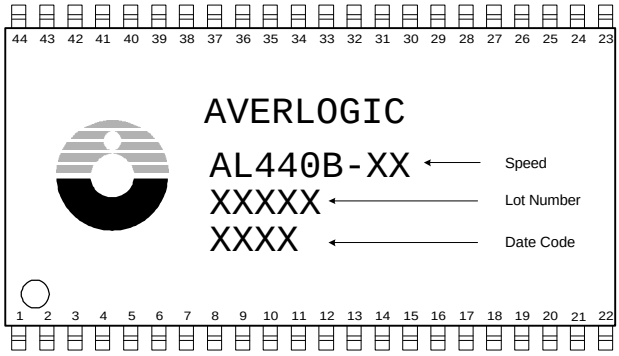
- 4Mbits (512k x 8 bits) organization FIFO
- Independent 8-bit data I/O port operations
- Available in 2 speed grades: 80 and 40Mhz
- Input Enable control (write mask)
- Output Enable control (data skipping)
- Supports Input ready/Output ready flags
- Selectable control signal polarity
- Programmable window mode data access with mirroring function support
- Self-refresh
- 5V signals input tolerance
- 3.3V±10% power supply
- Standard 44-pin TSOP (II) package

Description

The AL440B is a high-performance FIFO (First-In-First-Out) field memory chip designed to buffer audio/video/graphic digital data for a wide range of applications.

Ordering Information

Part number	Package	Power supply
AL440B-24 (40MHz)	44-pin plastic TSOP(II)	+3.3V±10%
AL440B-12 (80MHz)	44-pin plastic TSOP(II)	+3.3V±10%



AL440B-12/24 TSOP (II) pinout diagram

The AL440B FIFO memory provides completely independent 8bit input and output ports that can operate at a maximum speed of 80 MHz. The built-in address and pointer control circuits provide a straightforward bus interface to serially read/write memory that can reduce inter-chip design efforts. Manufactured using a state-of-the-art embedded high density memory cell array, the AL440B uses high performance process technologies with extended controller functions (write mask, read skip, window mode read/write .. etc.), allowing easy operation of non-linearity and regional read/write FIFO for PIP, Digital TV, security system and video camera applications.

The 4Mbits AL440B is configured as 512k x 8-bit FIFO to accommodate NTSC, PAL or up to SVGA resolution. Running at high speed (80Mhz maximum) and low power consumption AC characteristics (3.3V power supply) allow the high performance and high quality application capability for designs such as HDTV.

Additional manipulation is produced by the Input/Output Enable control signals. The application can use input enable to control whether new data is going to be written over the old data or not. For read data, the output enable signal can control whether data is going to be skipped during the read operation.

The Input/Output Ready flags report the FIFO status. The flags can be used to indicate Fullness/Emptiness of the FIFO capacity. Expanding AL440B data bus width is also possible by using multiple AL440B chips in parallel.

To have better control flexibility in the inter-chip design, the polarities of the AL440B control signals are selectable. The read and write ports control signals, such as Read/Write Enable, Input/Output Enable.., can be either active low or high by pulling /PLRTY signal to high or low respectively.

Window data read/write is supported in the AL440B to benefit the designing effort for applications such as PIP display. The window mode is enabled by driving low on /SDAEN signal. A serial bus can program built-in registers to set up coordinates of the window and the settings take effect following by next read/write reset pulse. Window mirroring can cooperate with the window mode data access to flip window data in x or y direction. When window-mirroring function is turned on, write data can be stored in reverse sequence.

Available as a 44-pin TSOP (II), the small footprint allows product designers to keep real estate to a minimum.