

M62021L,P,FP

SYSTEM RESET IC WITH SWITCH FOR MEMORY BACK-UP

DESCRIPTION

The M62021 is a system IC that controls the memory backup function of SRAM and microcomputer (internal RAM).

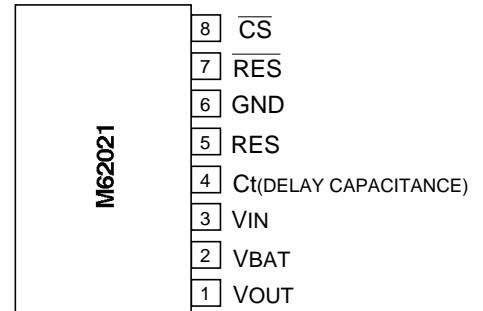
The IC outputs reset signals(RES/RES) to a microcomputer at power-down and power failure.It also shifts the power supply to RAM from main to backup,outputs a signal (CS) that invokes standby mode,and alters RAM to backup circuit mode.

The M62021 contains,in a single chip,power supply monitor and RAM backup functions needed for a microcomputer system,so that the IC makes it possible to construct a system easily and with fewer components compared with a conventional case that uses individual ICs and discrete components.

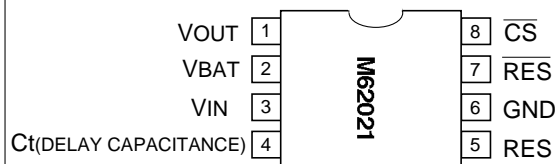
FEATURES

- Built-in switch for selection between main power supply and backup power supply to RAM.
- Small difference between input and output voltage (I_{OUT}=80mA,V_{IN}=5V)0.2V typ
- Detection voltage (power supply monitor voltage)4.40V±0.2V
- Chip select signal output(CS)
- Two channels of reset outputs(RES/RES)
- Power on reset circuit built-in
- Delay time variable by an external capacitance connected to Ct pin
- Facilitates to form backup function with a few number of components

PIN CONFIGURATION (TOP VIEW)



Outline 8P5(L)

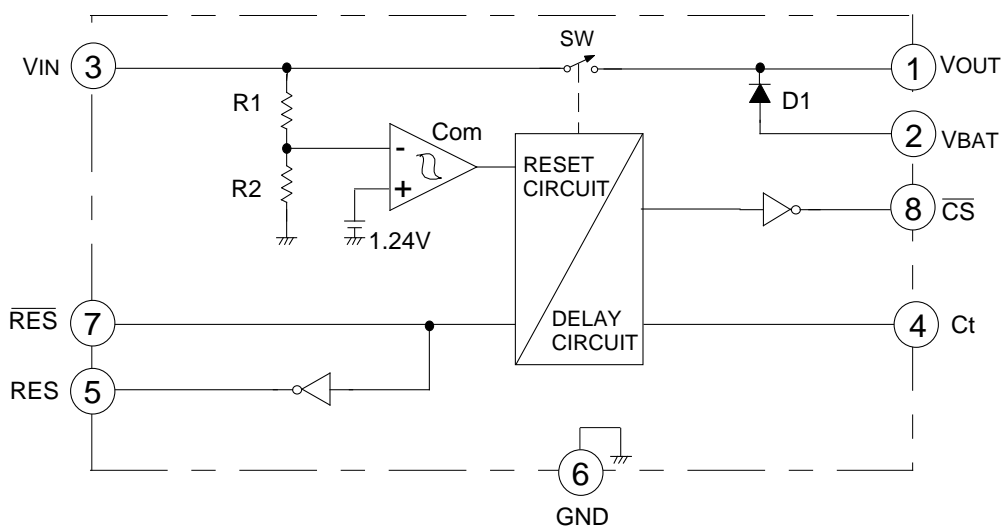


Outline 8P4(P)
8P2S-A(FP)

APPLICATION

Power supply control systems for memory backup of microcomputer system and SRAM boards with built-in backup function that require switching between external power supply and battery.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{IN}	Input voltage		7	V
I _{OUT}	Output current		100	mA
P _d	Power dissipation		800(SIP)/625(DIP)/440(FP)	mW
K _θ	Thermal derating	(Ta 25°C)	8(SIP)/6.25(DIP)/4.4(FP)	mW/°C
T _{opr}	Operating temperature		-20 ~ +75	°C
T _{stg}	Storage temperature		-40 ~ +125	°C

ELECTRICAL CHARACTERISTICS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _s	Detection voltage	V _{IN} (At the change from H →L)	4.2	4.4	4.6	V
V _s	Hysteresis voltage	V _s =V _{SH} -V _{SL}	50	100	200	mV
V _s / T	Temperature coefficient of detection voltage			0.005		%/°C
I _{CC}	Circuit current	I _{OUT} =0mA	V _{IN} =4V	2.0	4.0	mA
			V _{IN} =5V	7.5	12.0	
V _{DROP}	Difference between input and output voltage	V _{IN} =5V	I _{OUT} =50mA	0.125	0.25	V
			I _{OUT} =80mA	0.2	0.4	
V _{OH} (Ct)	Ct output voltage (high level)	V _{IN} =5V(Note1)	4.5	5.0		V
V _{OL} (Ct)	Ct output voltage (low level)	V _{IN} =4V(Note1)		0.02	0.1	V
V _{OH} (RES)	RES output voltage (high level)	V _{IN} =4V(Note1)	3.5	4.0		V
V _{OL} (RES)	RES output voltage (low level)	V _{IN} =5V	(Note1)	0.02		V
			I _{SINK} =1mA	0.05	0.2	
V _{OH} (RES)	RES output voltage (high level)	V _{IN} =5V(Note1)	4.5	5.0		V
V _{OL} (RES)	RES output voltage (low level)	V _{IN} =4V	(Note1)	0.02		V
			I _{SINK} =1mA	0.05	0.2	
V _{OH} (CS)	CS output voltage (high level)	V _{IN} =4V (Note2)	3.50	3.57		V
		V _{IN} =0V, V _{BAT} =3V (Note2)	2.40	2.47		
V _{OL} (CS)	CS output voltage (low level)	V _{IN} =5V	(Note1)	0.08		V
			I _{SINK} =1mA	0.1	0.3	
I _R	Backup Di leak current	V _{BAT} =3V	V _{IN} =5V		±0.5	μA
			V _{IN} =0V		±0.5	
V _F	Backup Di forward direction voltage	I _F =10μA		0.54	0.6	V
t _{pd}	Delay time	V _{IN} =0V → 5V, Ct=4.7μF	10	27	55	ms
t _d	Response time	V _{IN} =5V → 4V		5.0	25.0	μs
V _{OPL} (RES)	RES limit voltage of operation	(Note 3)		0.65		V

Note 1.Regarding conditions to measure V_{OH} and V_{OL},voltage values are to be generated by internal resistance only and no external resistor is used.

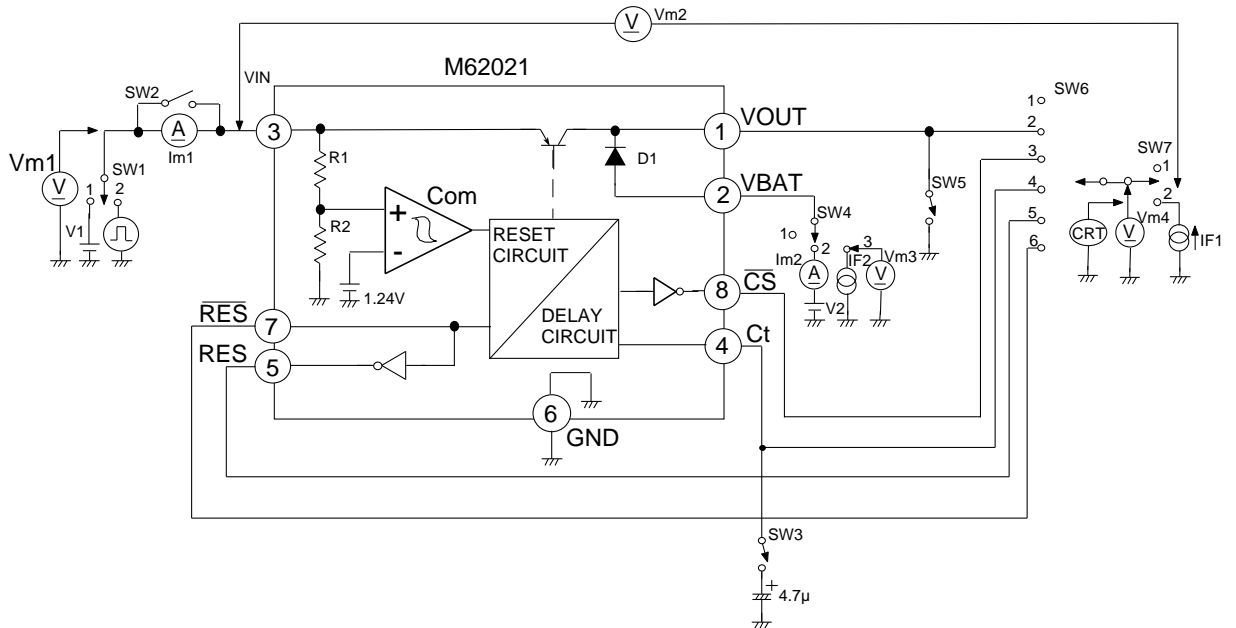
2.These values are produced inserting an external resistor,RCS=1M ,between the CS pin and GND.

3.With no external resistor (10k internal resistance only)

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TEST CIRCUIT



SWITCH MATRIX

Symbol	Parameter	V1	V2	IF1	IF2	S W							Measuring instrument
						1	2	3	4	5	6	7	
Icc	Circuit current	4V	-	-	-	1	ON	OFF	1	OFF	1	1	Im1
		5V				1	ON	OFF	1	OFF	1	1	
Vs (VSL)	Detection voltage (VIN negative-going)	Decrease from 5V	-	-	-	1	ON	OFF	1	OFF	2	1	(Note5) Vm4 CRT Vm1
											3		
											4		
											5		
VDROP	Difference between input and output voltage	5V	-	-50mA -80mA	-	1	ON	OFF	1	OFF	2	2	Vm2
											4		
VOH(Ct)	Ct output voltage(high level)	5V	-	-	-	1	ON	OFF	1	OFF	4	1	Vm4
VOL(Ct)	Ct output voltage(low level)	4V									4		
VOH(RES)	RES output voltage(high level)	4V	-	-	-	1	ON	OFF	1	OFF	5	1	Vm4
VOL(RES)	RES output voltage(low level)	5V									5		
VOH(RES)	RES output voltage(high level)	5V	-	-	-	1	ON	OFF	1	OFF	6	1	Vm4
VOL(RES)	RES output voltage(low level)	4V									6		
VOH(CS)	CS output voltage(high level)(Note 4)	4V 0V	3V	-	-	1	ON	OFF	1	OFF	3	1	Vm4
VOL(CS)	CS output voltage(low level)	5V	-								3		
IR	Backup Di leak current	5V 0V	3V	-	-	1	ON	OFF	2	OFF	1	1	Im2
VF	Backup Di forward direction voltage	0V	-								10µA		
tpd td	Delay time Response time	VOUT	-	-	-	2	ON	ON	1	OFF	2	1	CRT
		CS									3		
		RES									5		
		RES									6		

Notes 4.To measure VOH(CS),insert a 1M resistor between the CS pin and GND.

5. While monitoring each output by Vm4 or CRT,measure the input voltage Vm1 when the output goes from H to L and L to H.Regarding VSH,raise VIN from 4V and measure the input voltage Vm1 when the output goes from H to L and L to H. Vs is VSH-VSL.

6. To measure delay time, change VIN from 0V to 5V and compare,with respect to each pin,the positive-going edge observed on a monitor with that of VIN.To measure response time,change VIN from 5V to 4V and compare,with respect to each pin,the negative-going edge observed on a monitor with that of VIN.

7.Set the switch to OFF when measuring response time.

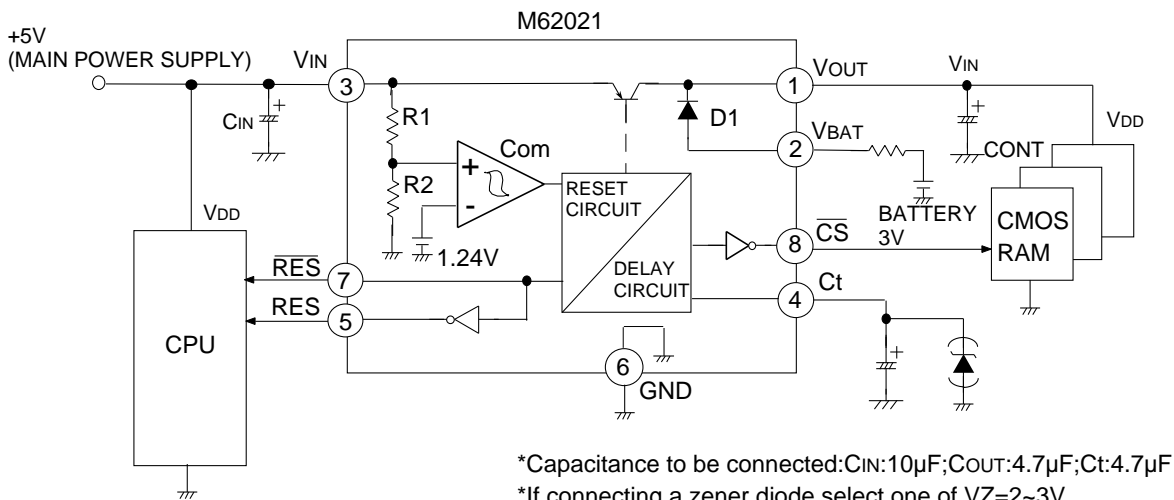
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EXPLANATION OF TERMINALS

Pin No.	Symbol	Name	Function
①	VOUT	Power supply output	VIN and VBAT are controlled by means of an internal switch and output through VOUT The pin is capable of outputting up to 100mA. Use it as VDD of CMOS RAM and the like
②	VBAT	Backup power supply input	Backup power supply is connected to this pin If a lithium battery is used, insert a resistor in series for safety purposes
③	VIN	Power supply input	+5V input pin. Connect to a logic power supply.
④	Ct	Delay capacitor connection pin	A delay capacitor is connected to this pin. By connecting a capacitor, it is possible to delay each output
⑤	RES	Positive reset output	Connect to the positive reset input of a microcomputer. The pin is capable of flowing 1mA sink current
⑥	GND	Ground	Reference for all signals
⑦	$\overline{\text{RES}}$	Negative reset output	Connect to the negative reset input of a microcomputer. The pin is capable of flowing 1mA sink current
⑧	$\overline{\text{CS}}$	Chip select output	Connect to the chip select of RAM. The CS output is at low level in normal state thereby letting RAM be active. Under failure or backup condition, the CS output is set to high level, then RAM enters standby state disabling read/write function. The pin is capable of flowing a 1mA sink current

APPLICATION EXAMPLE



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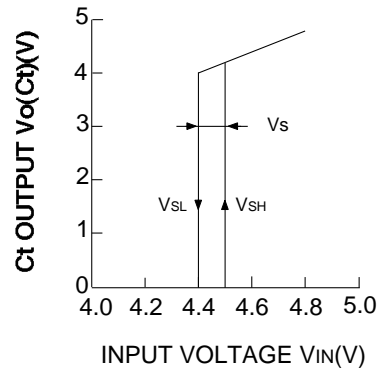
CONFIGURATION

<Power supply detector>

The internal reference voltage V_{ref} is compared by means of a comparator with resistor-divided voltage V_R (resistor-divided voltage produced by R_1 and R_2 from V_{IN}).

If the input voltage is 5V, V_R is set to 1.24V or higher, so the comparator output is at low level and the Ct output (Q1 collector output) is set to high level. If the input voltage drops to below 4.4V in an abnormal condition, V_R becomes below 1.24V, so the comparator output goes from low to high level and the Ct output, from high to low. The input voltage at this point is called V_{SL} . Next, when the input voltage, restored from abnormal state, has a rise, the comparator output goes from high to low level and the Ct output, from low to high.

The comparator used for detection has 100mV hysteresis (V_s), so that malfunctioning is prevented in case that the input voltage slowly drops or V_R nearly equals V_{ref} .



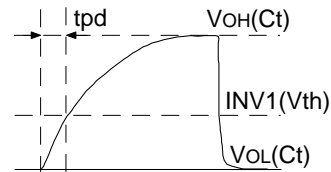
<Delay Circuit>

Connecting an external capacitor to the Ct pin lets RES, \overline{RES} , CS, and VOUT be delayed due to RC transient phenomenon (electric charge).

Delay time is determined as follows.

$$\begin{aligned} \text{Delay time}(t_{pd}) &= Ct \times (R_3 + R_4) \times \ln \frac{[V_{OH}(Ct) - V_{OL}(Ct)]}{[V_{OH}(Ct) - INV1(V_{TH})]} \\ &= Ct \times 22k \times 0.2614 \\ &\approx 5.75 \times 10^3 \times Ct \end{aligned}$$

*Ct is an external capacitance.



DELAYED OUTPUT WAVEFORMS OF Ct

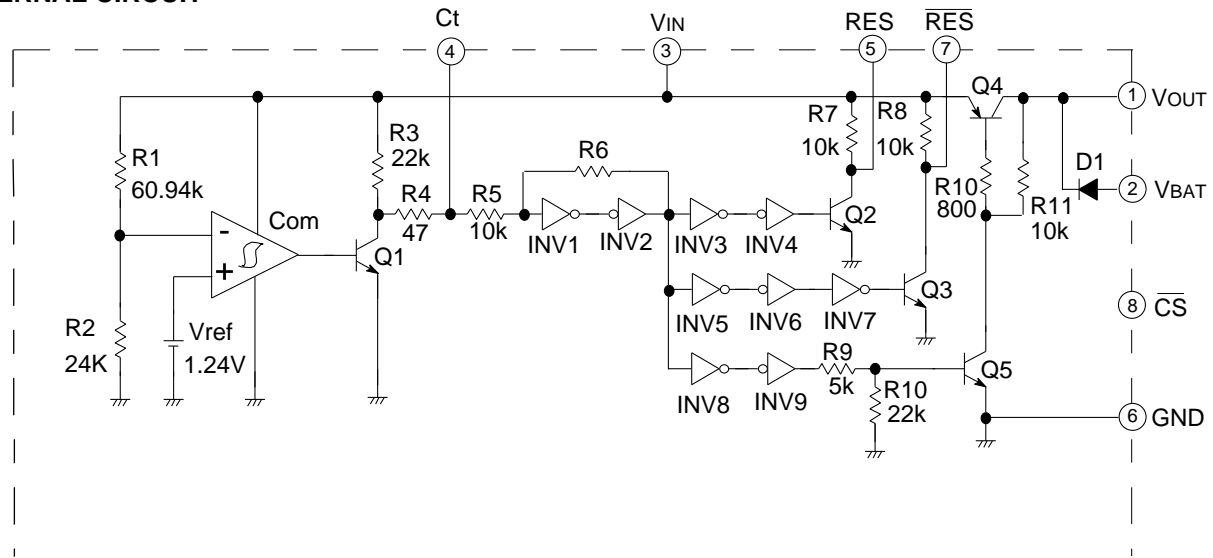
Taking into consideration the time taken by the oscillator of microcomputer to be stable, connect a 4.7 μ F capacitor to the Ct pin.

(As the response time of detection can be slowed due to internal structure depending on the rising rate of power supply, avoid connecting a too large capacitance.)

<Schmitt trigger circuit>

Since waveforms show a gentle rise due to the RC delay circuit, INV1, INV2, R5, and R6 constitute a schmitt trigger circuit to produce hysteresis so as to prevent each output from chattering.

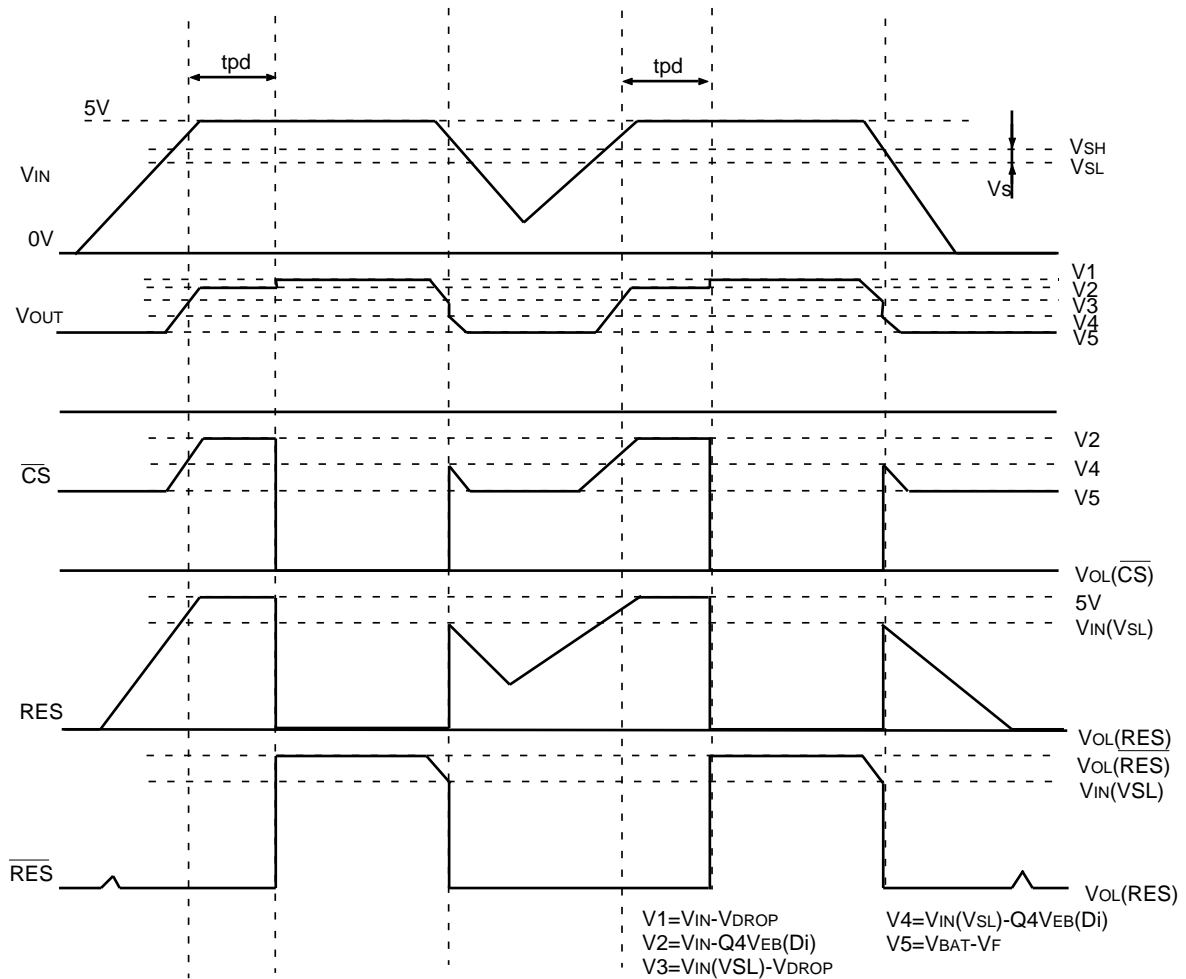
INTERNAL CIRCUIT



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TIMING CHART

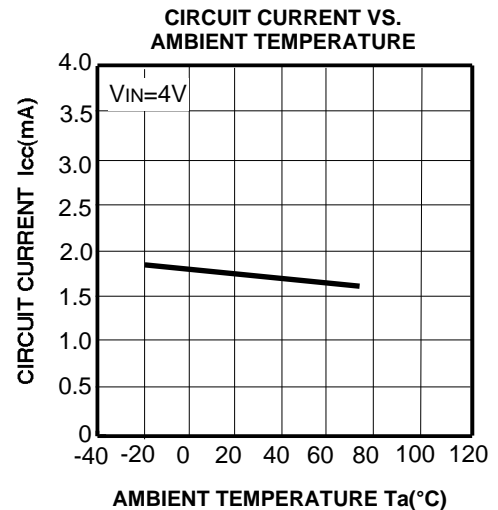
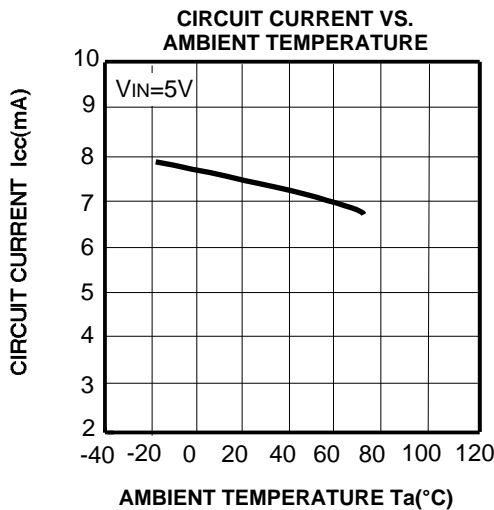
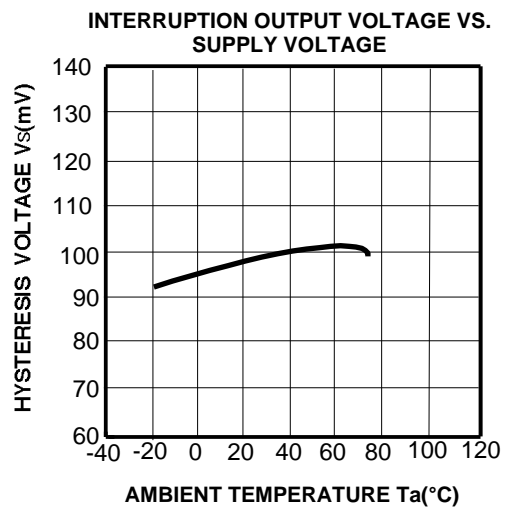
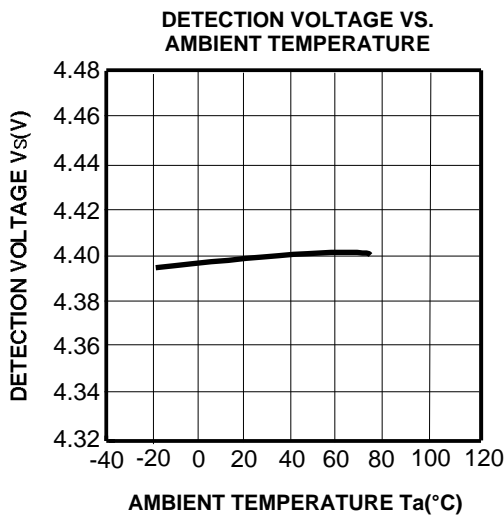
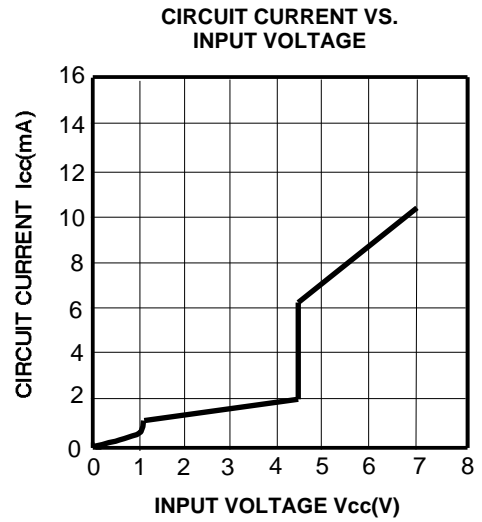
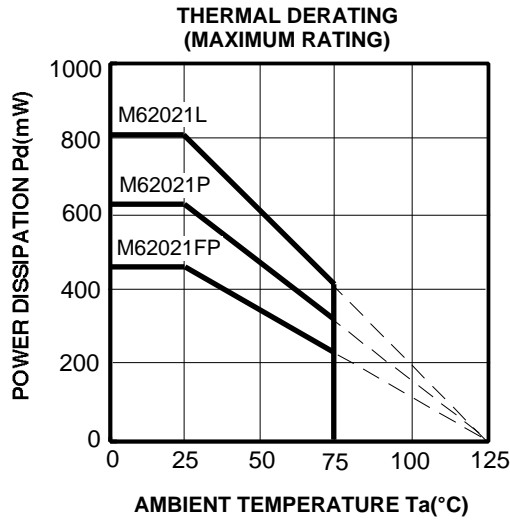


Input voltage / Output pin	In normal operation	In failure (instantaneous drop)	Restoration from failure (instantaneous drop)	In backup state
		Input voltage: 5V	Input voltage: 5V → 4V Each output varies if the input voltage drops to V_{SL} or under	Input voltage: 4V → 5V If the input voltage goes higher than V_{SL} by 100mV, each output varies after delay produced by the delay circuit
V _{OUT}	With Q4 set to ON, a voltage ($V_{IN} - V_{DROP}$) is output	Q4 is turned OFF. A voltage ($V_{IN} - Q_4 V_{EB}(Di)$) is output by the diode between E and B of Q4	Q4 is turned ON after delay and a voltage ($V_{IN} - V_{DROP}$) is output	$V_{BAT} - V_F$
RES	The output level is $V_{OL}(\overline{RES})$ with a logic low	As the state shifts from a logic low to logic high, the output level becomes approximately equal to the input voltage	A logic high is maintained, and then shifts to a logic high	—
\overline{RES}	The output level is $V_{OH}(\overline{RES})$ with a logic low	As the state shifts from a logic high to logic low, the output level becomes $V_{OL}(\overline{RES})$	A logic low is held, and then shifts to a logic high	—
\overline{CS}	The output level is $V_{OL}(\overline{CS})$ with a logic low	As the state shifts from a logic low to logic high, the output level becomes the voltage $V_{IN} - Q_4 V_{EB}(Di)$.	A logic high is maintained, and then shifts to a logic high	The output is a logic high and the output level is $V_{BAT} - V_F$

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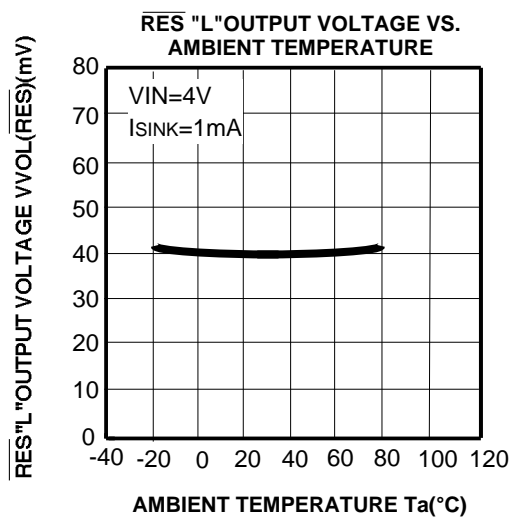
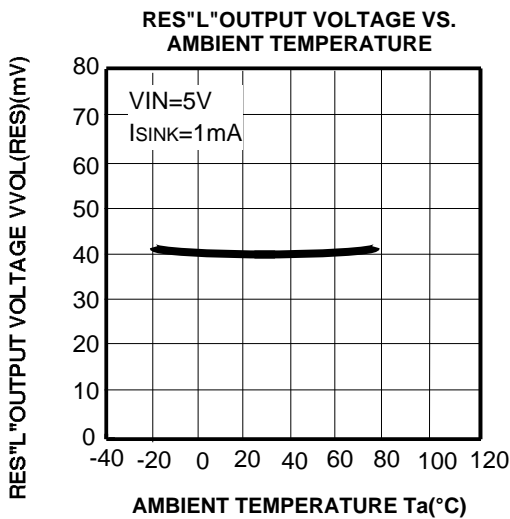
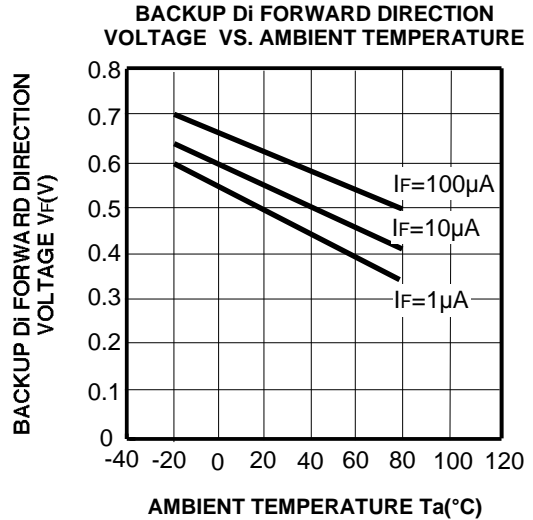
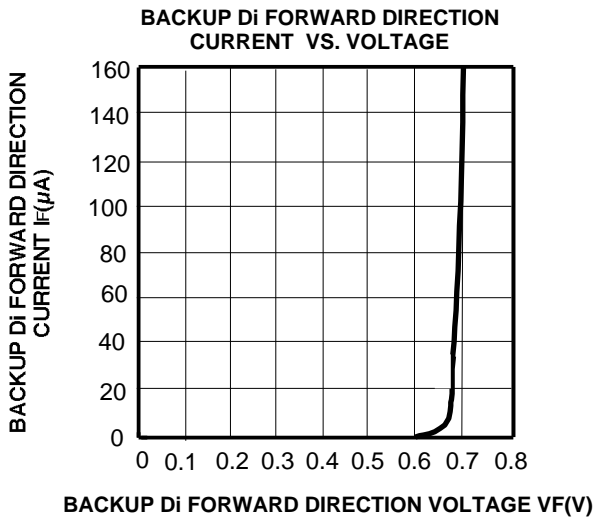
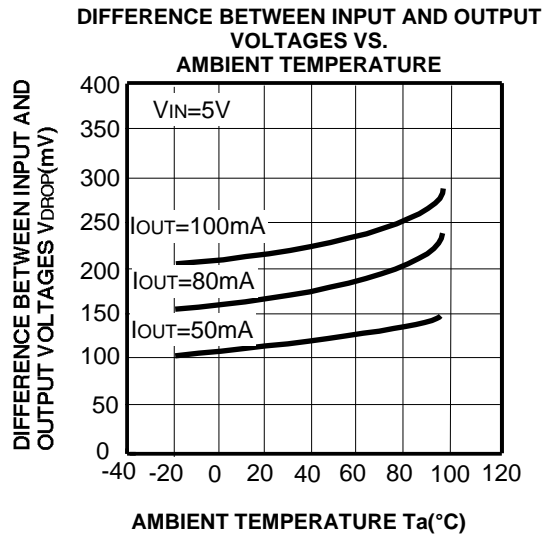
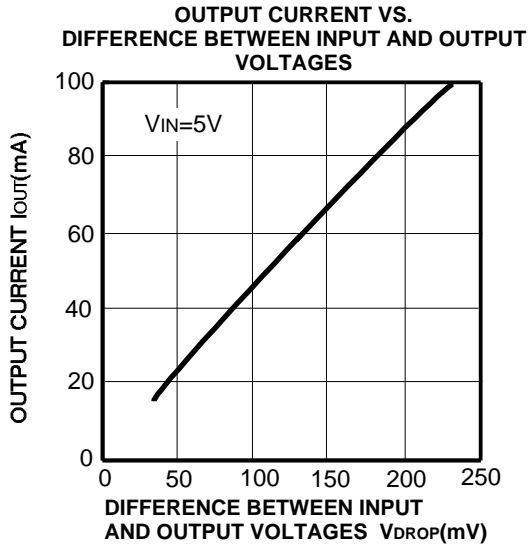
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TYPICAL CHARACTERISTICS



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