

# M56710FP

## F2F Magnetic Stripe Encoding Card Reader

REJ03F0175-0201

Rev.2.01

Mar 31, 2008

### Description

The M56710FP is a semiconductor integrated circuit of Bi-CMOS structure having an F2F demodulator function for magnetic card reader.

### Features

- Low current dissipation (0.7 mA when on standby as a standard)
- Provided with glance-over selection input (4, 8, and 16 bits)
- Provided with output polarity (“L” active or “H” active) switching input
- Miniature mini-mold package
- Wide operating temperature range  $T_a = -20$  to  $75^\circ\text{C}$

### Application

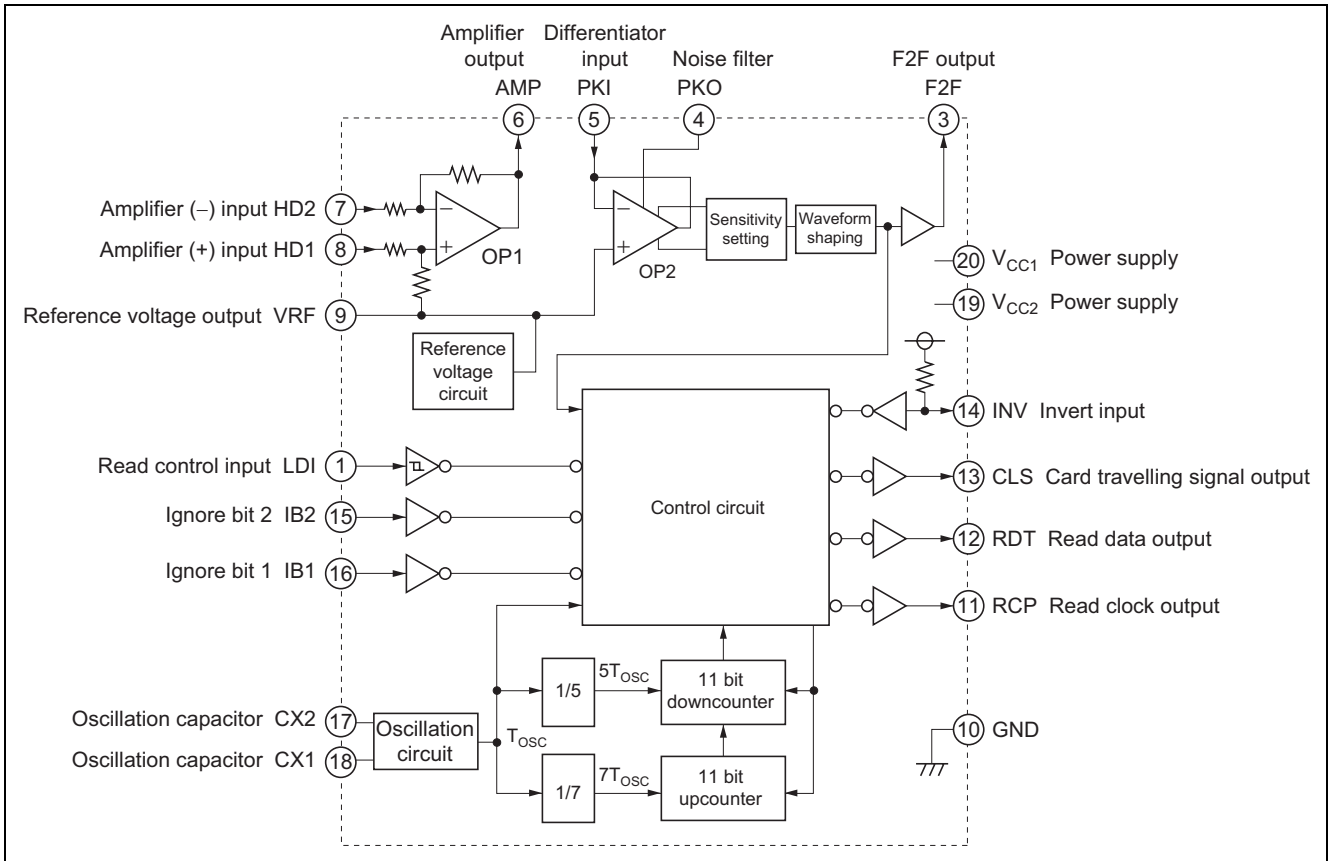
Magnetic card reader

### Functional Description

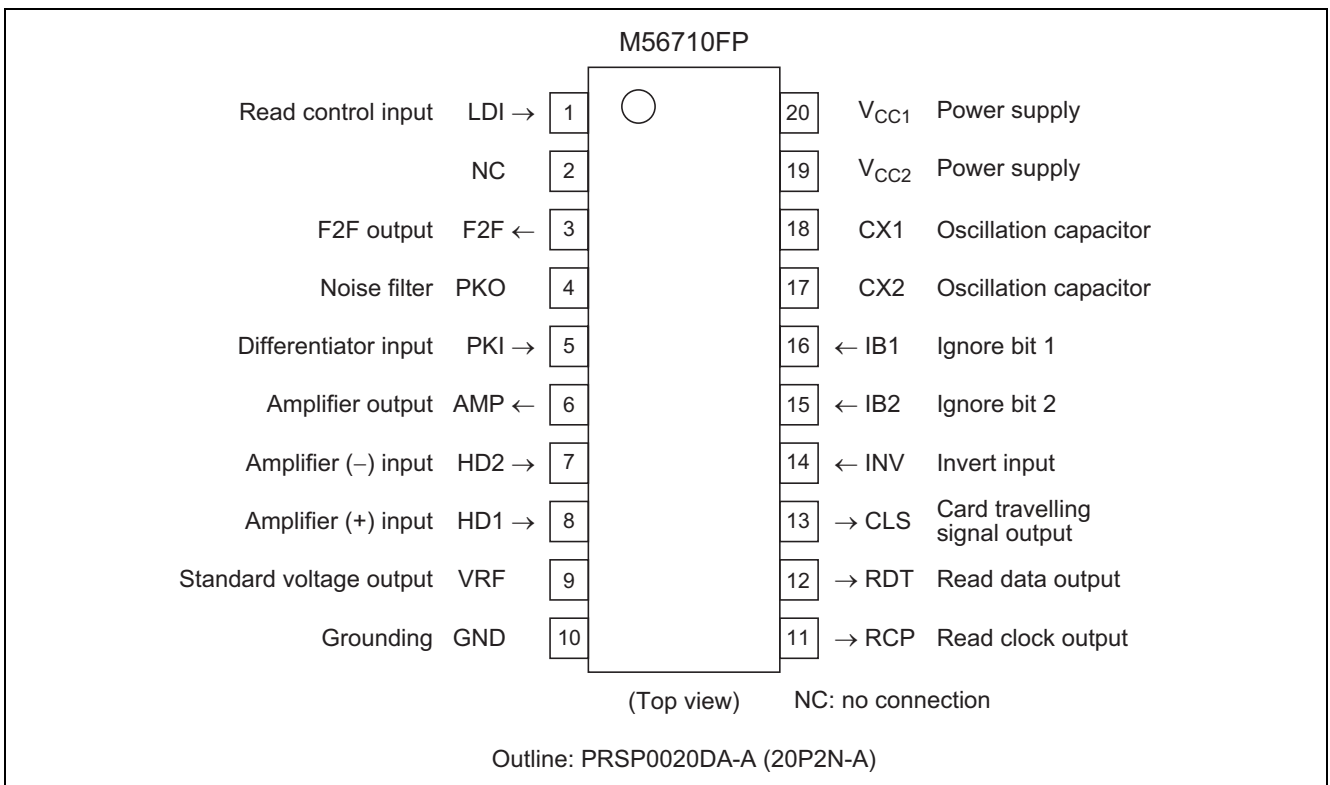
Data signal which is read from magnetic card via magnetic head is input from HD2 and HD1 pins., and converted into F2F pattern signal by analog processing in amplifier OP1, differentiator OP2, sensitivity setting circuit and waveform shaping circuit. If F2F signal is input, the logic section glances over the prescribed number of bits set by IB1 and IB2 input before performing digital processing, and then outputs card reading signal CLS, read clock signal RCP, and read data signal RDT. INV turning to “L” switches each output of CLS. RCP and RDT from “L” active to “H” active.

- Standard Bits:  
Let the number of glance-over bits set by IB1 and IB2 be M.  
Let the Mth FC (flux change) through M+1st FC after LDI input is turned from “L” to “H” be a standard bit with a time width of  $T_{B0}$ .  
I/O is discriminated from the next bit to this standard bit as a data bit.
- I/O discrimination  
Let the data bit time width of a data bit be  $T_{Bn}$ , and if there is one next FC between the FC at the end of that bit (i.e. the beginning of the next bit) to  $5/7T_{Bn}$ , let the next bit ( $B_{n+1}$ ) be data “1”, and, if there is no FC, be data “0”.
- Output signal time width  
When letting the oscillation cycle of oscillation circuit be  $T_{OSC}$ .  
— RCP output pulse width TOW: about  $16 T_{OSC}$   
— RCP delay time to RDT: about  $8 T_{OSC}$

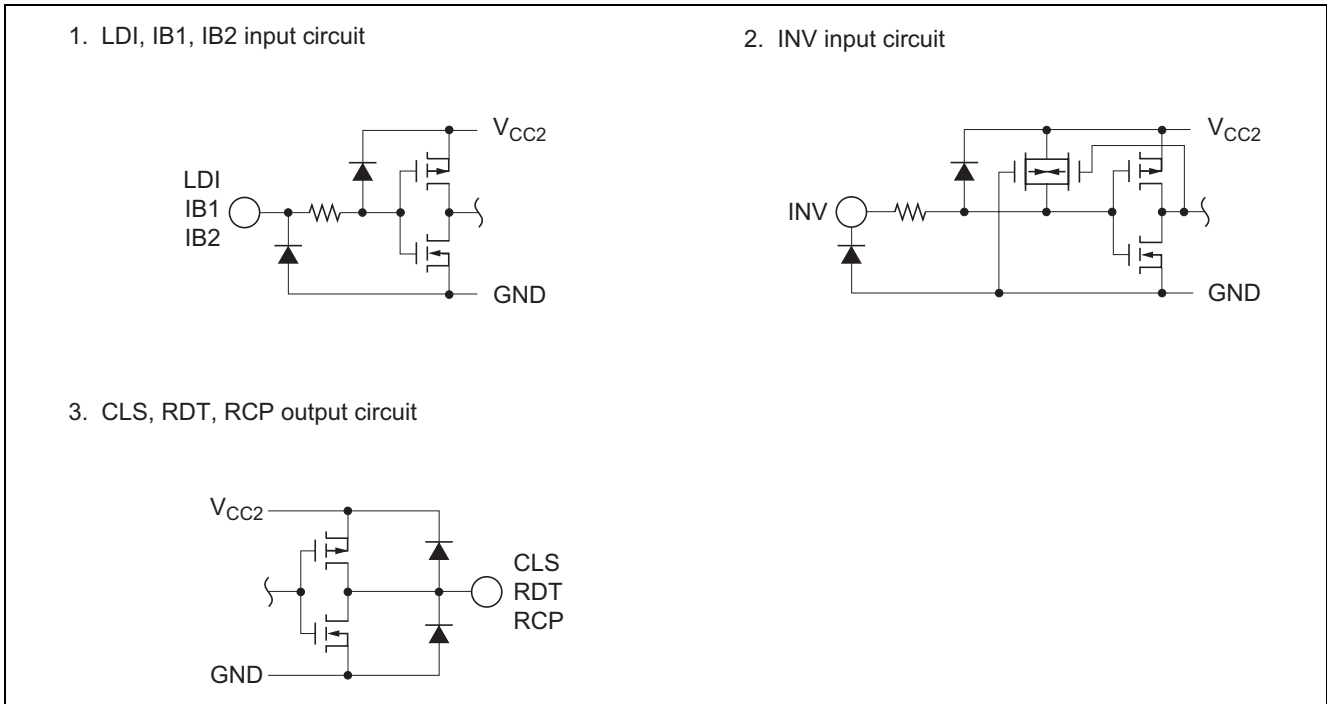
### Block Diagram



### Pin Arrangement



## I/O Circuit



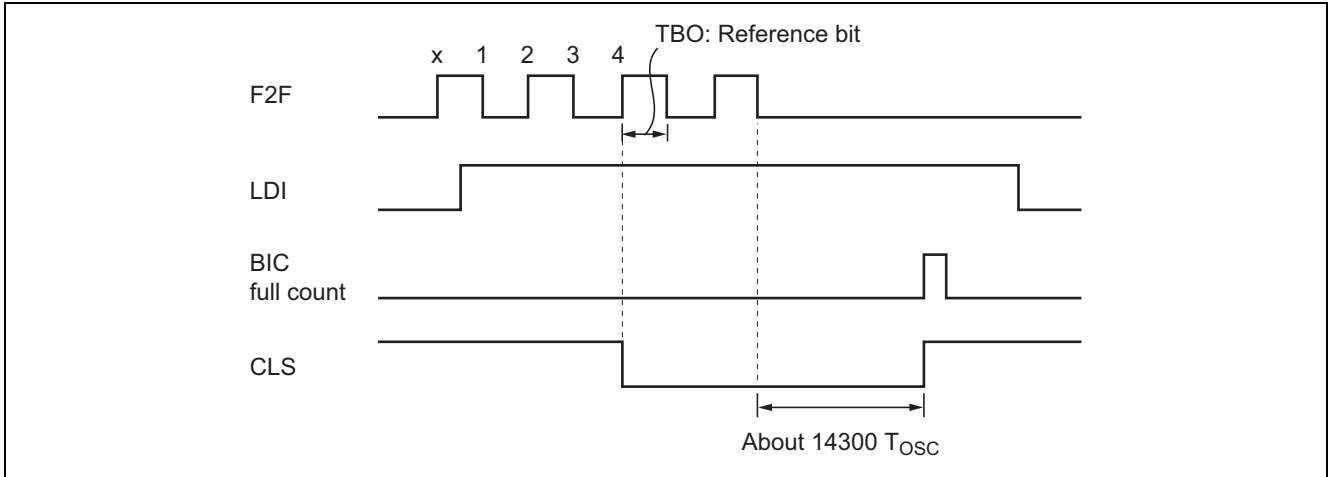
## Pin Function Description

Pin No.	Pin Name	Name	Function
1	LDI	Read control input	Schmitt trigger input. At "L", reset the internal digital circuit. At "H", F2F modulation is possible.
3	F2F	F2F output	F2F signal output that has amplified, differentiated and further waveform-shaped the magnetic head signal.
4	PKO	Noise filter	Connect noise removing capacitor CNF between PKI and PKO.
5	PKI	Differentiator input	Refer to PKO and AMP.
6	AMP	Amplifier output	Connect resistor RPK and capacitor CPK between AMP and PKI.
7	HD2	Amplifier (-) input	Connect magnetic head between HD1 and HD2.
8	HD1	Amplifier (+) input	Connect magnetic head between HD1 and HD2.
9	VRF	Reference voltage output	Reference voltage output of $V_{CC} 1/2$
10	GND	Grounding	
11	RCP	Read clock output	Clock pulse output after F2F modulation
12	RDT	Read data output	Data output after F2F modulation
13	CLS	Card travelling signal output	Signal output indicating that card is travelling
14	INV	Invert input	CLS, RDT and RCP output becomes "L" active at "H" (OPEN), and "H" active at "L".
15	IB2	Ignore bit 2	Glance-over bit setting pin
16	IB1	Ignore bit 1	Glance-over bit setting pin
17	CX2	Oscillation capacitor	Connect capacitor $C_{OSC}$ between CX1 and CX2 to set oscillation frequency.
18	CX1	Oscillation capacitor	Connect capacitor $C_{OSC}$ between CX1 and CX2 to set oscillation frequency.
19	$V_{CC2}$	Power supply	Digital circuit section power supply pin. Supply voltage is $V_{CC}$ .
20	$V_{CC1}$	Power supply	Analog circuit section power supply pin. Supply voltage is $V_{CC}$ (same voltage as $V_{CC2}$ ).

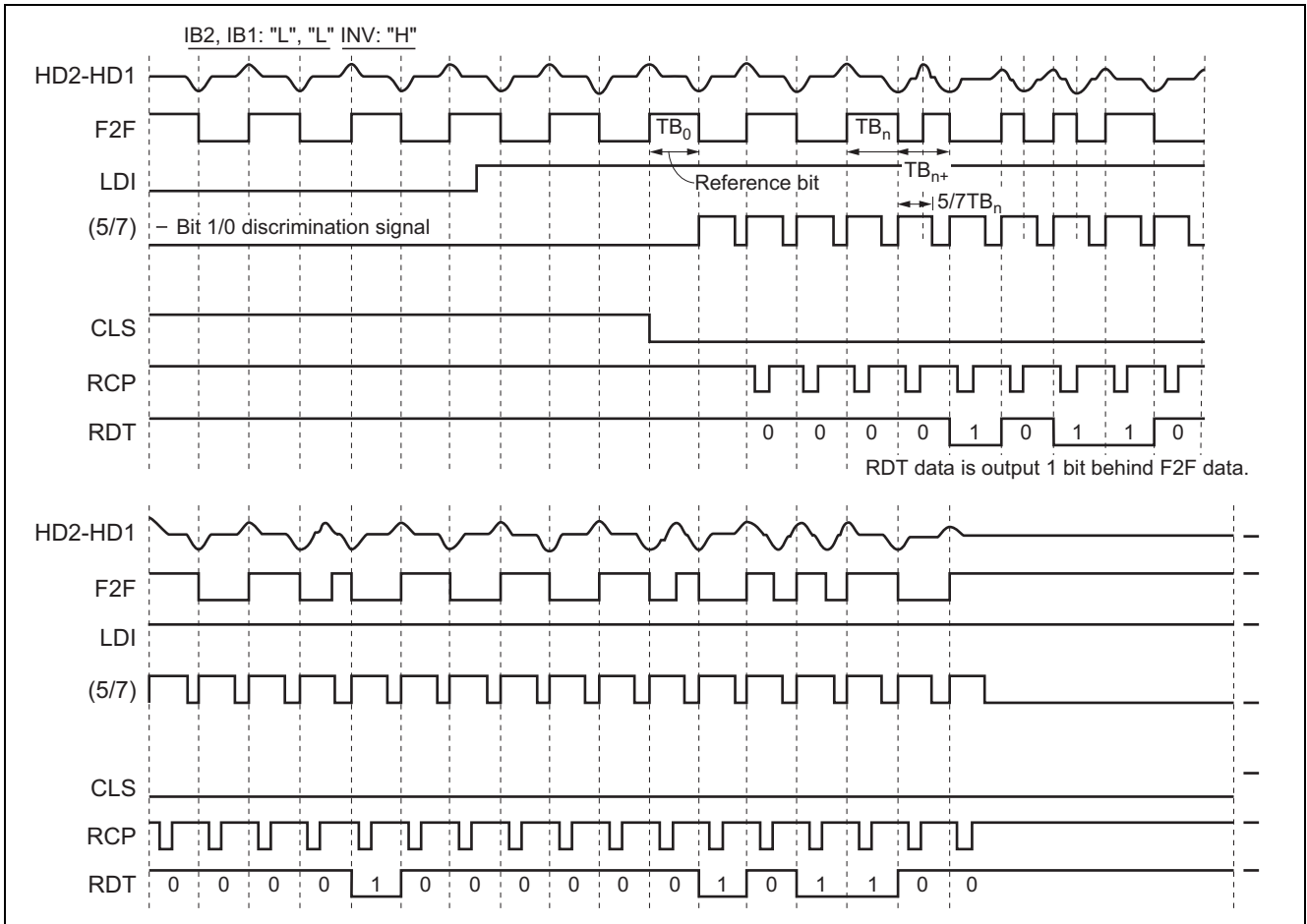
### Glance-Over Bit Setting and Timing By IB1 and IB2

IB2 input	IB1 input	Number of glance-over bits	Description
L	L	4	Internal digital circuit is reset with LDI input at "L". LDI input may be at "H" at all times. CLS output turns to "L" after counting the flux change FC (change in the status of F2F) of the number of glance-over bits, and returns to "H" when BIC (bit interval counter) has fully counted. (At "L" active).
L	H	8	
H	L	16	
H	H	—	

Note: IB2, IB1 : "L", "L"



### Operating Timing Diagram



### Absolute Maximum Ratings

( $T_a = -20$  to  $75^\circ\text{C}$ , unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.3 to +6.5	V	$V_{CC1}, V_{CC2}$
Input voltage	$V_I$	-0.3 to $V_{CC}+0.3$	V	LDI, IB1, IB2, INV
Input voltage	$V_I$	-0.3 to $V_{CC}+0.3$	V	HD1, HD2
Output voltage	$I_o$	-10 to +10	mA	CLS, RDT, RCP
Differential input voltage	$V_{ID}$	-1.2 to +1.2	V	Between HD2 and HD1 pins
Operating temperature	$T_{opr}$	-20 to 75	$^\circ\text{C}$	
Storage temperature	$T_{stg}$	-55 to 125	$^\circ\text{C}$	

Notes: 1. Voltage is based on GND pin of the circuit (0 V), unless otherwise noted.

2. Direction of the current flowing into the circuit is represented by "positive" (without code) and that flowing out of the circuit by "negative" (-code).

## Recommended Operating Conditions

(Ta = -20 to 75°C, unless otherwise noted)

Item	Symbol	Limits			Unit	Test Conditions	
		Min	Typ	Max			
Supply voltage	V <sub>CC1</sub> , V <sub>CC2</sub>	V <sub>CC</sub>	4.0	5	5.5	V	V <sub>CC1</sub> and V <sub>CC2</sub> shall have the identical voltage.
Input voltage	LDI	V <sub>I</sub>	0	—	V <sub>CC</sub>	V	
“H” input voltage	IB1, IB2, INV	V <sub>IH</sub>	0.8V <sub>CC</sub>	—	V <sub>CC</sub>	V	
“L” input voltage	IB1, IB2, INV	V <sub>IL</sub>	0	—	0.2V <sub>CC</sub>	V	
“H” output current	CLS, RDT, RCP	I <sub>OH</sub>	-0.5	—	0	mA	
“L” output current	CLS, RDT, RCP	I <sub>OL</sub>	0	—	5	mA	
Differential input voltage	HD2-HD1	V <sub>IN</sub>	3	—	80	mVp-p	
Input frequency	HD2-HD1	f <sub>IN</sub>	0.3	—	15	kHz	
Oscillation frequency		f <sub>OSC</sub>	0.2	—	2	MHz	f <sub>osc</sub> = 1/T <sub>osc</sub>
External capacitor	CX1, CX2	C <sub>OSC</sub>	25	—	100	pF	f <sub>osc</sub> ∝ 1/C <sub>osc</sub>
External capacitor	CX1, CX2	C <sub>OSC</sub>	—	33	—	pF	Reference value when corresponding to 210BPI
External resistor	AMP	R <sub>PK</sub>	—	470	—	Ω	Reference value when corresponding to 210BPI
External capacitor	PKI	C <sub>PK</sub>	—	0.033	—	μF	Reference value when corresponding to 210BPI
External capacitor	PKI, PKO	C <sub>NF</sub>	—	220	—	pF	Reference value
External resistor	PKI, F2F	R <sub>PF</sub>	—	4.7	—	MΩ	Reference value
External capacitor	V <sub>CC1</sub> , V <sub>CC2</sub>	C <sub>VC</sub>	—	0.1	—	μF	Reference value
External capacitor	VRF	C <sub>VR</sub>	0.8	1	2	μF	Reference value

## Electrical Characteristics

(Ta = -20 to 75°C, V<sub>CC</sub> = 5 V, unless otherwise noted)

Item		Symbol	Test Circuit	Limits			Unit	Test Conditions
				Min	Typ	Max		
Threshold voltage	IB1, IB2, INV	V <sub>TH</sub>	—	0.3V <sub>CC</sub>	—	0.7V <sub>CC</sub>	V	V <sub>CC</sub> = 4 to 5.5 V
“L” output voltage	CLS, RDT, RCP	V <sub>OL</sub>	2	—	—	0.2	V	V <sub>CC</sub> = 4 V I <sub>OL</sub> = 10 μA
			2	—	—	0.4	V	
“H” output voltage	CLS, RDT, RCP	V <sub>OH</sub>	2	3.8	—	—	V	V <sub>CC</sub> = 4 V I <sub>OH</sub> = -10 μA
			2	3.2	—	—	V	
“L” input current	LDI, IB1, IB2	I <sub>IL</sub>	2	-10	—	+10	μA	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V
“L” input current	INV	I <sub>IL</sub>	2	-80	—	-10	mA	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V
“H” input current	LDI, IB1, IB2, INV	I <sub>IH</sub>	2	-10	—	+10	μA	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 5.5 V
Positive threshold current	INV	I <sub>IT+</sub>	2	-250	—	-50	μA	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>TH</sub>
Reference voltage	VRF	VREF	1	2.3	2.5	2.7	V	V <sub>IN</sub> = 0 mVp-p
Voltage gain 1	OP1	GV11	3	18	20	24	Double	f <sub>IN</sub> = 1 kHz V <sub>IN</sub> = 80 mVp-p sine wave
Voltage gain 2	OP1	GV21	3	18	20	24	Double	f <sub>IN</sub> = 15 kHz V <sub>IN</sub> = 80 mVp-p sine wave
Input resistance	OP1	RIN1	3	7	10	14	kΩ	f <sub>IN</sub> = 1 kHz V <sub>IN</sub> = 80 mVp-p sine wave
Maximum output voltage	OP1	VOPP1	3	2	—	—	Vp-p	f <sub>IN</sub> = 1 kHz sine wave THD AMP = 5%
“L” sensitivity current	PKI – F2F	I <sub>IL2</sub>	4	—	—	-0.3	μA	V <sub>M</sub> , F2F < 0.5 V
“H” sensitivity current	PKI – F2F	I <sub>IH2</sub>	4	0.3	—	—	μA	V <sub>M</sub> , F2F > 4.5 V
Positive threshold voltage	PKI – F2F	V <sub>TH+2</sub>	5	0.2	0.45	0.7	V	On the VRF basis
Negative threshold voltage	PKI – F2F	V <sub>TH-2</sub>	5	-0.7	-0.45	-0.2	V	On the VRF basis
Threshold differential voltage	PKI – F2F	V <sub>THD2</sub>	—	-0.15	—	0.15	V	(V <sub>TH+2</sub> ) –  V <sub>TH-2</sub>
Pin voltage range	PKO	V <sub>PKO</sub>	4	-1.2	—	1.2	V	On the VRF basis  PK  = 1 mA – +1 mA
“L” output voltage	F2F	V <sub>OL3</sub>	5	—	—	0.5	V	V <sub>PKI</sub> = 0 V, I <sub>F2F</sub> = 0.5 mA
“H” output voltage	F2F	V <sub>OH3</sub>	5	4.5	—	—	V	V <sub>PKI</sub> = 5 V, I <sub>F2F</sub> = -0.5 mA
Positive threshold voltage	LDI	V <sub>TH+4</sub>	6	2.5	—	3.5	V	

(Ta = -20 to 75°C, VCC = 5 V, unless otherwise noted)

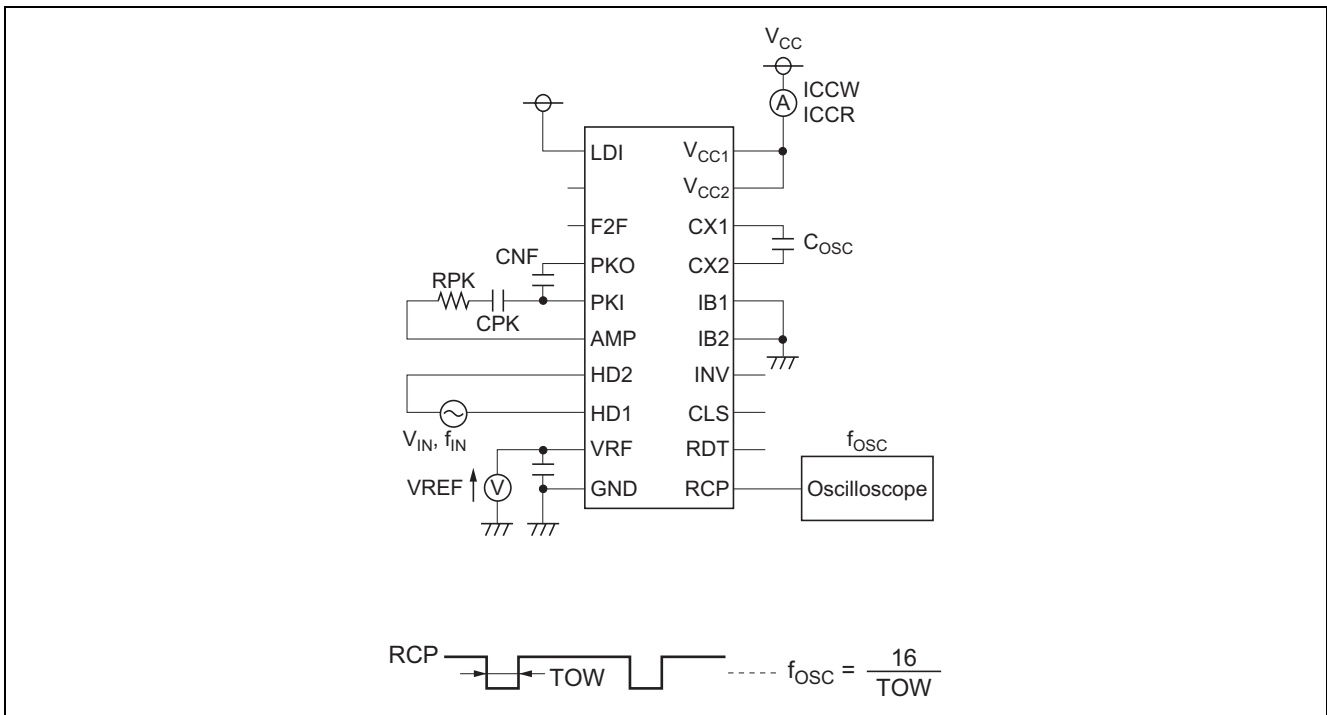
Item	Symbol	Test Circuit	Limits			Unit	Test Conditions	
			Min	Typ	Max			
Negative threshold voltage	LDI	VTH-4	6	1.5	—	2.7	V	
Hysteresis width	LDI	VHY4	—	0.5	—	1.5	V	(VTH+4) - (VTH-4)
Standby circuit current	VCC1, VCC2	ICCW	1	—	0.7	1.0	mA	VIN = 0 mVp-p
Operating circuit current	VCC1, VCC2	ICCR	1	—	1.9	2.4	mA	fIN = 8.2 kHz VIN = 68 mVp-p sine wave fOSC = 1 MHz
Oscillation frequency	RCP	fOSC	1	0.75	—	1.5	MHz	COSC = 33 pF
Output pulse width	RCP	TOW	7	15	16	17	μs	fOSC = 1 MHz
Intra-output delay time	RDT, RCP	TOD	7	7	8	9	μs	fOSC = 1 MHz
Input noise width	INV	TNW	7	0.5	—	—	μs	

Note: 1. Min. and max. limits do not represent absolute values.  
 2. Typ. limits represent standard values when Ta = 25°C and VCC = 5V.

**Test Circuit**

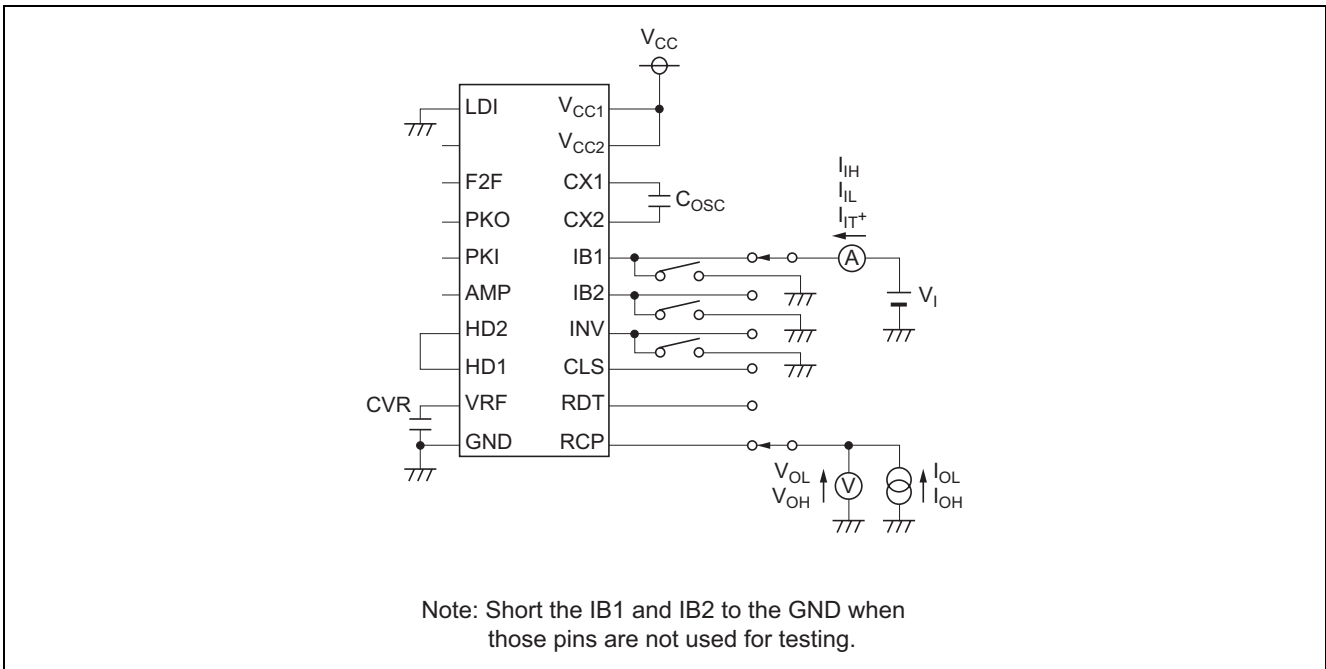
On the following drawing, COSC = 33 pF, RPK = 470 Ω, CPK = 0.033 μF, CNF = 470 pF, CVR = 1 μF

1. Testing of VREF, ICCW, ICCR, fosc

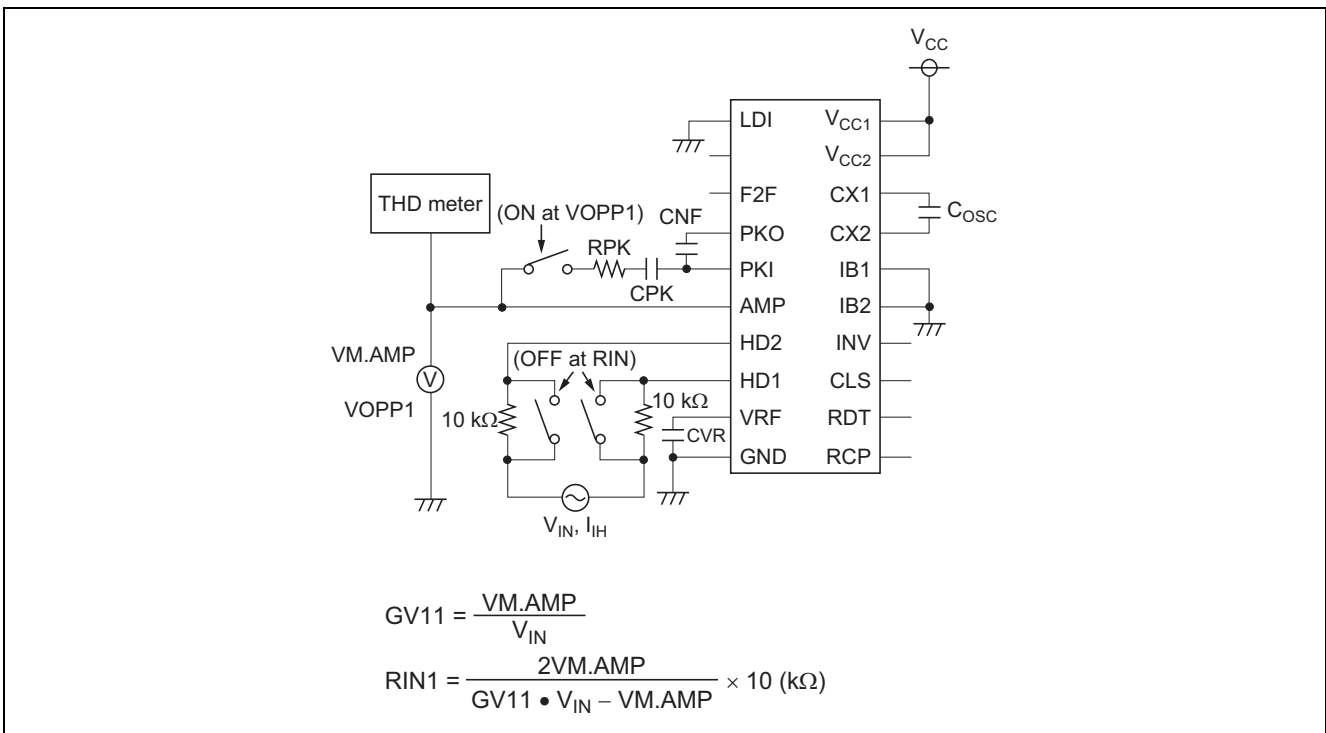




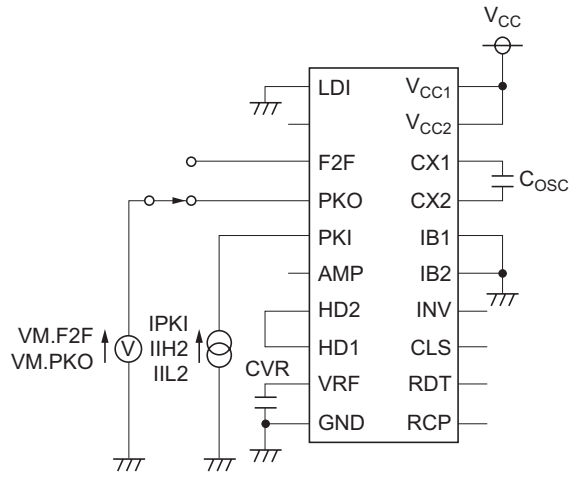
2. Testing of  $V_{OL}$ ,  $V_{OH}$ ,  $I_{IL}$ ,  $I_{IH}$ ,  $I_{IT+}$



3. Testing of  $GV_{11}$ ,  $GV_{21}$ ,  $RIN_1$ ,  $VO_{PP1}$

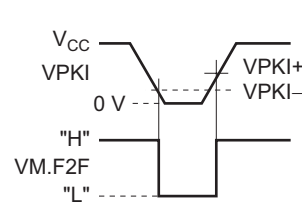
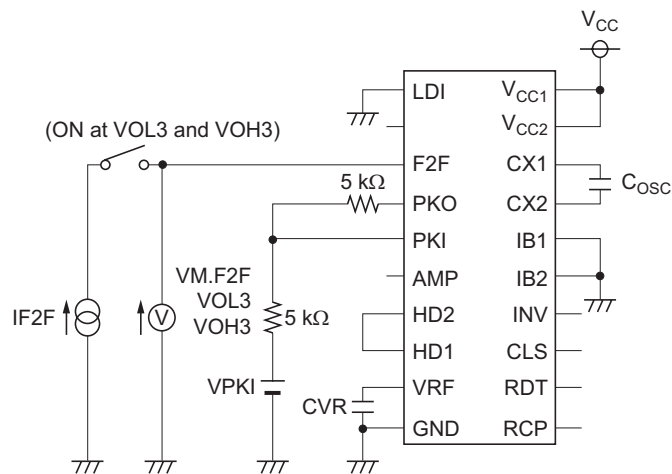


4. Testing of I<sub>IH2</sub>, I<sub>IL2</sub>, V<sub>PKO</sub>



Note: I<sub>IL2</sub> is PKI input current providing V<sub>M.F2F</sub> < 0.5 V.  
 I<sub>IH2</sub> is PKI input current providing V<sub>M.F2F</sub> > 4.5 V.  
 V<sub>PKO</sub> = V<sub>M.PKO</sub> - V<sub>REF</sub>

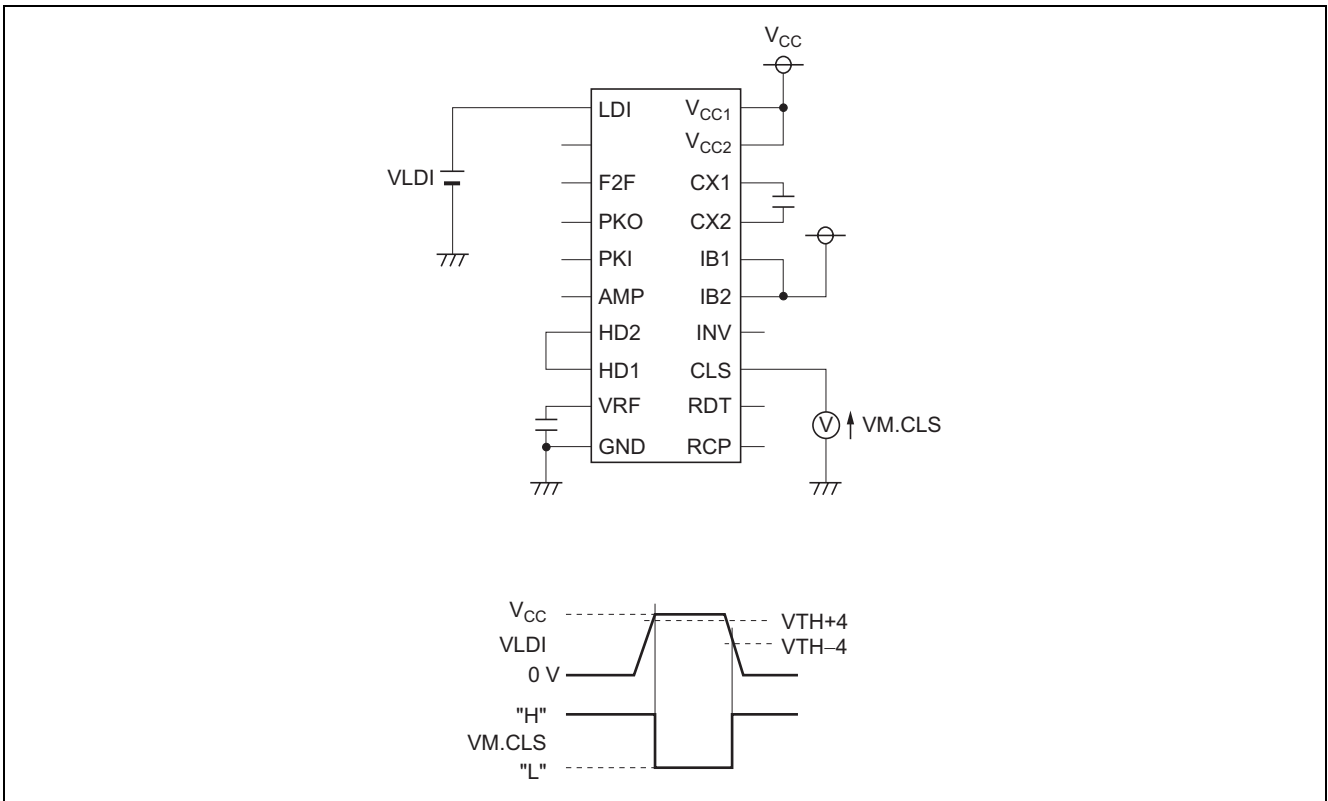
5. Testing of V<sub>TH+2</sub>, V<sub>TH-2</sub>, V<sub>OL3</sub>, V<sub>OH3</sub>



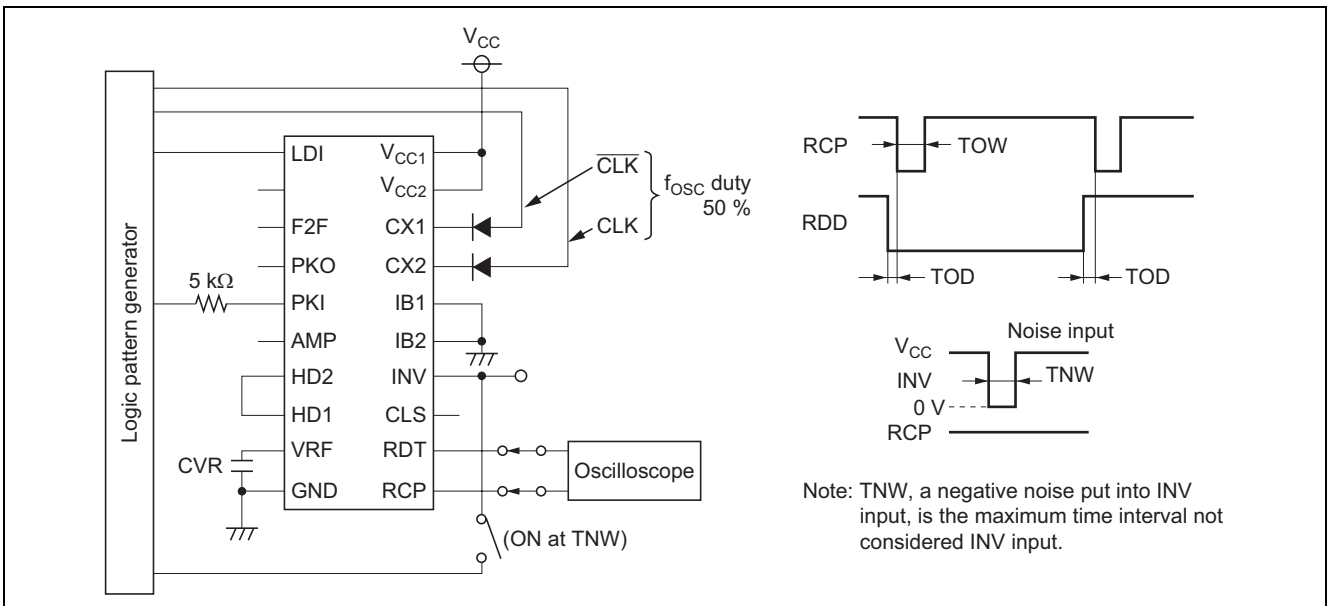
$$V_{TH+2} = V_{REF} - V_{PKI-}$$

$$V_{TH-2} = V_{REF} - V_{PKI+}$$

6. Testing of VTH+4, VTH-4

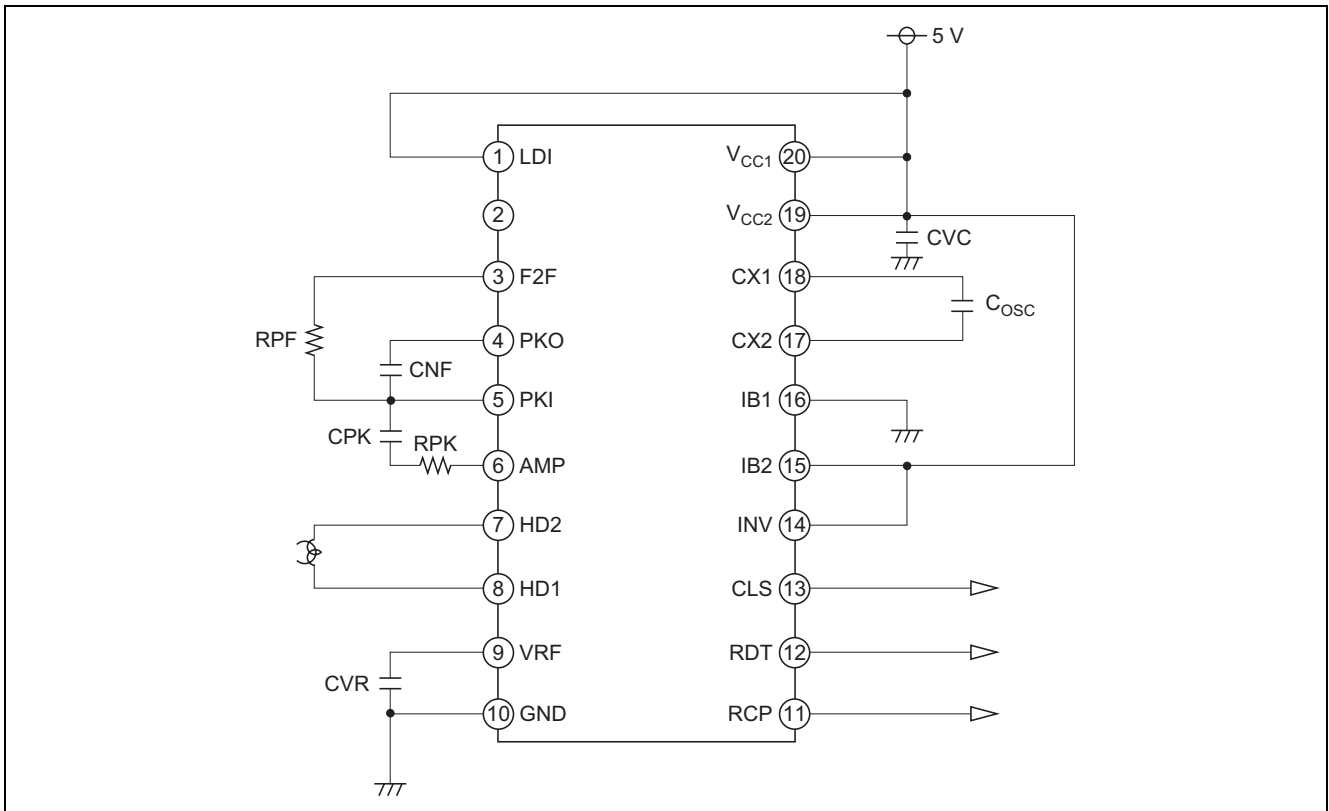


7. Testing of TOW, TOD, TNW



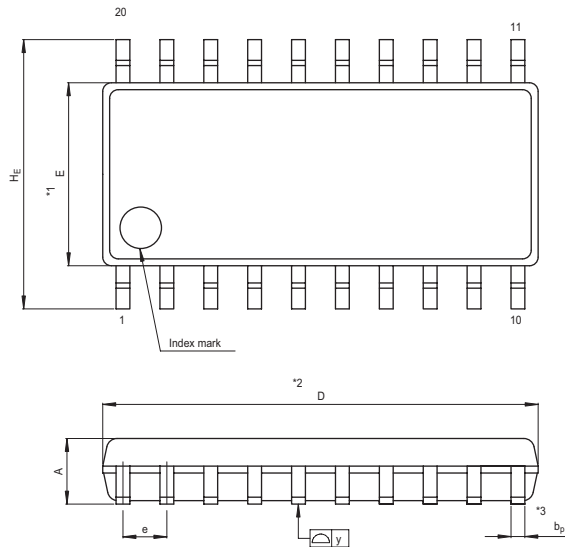
## Application Example

When setting the glance-over bit to 16 bits to let it be “L” active output

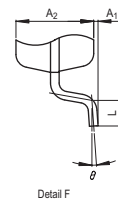


### Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.3x12.6-1.27	PRSP0020DA-A	20P2N-A	0.3g



NOTE)  
 1. DIMENSIONS \*\*1\* AND \*\*2\* DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3\* DOES NOT INCLUDE TRIM OFFSET.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.5	12.6	12.7
E	5.2	5.3	5.4
A <sub>2</sub>	—	1.8	—
A <sub>1</sub>	0	0.1	0.2
A	—	—	2.1
b <sub>p</sub>	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H <sub>E</sub>	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

Notes:

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