M56710FP

F2F Magnetic Stripe Encoding Card Reader

REJ03F0175-0201
Rev.2.01
Mar 31, 2008

Description

The M56710FP is a semiconductor integrated circuit of Bi-CMOS structure having an F2F demodulator function for magnetic card reader.

Features

- Low current dissipation (0.7 mA when on standby as a standard)
- Provided with glance-over selection input (4, 8, and 16 bits)
- Provided with output polarity ("L" active or "H" active) switching input
- Miniature mini-mold package
- Wide operating temperature range Ta = –20 to 75°C

Application

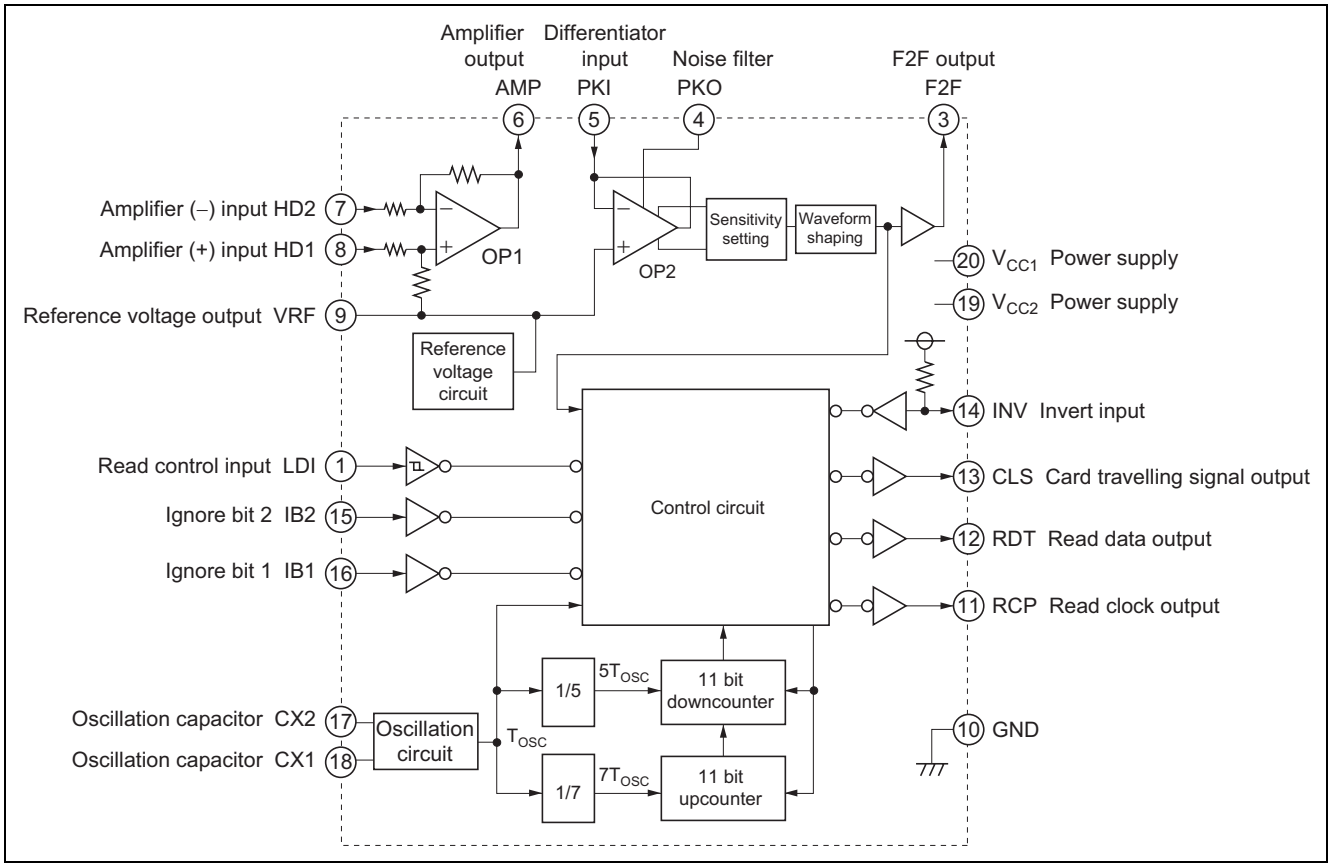
Magnetic card reader

Functional Description

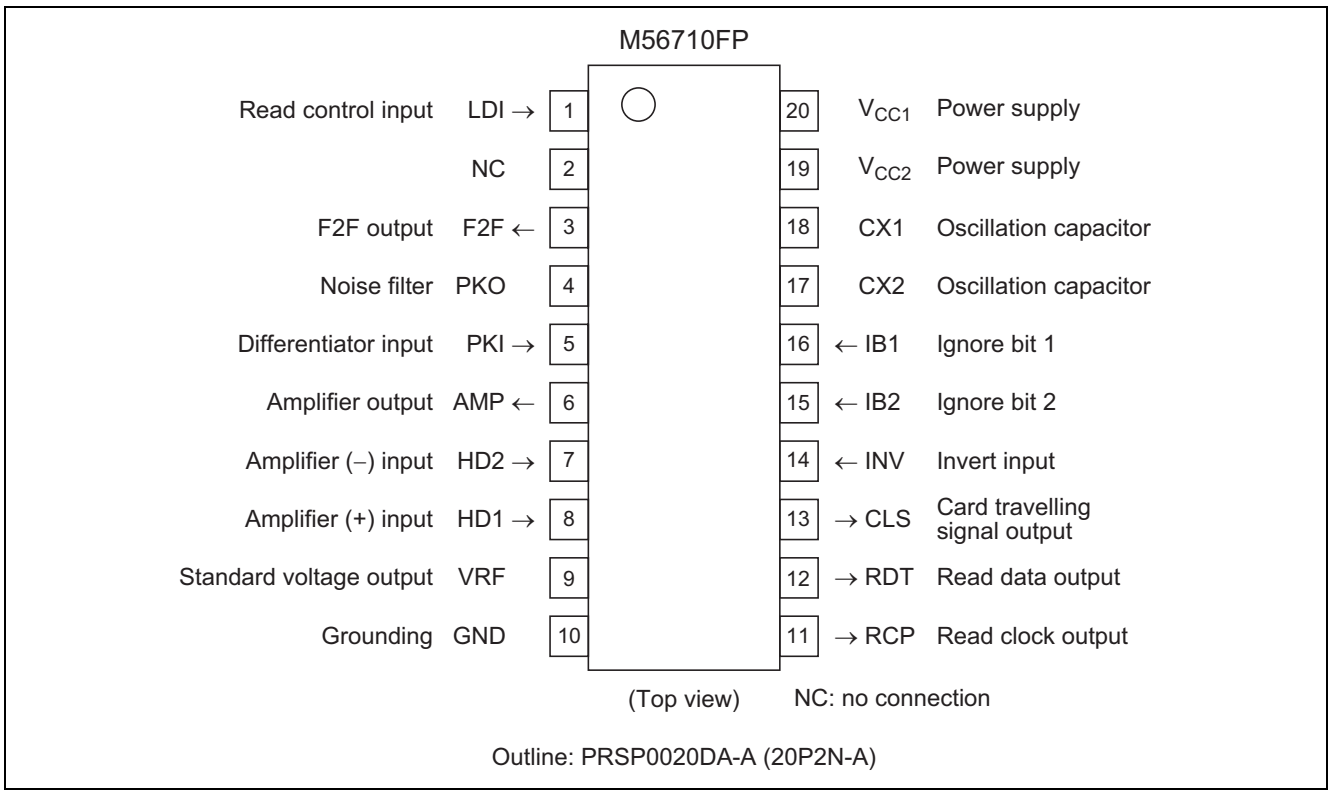
Data signal which is read from magnetic card via magnetic head is input from HD2 and HD1 pins., and converted into F2F pattern signal by analog processing in amplifier OP1, differentiator OP2, sensitivity setting circuit and waveform shaping circuit. If F2F signal is input, the logic section glances over the prescribed number of bits set by IB1 and IB2 input before performing digital processing, and then outputs card reading signal CLS, read clock signal RCP, and read data signal RDT. INV turning to "L" switches each output of CLS. RCP and RDT from "L" active to "H" active.

- Standard Bits:
  Let the number of glance-over bits set by IB1 and IB2 be M.
  Let the Mth FC (flux change) through M+1st FC after LDI input is turned from "L" to "H" be a standard bit with a time width of TB0.
  I/O is discriminated from the next bit to this standard bit as a data bit.
- I/O discrimination
  Let the data bit time width of a data bit be TBn, and if there is one next FC between the FC at the end of that bit (i.e. the beginning of the next bit) to 5/7TBn, let the next bit (Bn+1) be data "1", and, if there is no FC, be data "0".
- Output signal time width
  When letting the oscillation cycle of oscillation circuit be T_{OSC}.
  — RCP output pulse width TOW: about 16 T_{OSC}
  — RCP delay time to RDT: about 8 T_{OSC}

Block Diagram



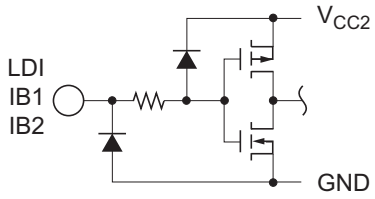
Pin Arrangement



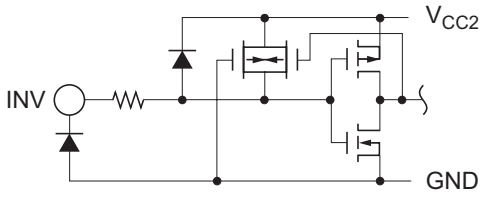
Outline: PRSP0020DA-A (20P2N-A)

I/O Circuit

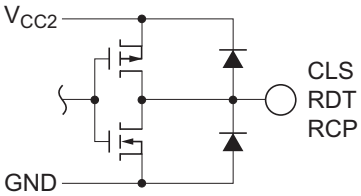
1. LDI, IB1, IB2 input circuit



2. INV input circuit



3. CLS, RDT, RCP output circuit



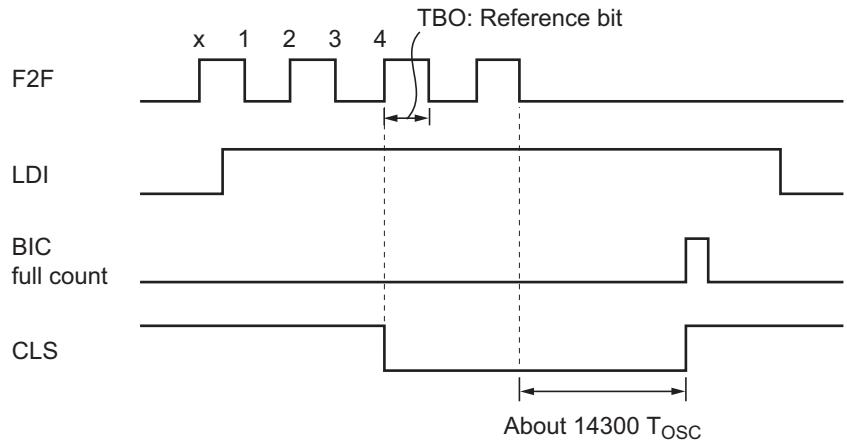
Pin Function Description

Pin No.	Pin Name	Name	Function
1	LDI	Read control input	Schmidt trigger input. At “L”, reset the internal digital circuit. At “H”, F2F modulation is possible.
3	F2F	F2F output	F2F signal output that has amplified, differentiated and further waveform-shaped the magnetic head signal.
4	PKO	Noise filter	Connect noise removing capacitor CNF between PKI and PKO.
5	PKI	Differentiator input	Refer to PKO and AMP.
6	AMP	Amplifier output	Connect resistor RPK and capacitor CPK between AMP and PKI.
7	HD2	Amplifier (–) input	Connect magnetic head between HD1 and HD2.
8	HD1	Amplifier (+) input	Connect magnetic head between HD1 and HD2.
9	VRF	Reference voltage output	Reference voltage output of V_{CC} 1/2
10	GND	Grounding	
11	RCP	Read clock output	Clock pulse output after F2F modulation
12	RDT	Read data output	Data output after F2F modulation
13	CLS	Card travelling signal output	Signal output indicating that card is travelling
14	INV	Invert input	CLS, RDT and RCP output becomes “L” active at “H” (OPEN), and “H” active at “L”.
15	IB2	Ignore bit 2	Glance-over bit setting pin
16	IB1	Ignore bit 1	Glance-over bit setting pin
17	CX2	Oscillation capacitor	Connect capacitor C_{OSC} between CX1 and CX2 to set oscillation frequency.
18	CX1	Oscillation capacitor	Connect capacitor C_{OSC} between CX1 and CX2 to set oscillation frequency.
19	V_{CC2}	Power supply	Digital circuit section power supply pin. Supply voltage is V_{CC}.
20	V_{CC1}	Power supply	Analog circuit section power supply pin. Supply voltage is V_{CC} (same voltage as V_{CC2}).

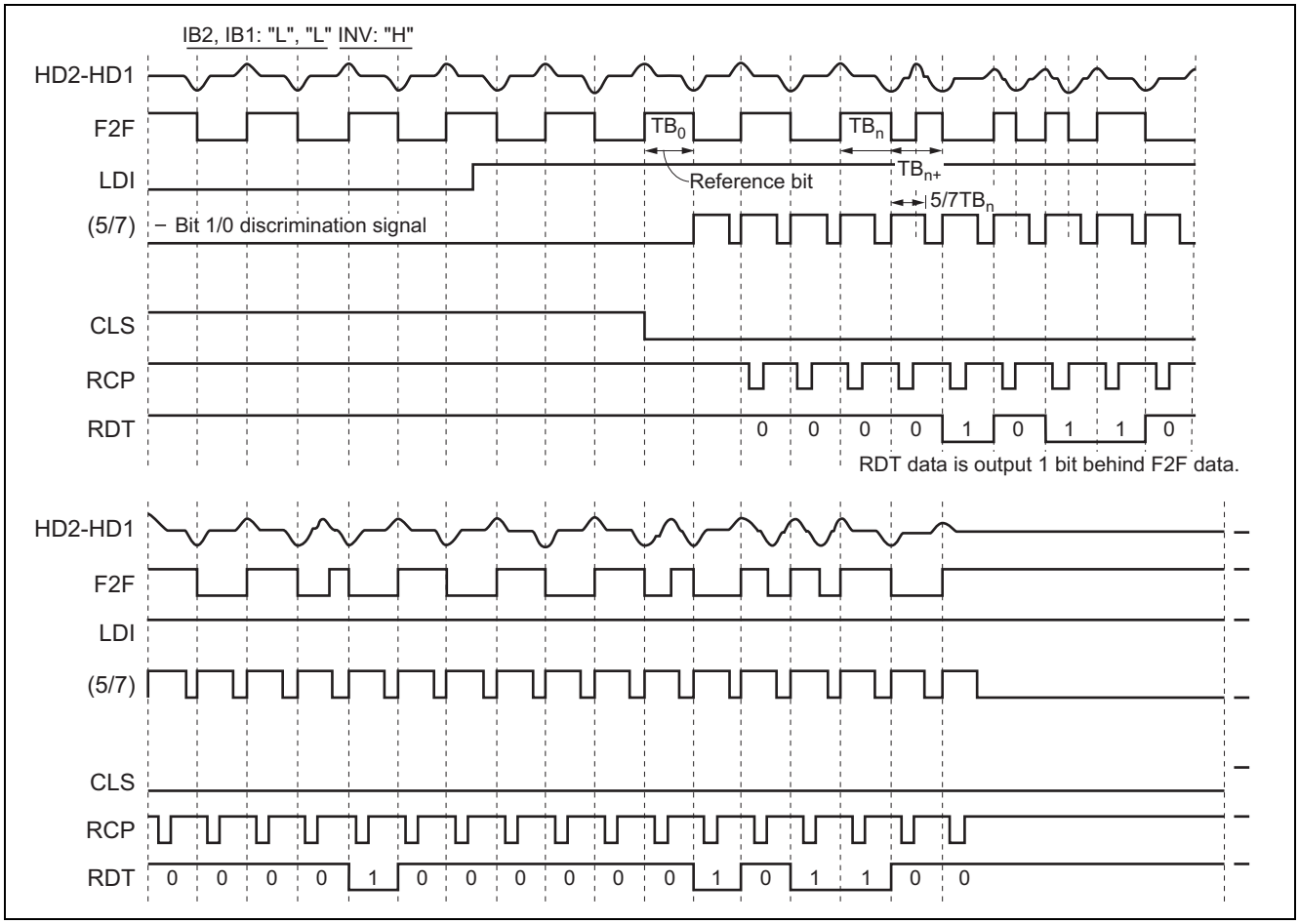
Glance-Over Bit Setting and Timing By IB1 and IB2

IB2 input	IB1 input	Number of glance-over bits	Description
L	L	4	Internal digital circuit is reset with LDI input at “L”.
L	H	8	LDI input may be at “H” at all times.
H	L	16	CLS output turns to “L” after counting the flux change FC (change in the status of F2F) of the number of glance-over bits, and returns to “H” when BIC (bit interval counter) has fully counted. (At “L” active).
H	H	—	—

Note: IB2, IB1 : “L”, “L”



Operating Timing Diagram



Absolute Maximum Ratings

(Ta = −20 to 75°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	−0.3 to +6.5	V	V_{CC1}, V_{CC2}
Input voltage	V_I	−0.3 to V_{CC}+0.3	V	LDI, IB1, IB2, INV
Input voltage	V_I	−0.3 to V_{CC}+0.3	V	HD1, HD2
Output voltage	I_O	−10 to +10	mA	CLS, RDT, RCP
Differential input voltage	V_{ID}	−1.2 to +1.2	V	Between HD2 and HD1 pins
Operating temperature	Topr	−20 to 75	°C	
Storage temperature	Tstg	−55 to 125	°C	

Notes: 1. Voltage is based on GND pin of the circuit (0 V), unless otherwise noted.
2. Direction of the current flowing into the circuit is represented by “positive” (without code) and that flowing out of the circuit by “negative” (−code).

Recommended Operating Conditions

(Ta = –20 to 75°C, unless otherwise noted)

Item		Symbol	Limits			Unit	Test Conditions
			Min	Typ	Max		
Supply voltage	V_{CC1}, V_{CC2}	V_{CC}	4.0	5	5.5	V	V_{CC1} and V_{CC2} shall have the identical voltage.
Input voltage	LDI	V_I	0	—	V_{CC}	V	
“H” input voltage	IB1, IB2, INV	V_{IH}	0.8V_{CC}	—	V_{CC}	V	
“L” input voltage	IB1, IB2, INV	V_{IL}	0	—	0.2V_{CC}	V	
“H” output current	CLS, RDT, RCP	I_{OH}	–0.5	—	0	mA	
“L” output current	CLS, RDT, RCP	I_{OL}	0	—	5	mA	
Differential input voltage	HD2-HD1	V_{IN}	3	—	80	mVp-p	
Input frequency	HD2-HD1	f_{IN}	0.3	—	15	kHz	
Oscillation frequency		f_{OSC}	0.2	—	2	MHz	$f_{OSC} = 1/T_{OSC}$
External capacitor	CX1, CX2	C_{OSC}	25	—	100	pF	$f_{OSC} \propto 1/C_{OSC}$
External capacitor	CX1, CX2	C_{OSC}	—	33	—	pF	Reference value when corresponding to 210BPI
External resistor	AMP	R_{PK}	—	470	—	Ω	Reference value when corresponding to 210BPI
External capacitor	PKI	C_{PK}	—	0.033	—	μF	Reference value when corresponding to 210BPI
External capacitor	PKI, PKO	C_{NF}	—	220	—	pF	Reference value
External resistor	PKI, F2F	R_{PF}	—	4.7	—	MΩ	Reference value
External capacitor	V_{CC1}, V_{CC2}	C_{VC}	—	0.1	—	μF	Reference value
External capacitor	VRF	C_{VR}	0.8	1	2	μF	Reference value

Electrical Characteristics

(Ta = –20 to 75°C, V_{CC} = 5 V, unless otherwise noted)

Item		Symbol	Test Circuit	Limits			Unit	Test Conditions	
				Min	Typ	Max			
Threshold voltage	IB1, IB2, INV	VTH	—	$0.3V_{CC}$	—	$0.7V_{CC}$	V	V_{CC} = 4 to 5.5 V	
"L" output voltage	CLS, RDT, RCP	V_{OL}	2	—	—	0.2	V	V_{CC} = 4 V	I_{OL} = 10 μA
			2	—	—	0.4	V		I_{OL} = 5 mA
"H" output voltage	CLS, RDT, RCP	V_{OH}	2	3.8	—	—	V	V_{CC} = 4 V	I_{OH} = –10 μA
			2	3.2	—	—	V		I_{OH} = –0.5 mA
"L" input current	LDI, IB1, IB2	IIL	2	–10	—	+10	μA	V_{CC} = 5.5 V, V_I = 0 V	
"L" input current	INV	IIL	2	–80	—	–10	mA	V_{CC} = 5.5 V, V_I = 0 V	
"H" input current	LDI, IB1, IB2, INV	IIH	2	–10	—	+10	μA	V_{CC} = 5.5 V, V_I = 5.5 V	
Positive threshold current	INV	IIT+	2	–250	—	–50	μA	V_{CC} = 5.5 V, V_I = VTH	
Reference voltage	VRF	VREF	1	2.3	2.5	2.7	V	V_{IN} = 0 mVp-p	
Voltage gain 1	OP1	GV11	3	18	20	24	Double	f_{IN} = 1 kHz V_{IN} = 80 mVp-p sine wave	
Voltage gain 2	OP1	GV21	3	18	20	24	Double	f_{IN} = 15 kHz V_{IN} = 80 mVp-p sine wave	
Input resistance	OP1	RIN1	3	7	10	14	kΩ	f_{IN} = 1 kHz V_{IN} = 80 mVp-p sine wave	
Maximum output voltage	OP1	VOPP1	3	2	—	—	Vp-p	f_{IN} = 1 kHz sine wave THD AMP = 5%	
"L" sensitivity current	PKI – F2F	IIL2	4	—	—	–0.3	μA	VM, F2F < 0.5 V	
"H" sensitivity current	PKI – F2F	IIH2	4	0.3	—	—	μA	VM, F2F > 4.5 V	
Positive threshold voltage	PKI – F2F	VTH+2	5	0.2	0.45	0.7	V	On the VRF basis	
Negative threshold voltage	PKI – F2F	VTH–2	5	–0.7	–0.45	–0.2	V	On the VRF basis	
Threshold differential voltage	PKI – F2F	VTHD2	—	–0.15	—	0.15	V	(VTH+2) – |VTH–2|	
Pin voltage range	PKO	VPKO	4	–1.2	—	1.2	V	On the VRF basis |PK| = 1 mA – +1 mA	
"L" output voltage	F2F	VOL3	5	—	—	0.5	V	VPKI = 0 V, IF2F = 0.5 mA	
"H" output voltage	F2F	VOH3	5	4.5	—	—	V	VPKI = 5 V, IF2F = –0.5 mA	
Positive threshold voltage	LDI	VTH+4	6	2.5	—	3.5	V		

(Ta = –20 to 75°C, V_{CC} = 5 V, unless otherwise noted)

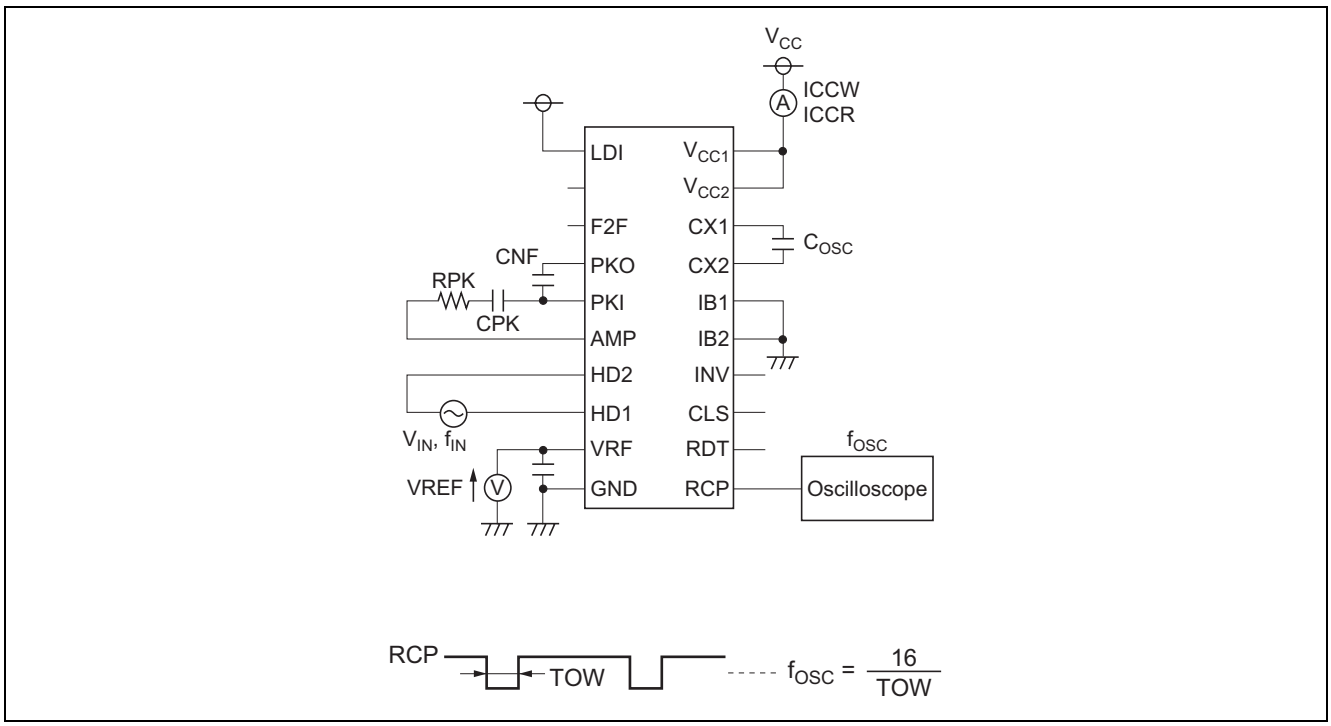
Item		Symbol	Test Circuit	Limits			Unit	Test Conditions
				Min	Typ	Max		
Negative threshold voltage	LDI	VTH–4	6	1.5	—	2.7	V	
Hysterisis width	LDI	VHY4	—	0.5	—	1.5	V	(VTH+4) – (VTH–4)
Standby circuit current	V_{CC1}, V_{CC2}	ICCW	1	—	0.7	1.0	mA	V_{IN} = 0 mVp-p
Operating circuit current	V_{CC1}, V_{CC2}	ICCR	1	—	1.9	2.4	mA	f_{IN} = 8.2 kHz V_{IN} = 68 mVp-p sine wave f_{OSC} = 1 MHz
Oscillation frequency	RCP	f_{OSC}	1	0.75	—	1.5	MHz	C_{OSC} = 33 pF
Output pulse width	RCP	TOW	7	15	16	17	µs	f_{OSC} = 1 MHz
Intra-output delay time	RDT, RCP	TOD	7	7	8	9	µs	f_{OSC} = 1 MHz
Input noise width	INV	TNW	7	0.5	—	—	µs	

Note: 1. Min. and max. limits do not represent absolute values.
2. Typ. limits represent standard values when Ta = 25°C and V_{CC} = 5V.

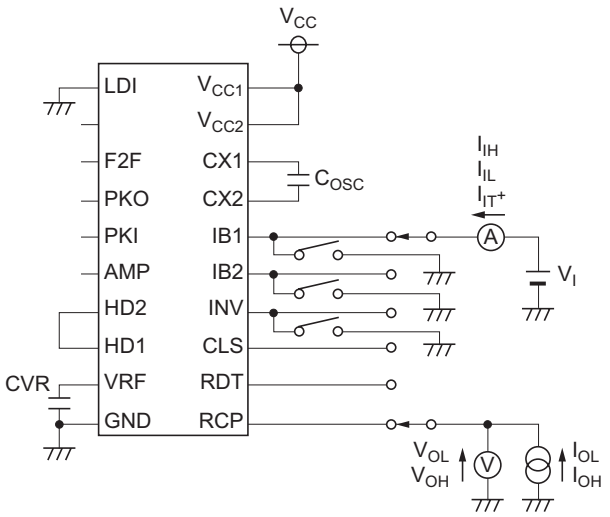
Test Circuit

On the following drawing, C_{OSC} = 33 pF, RPK = 470 Ω, CPK = 0.033 µF, CNF = 470 pF, CVR = 1 µF

1. Testing of VREF, ICCW, ICCR, fosc

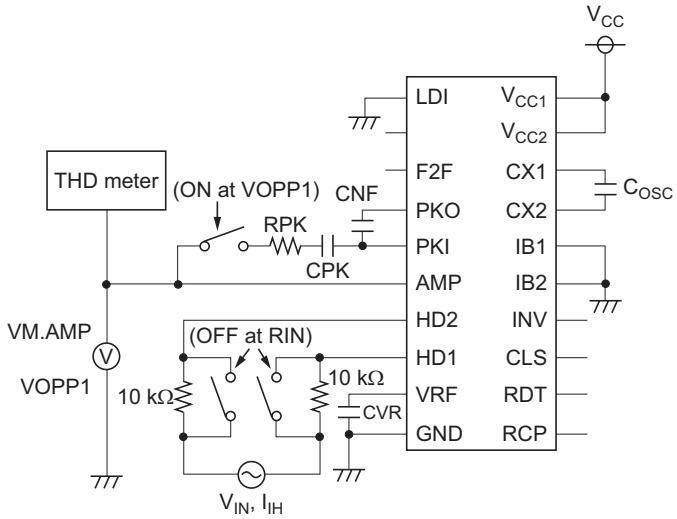


2. Testing of V_{OL}, V_{OH}, I_{IL}, I_{IH}, I_{IT+}



Note: Short the IB1 and IB2 to the GND when those pins are not used for testing.

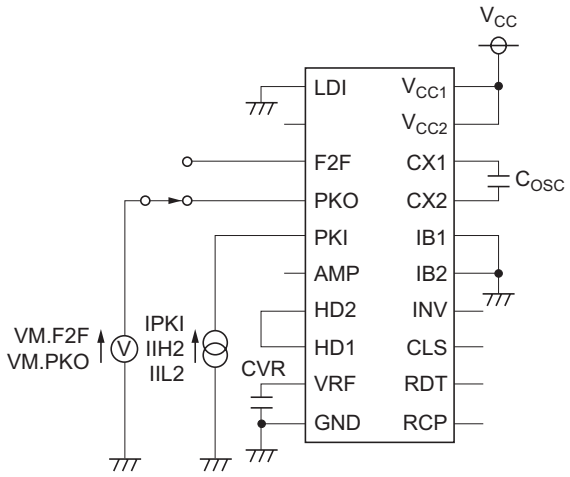
3. Testing of GV11, GV21, RIN1, VOPP1



$$GV11 = \frac{VM.AMP}{V_{IN}}$$

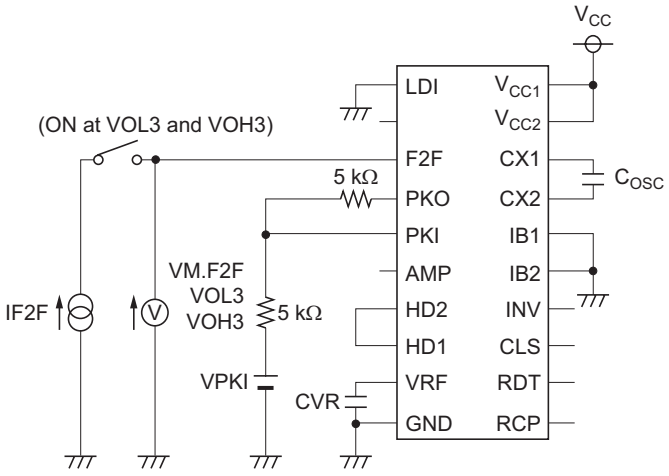
$$RIN1 = \frac{2VM.AMP}{GV11 \bullet V_{IN} - VM.AMP} \times 10\ (k\Omega)$$

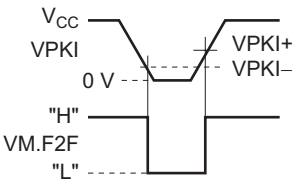
4. Testing of IIH2, IIL2, VPKO



Note: IIL2 is PKI input current providing VM.F2F < 0.5 V.
IIH2 is PKI input current providing VM.F2F > 4.5 V.
VPKO = VM.PKO – VREF

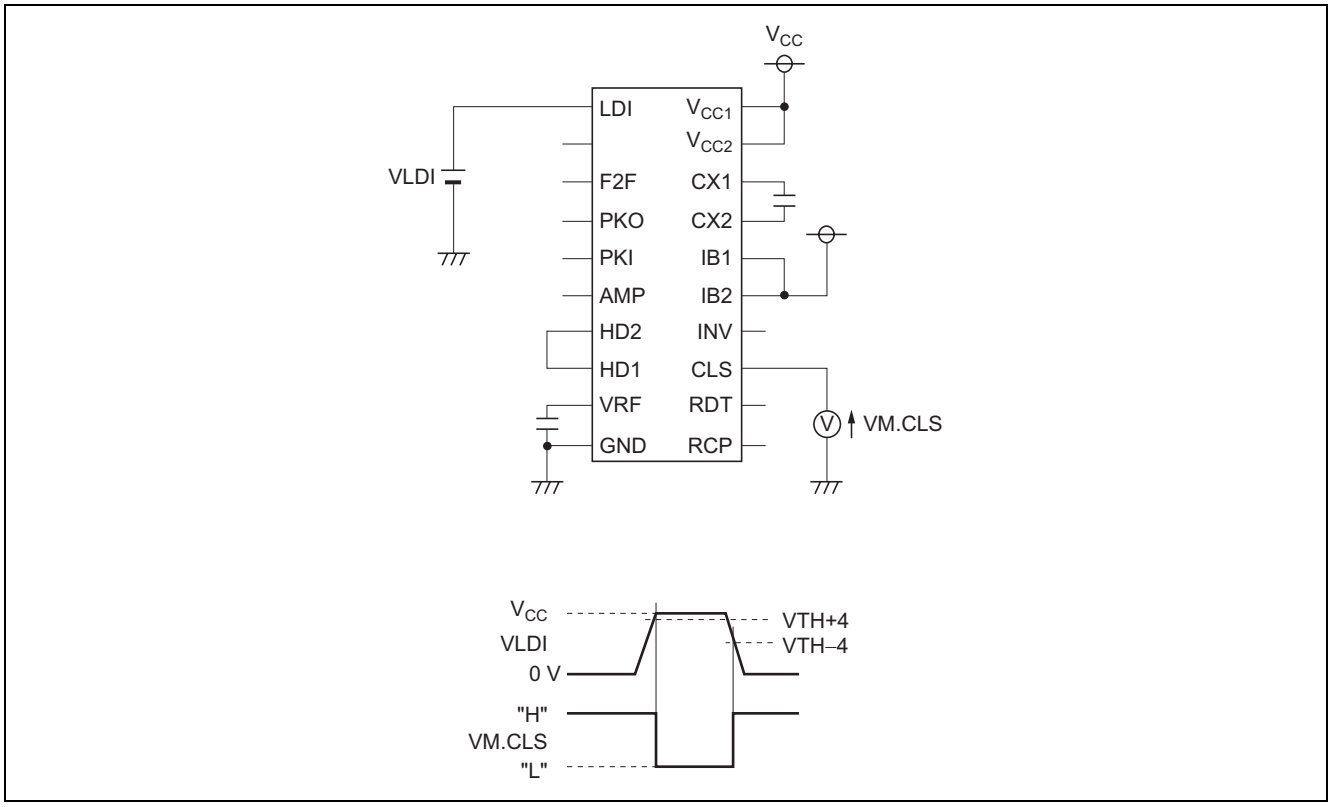
5. Testing of VTH+2, VTH–2, VOL3, VOH3



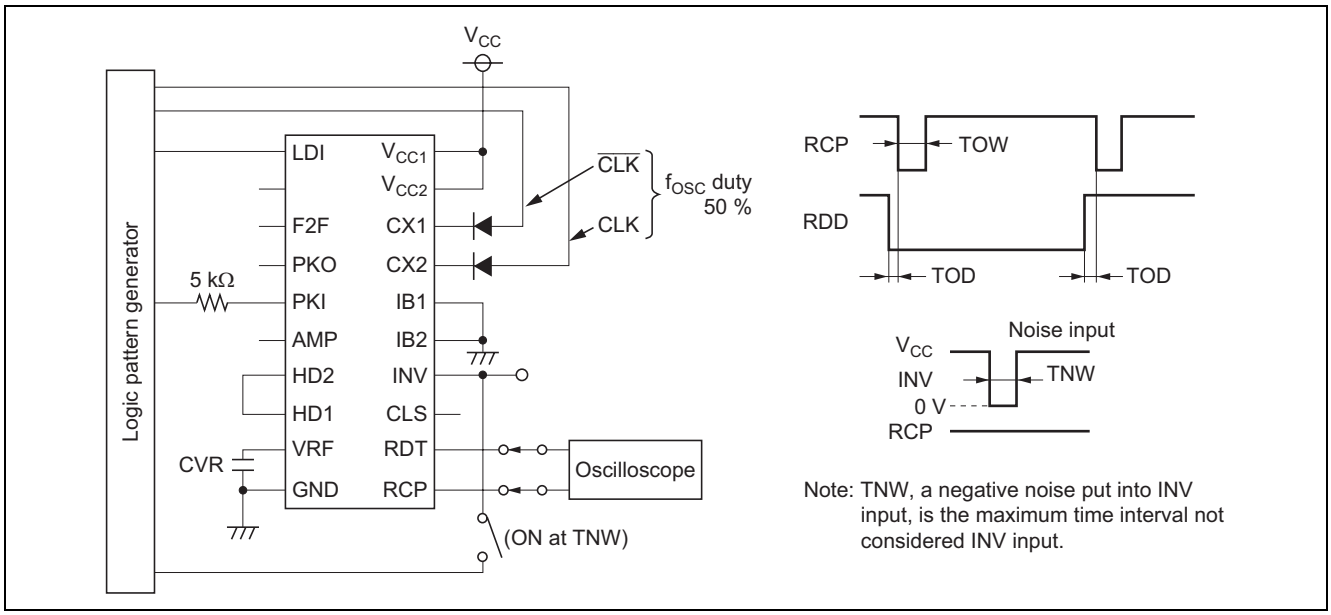


VTH+2 = VREF – VPKI–
VTH–2 = VREF – VPKI+

6. Testing of VTH+4, VTH−4



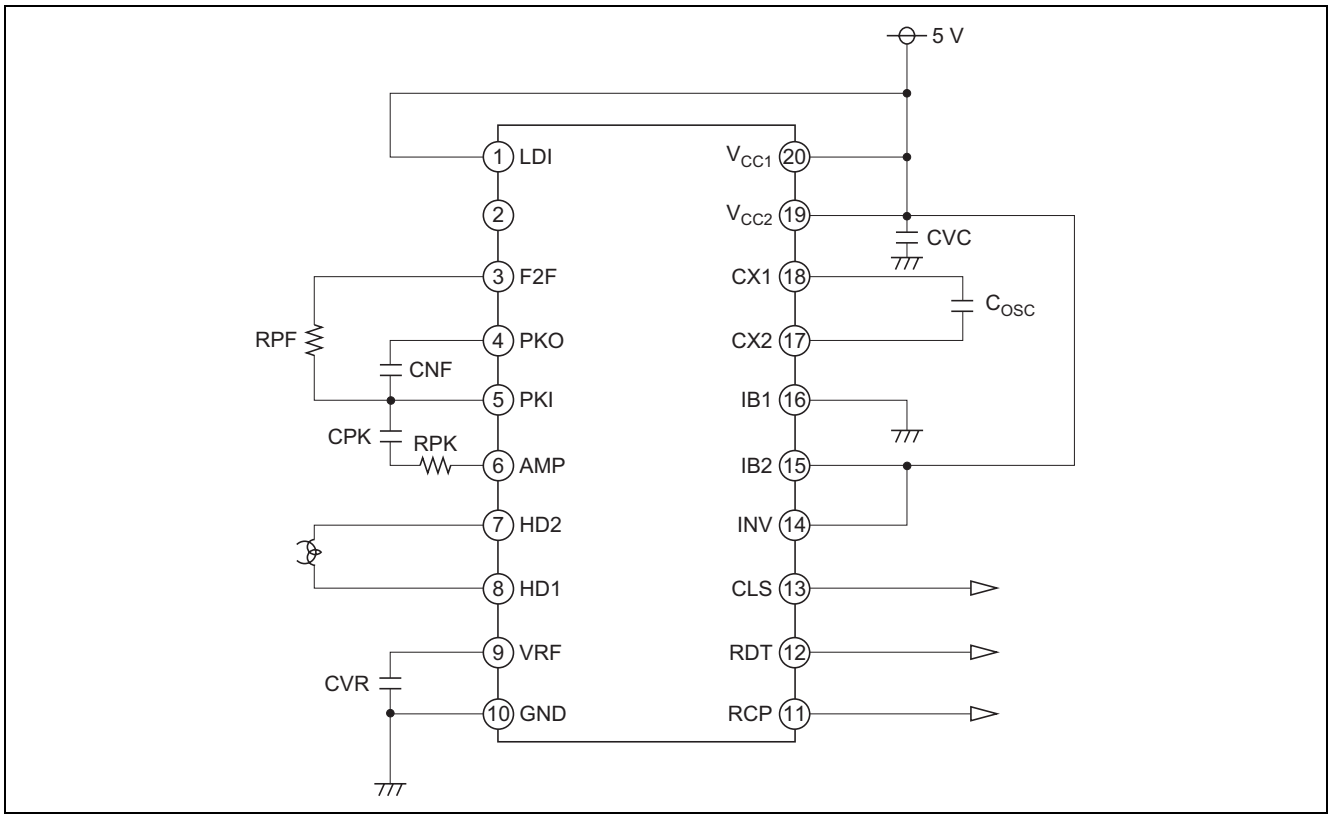
7. Testing of TOW, TOD, TNW



Note: TNW, a negative noise put into INV input, is the maximum time interval not considered INV input.

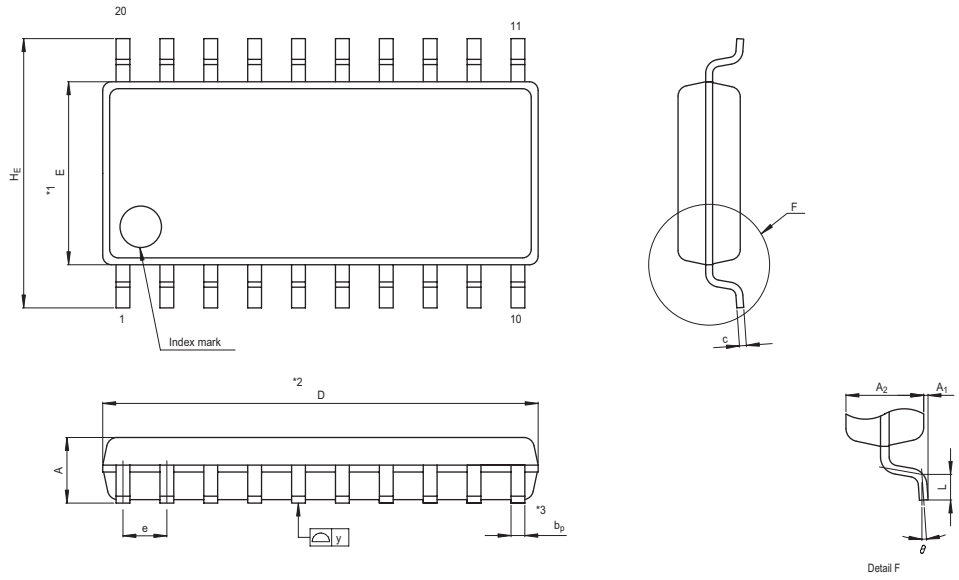
Application Example

When setting the glance-over bit to 16 bits to let it be “L” active output



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.3x12.6-1.27	PRSP0020DA-A	20P2N-A	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.5	12.6	12.7
E	5.2	5.3	5.4
A_2	—	1.8	—
A_1	0	0.1	0.2
A	—	—	2.1
b_p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

Colophon .7.2