

Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.059 at $V_{GS} = - 4.5$ V	- 4.5 ^a	4.9 nC
	0.098 at $V_{GS} = - 2.5$ V	- 4.5 ^a	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- Typical ESD Protection: 1700 V
- High Speed Switching
- Compliant to RoHS Directive 2002/95/EC

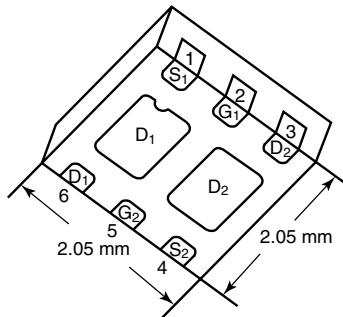


RoHS
COMPLIANT
HALOGEN
FREE

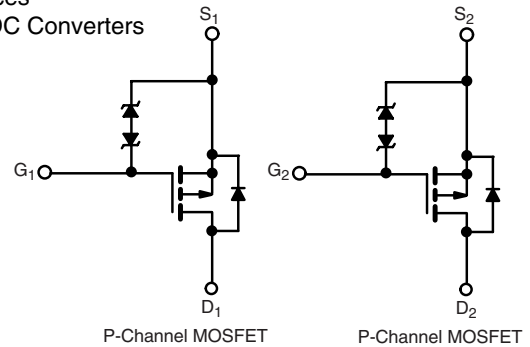
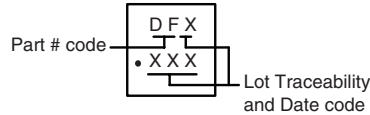
APPLICATIONS

- Load Switch, PA Switch and Battery Switch for Portable Devices
- DC/DC Converters

PowerPAK SC-70-6 Dual



Marking Code



Ordering Information: SiA921EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	- 4.5 ^a
		$T_C = 70$ °C	- 4.5 ^a
		$T_A = 25$ °C	- 4.5 ^{a, b, c}
		$T_A = 70$ °C	- 3.7 ^{b, c}
Pulsed Drain Current	I_{DM}	- 15	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	- 4.5 ^a
		$T_A = 25$ °C	- 1.6 ^{b, c}
Maximum Power Dissipation	P_D	$T_C = 25$ °C	7.8
		$T_C = 70$ °C	5
		$T_A = 25$ °C	1.9 ^{b, c}
		$T_A = 70$ °C	1.2 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	$t \leq 5$ s	R_{thJA}	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	12.5	16	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- See Solder Profile (www.vishay.com/ppg273257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 110 °C/W.

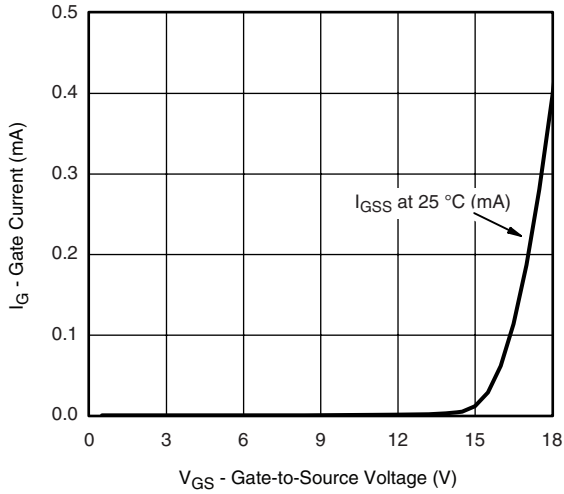
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-14		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.5		-1.4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			± 1	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 10	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-15			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -3.6\text{ A}$		0.048	0.059	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -1.5\text{ A}$		0.080	0.098	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -3.6\text{ A}$		11		S
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}, I_D = -4.7\text{ A}$		15	23	nC
				7.1	11	
				1.3		
Gate-Source Charge	Q_{gs}	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -4.7\text{ A}$		2.1		
Gate-Drain Charge	Q_{gd}			2.1		
Gate Resistance	R_g	$f = 1\text{ MHz}$		6.3		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 2.7\text{ }\Omega$ $I_D \cong -3.7\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		20	30	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 2.7\text{ }\Omega$ $I_D \cong -3.7\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		5	10	
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-4.5	A
Pulse Diode Forward Current	I_{SM}				-15	
Body Diode Voltage	V_{SD}	$I_S = -3.7\text{ A}, V_{GS} = 0\text{ V}$		-0.9	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -3.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		15	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			6	12	nC
Reverse Recovery Fall Time	t_a			8.5		ns
Reverse Recovery Rise Time	t_b			6.5		

Notes:

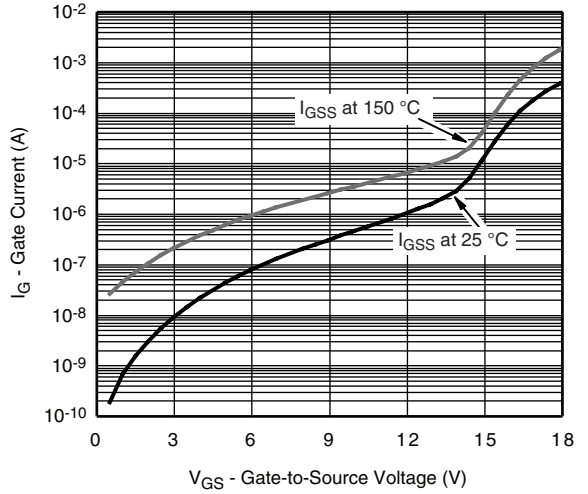
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

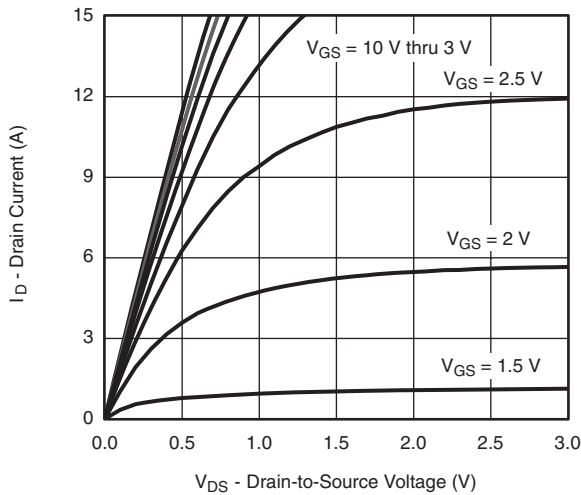
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



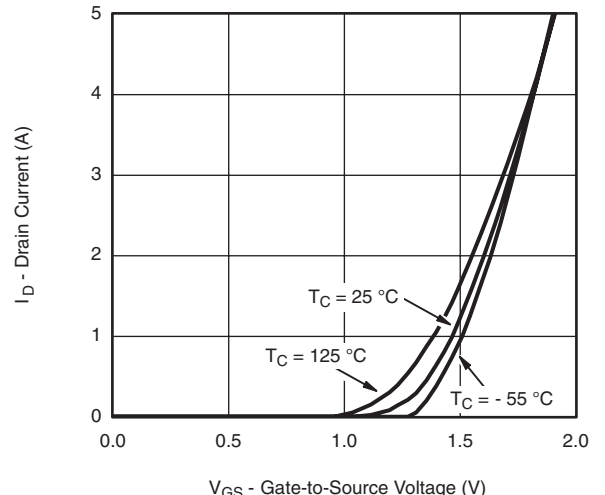
Gate Current vs. Gate-to-Source Voltage



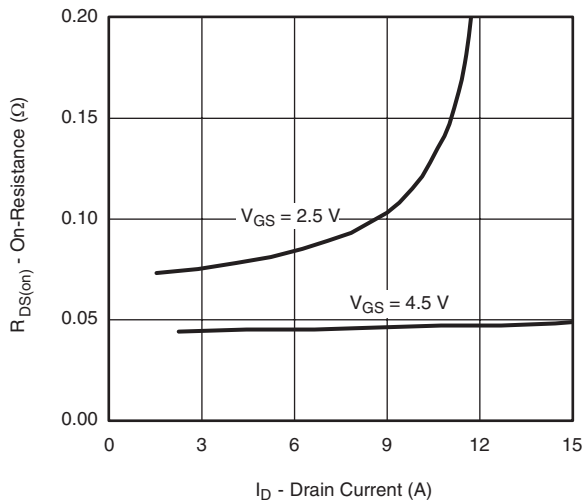
Gate Current vs. Gate-to-Source Voltage



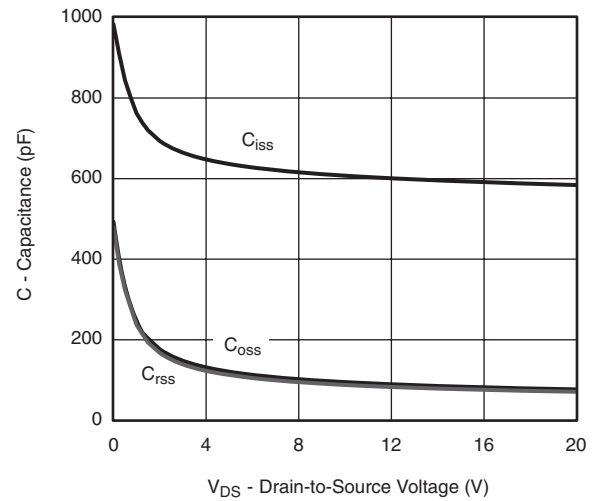
Output Characteristics



Transfer Characteristics

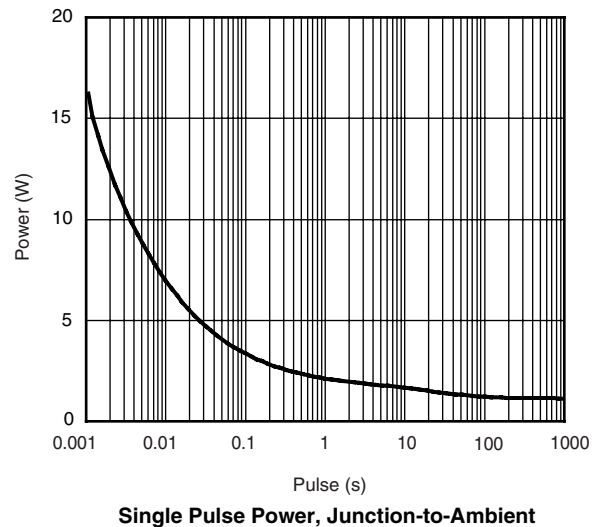
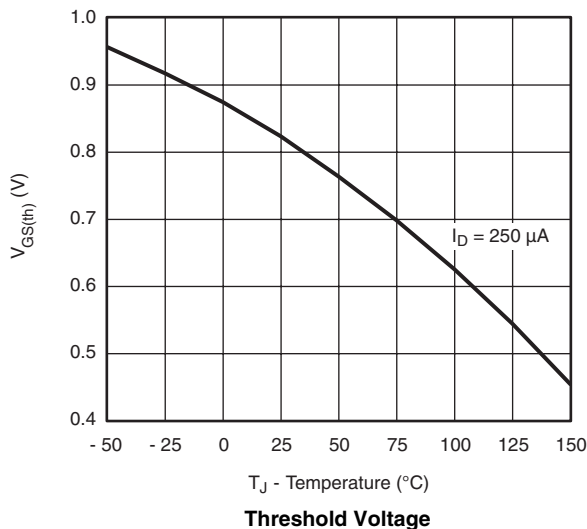
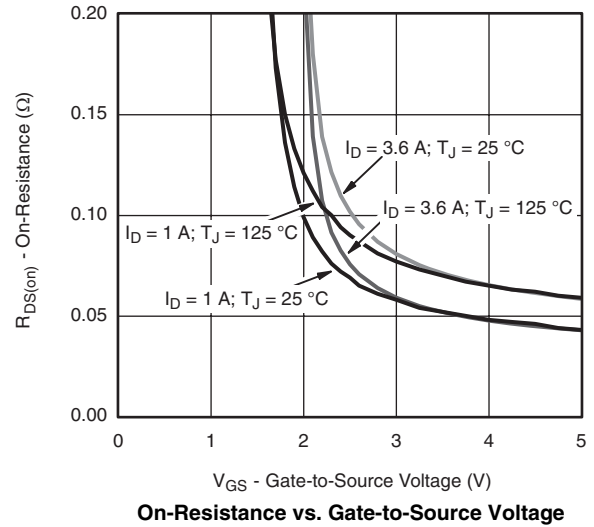
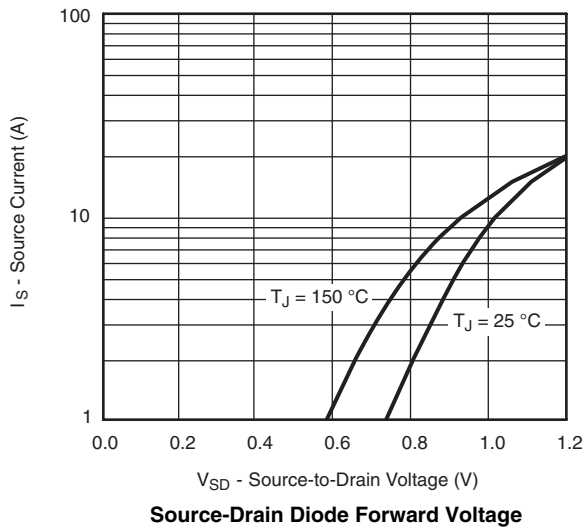
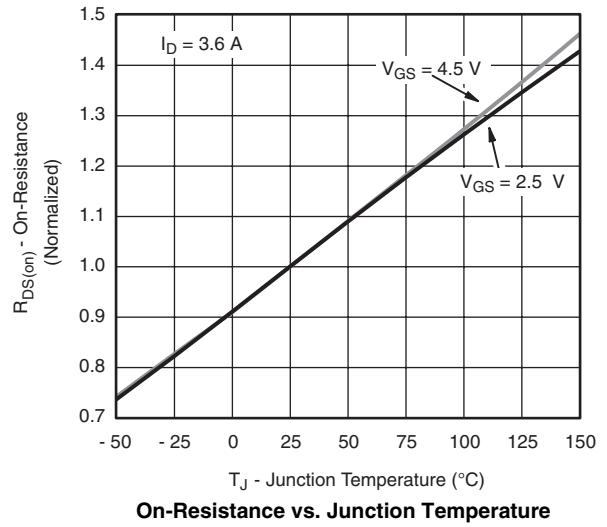
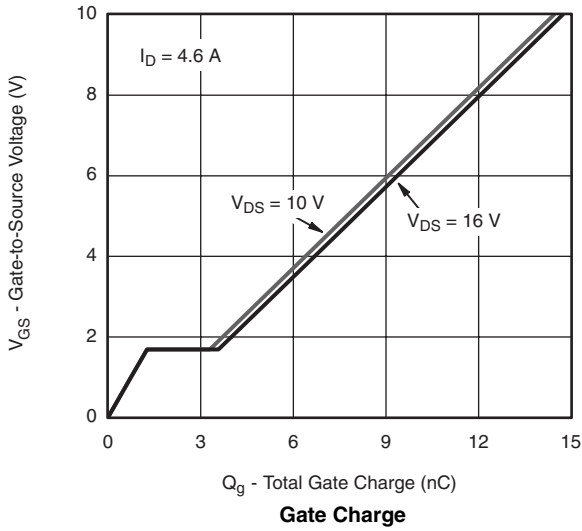


On-Resistance vs. Drain Current and Gate Voltage

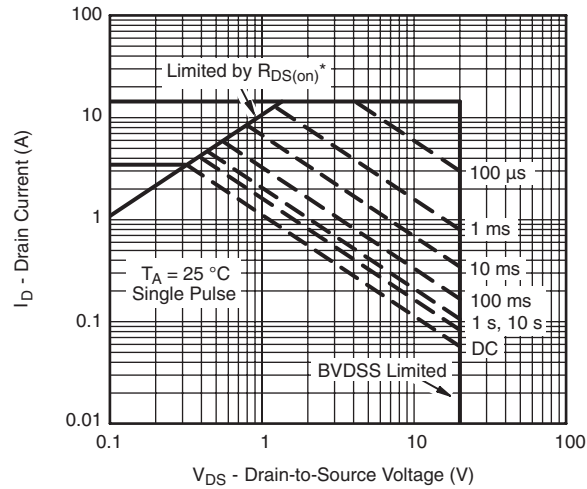


Capacitance

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

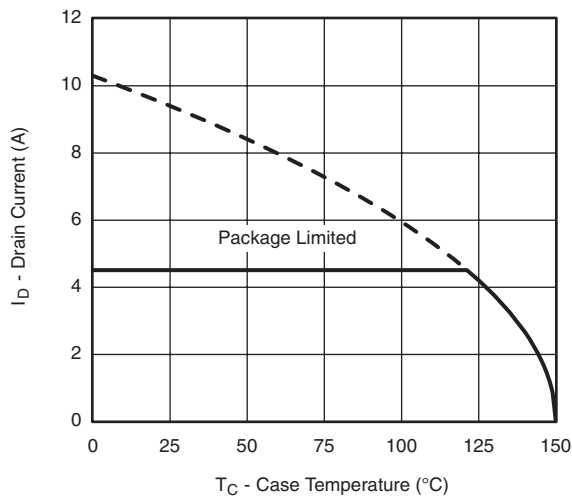


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

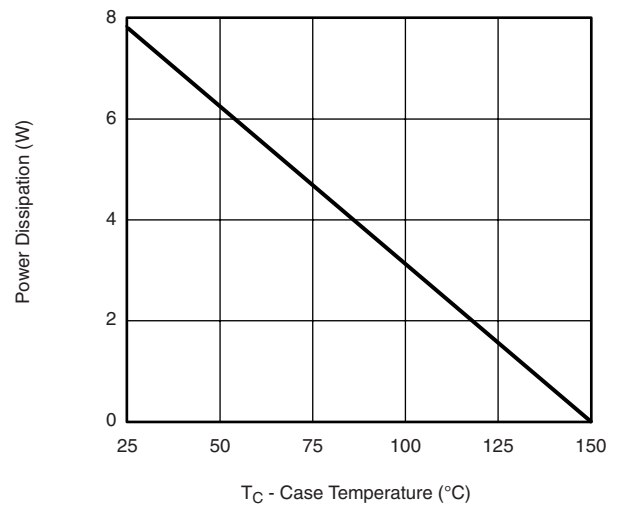


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



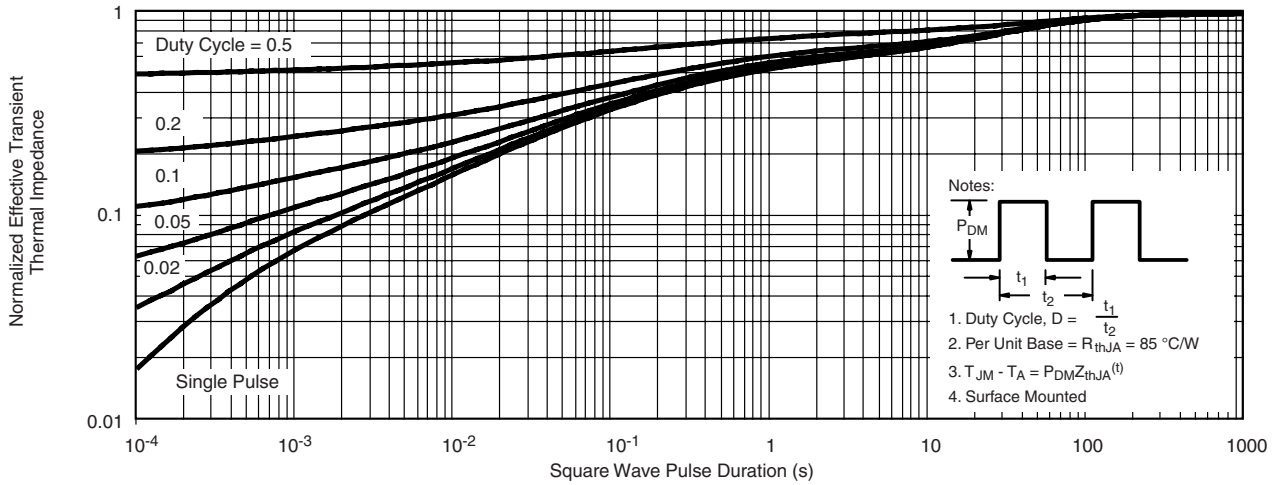
Current Derating*



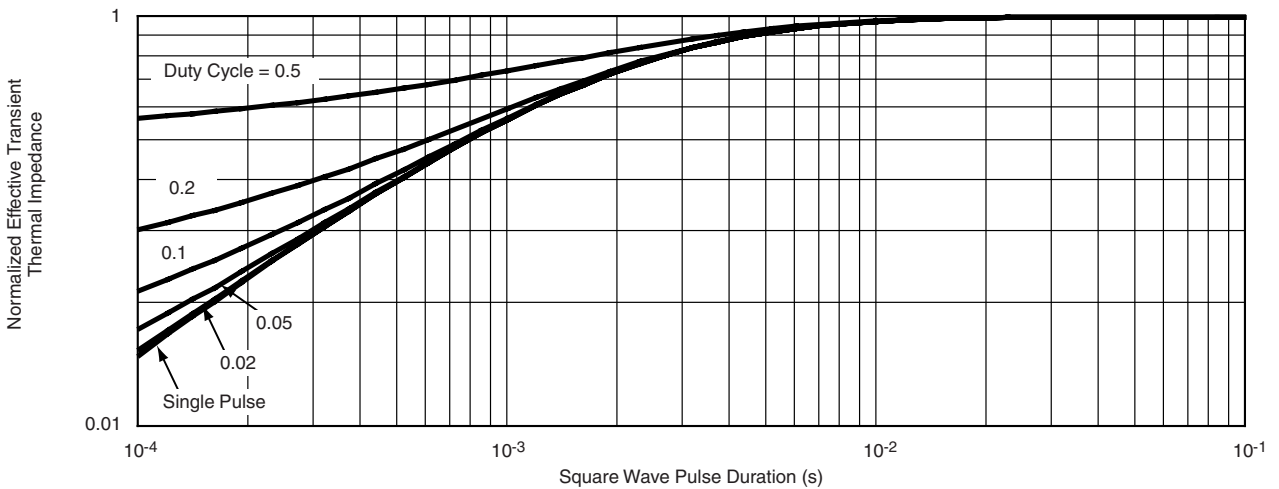
Power Derating

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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