STGW30N120KD

30 A - 1200 V - short circuit rugged IGBT

Features

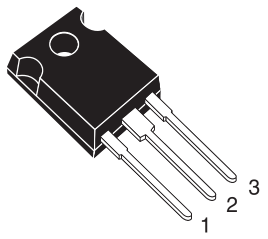
- Low on-losses
- High current capability
- Low gate charge
- Short circuit withstand time 10 µs
- IGBT co-packaged with ultra fast free-wheeling diode

Application

- Motor control

Description

This IGBT utilizes the advanced PowerMESH™ process resulting in an excellent trade-off between switching performance and low on-state behavior.



TO-247

Figure 1. Internal schematic diagram

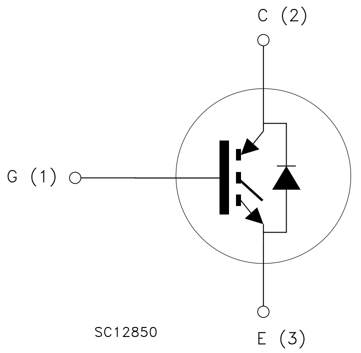


Table 1. Device summary

Order code	Marking	Package	Packaging
STGW30N120KD	GW30N120KD	TO-247	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0)	1200	V
I_C (1)	Collector current (continuous) at 25 °C	60	A
I_C (1)	Collector current (continuous) at 100 °C	30	A
I_{CL} (2)	Turn-off latching current	100	A
I_{CP} (3)	Pulsed collector current	100	A
V_{GE}	Gate-emitter voltage	±25	V
t_{scw}	Short circuit withstand time, V_{CE} = 0.5 $V_{(BR)CES}$ T_j = 125 °C, R_G = 10 Ω, V_{GE} = 12 V	10	µs
P_{TOT}	Total dissipation at T_C = 25 °C	175	W
I_F	Diode RMS forward current at T_C = 25 °C	30	A
I_{FSM}	Surge non repetitive forward current t_p = 10 ms sinusoidal	100	A
T_j	Operating junction temperature	– 55 to 125	°C

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Vclamp = 80% of V_{CES}, T_j =150 °C, R_G=10 Ω, V_{GE}=15 V
3. Pulse width limited by max. junction temperature allowed

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case IGBT max.	0.57	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case diode max.	1.6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient IGBT max.	50	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage (V_{GE} = 0)	I_C = 1 mA	1200			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE}= 15 V, I_C= 20 A V_{GE}= 15 V, I_C= 20 A, Tc =125 °C		2.8 2.7	3.85	V V
$V_{GE(th)}$	Gate threshold voltage	V_{CE}= V_{GE}, I_C= 1mA	4.5		6.5	V
I_{CES}	Collector cut-off current (V_{GE} = 0)	V_{CE} =1200 V V_{CE} =1200 V, Tc=125 °C			500 10	µA mA
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE} =± 20 V			± 100	nA
g_{fs}	Forward transconductance	V_{CE} = 25 V, I_C= 20 A		20		S

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE}=0		2520 170 33		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 960 V, I_C= 20 A,V_{GE}=15 V		105 21 56		nC nC nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, *(see Figure 17)*		36 22 840		ns ns A/µs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, Tc= 125 °C *(see Figure 17)*		35 22 760		ns ns A/µs
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, *(see Figure 17)*		70 251 260		ns ns ns
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, Tc= 125 °C *(see Figure 17)*		140 324 432		ns ns ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Eon (1) E_{off} (2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, *(see Figure 17)*		2.4 4.3 6.8		mJ mJ mJ
Eon (1) E_{off} (2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, Tc= 125 °C *(see Figure 17)*		3.9 5.8 9.7		mJ mJ mJ

1. Eon is the turn-on losses when a typical diode is used in the test circuit in *Figure 17*. If the IGBT is offered in a package with a co-pack diode, the co-pack diode is used as external diode. IGBTs and diode are at the same temperature (25°C and 125°C)
2. Turn-off losses include also the tail of the collector current

Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on-voltage	I_F = 20 A I_F = 20 A, T_C = 125 °C		1.9 1.7		V V
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_F = 20 A, V_R = 45 V, di/dt = 100 A/µs *(see Figure 20)*		84 235 5.6		ns nC A
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_F = 20 A, V_R = 45 V, Tc = 125 °C, di/dt = 100 A/µs *(see Figure 20)*		152 722 9		ns nC A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

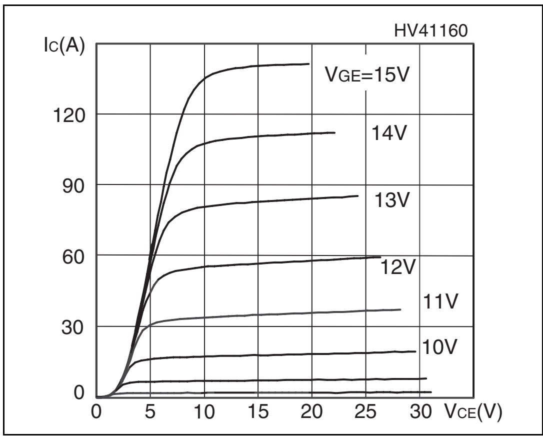


Figure 3. Transfer characteristics

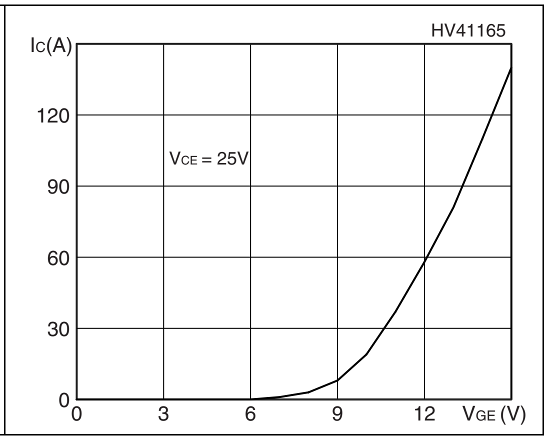


Figure 4. Transconductance

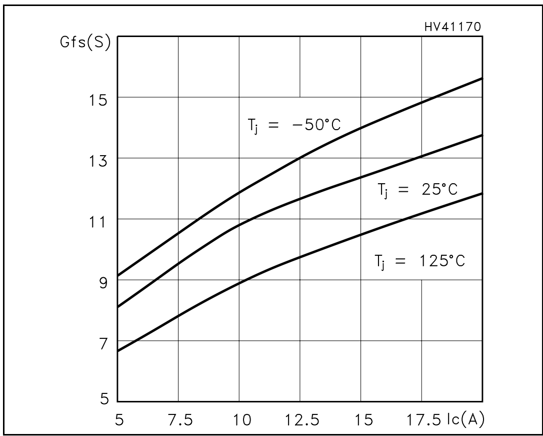


Figure 5. Collector-emitter on voltage vs. temperature

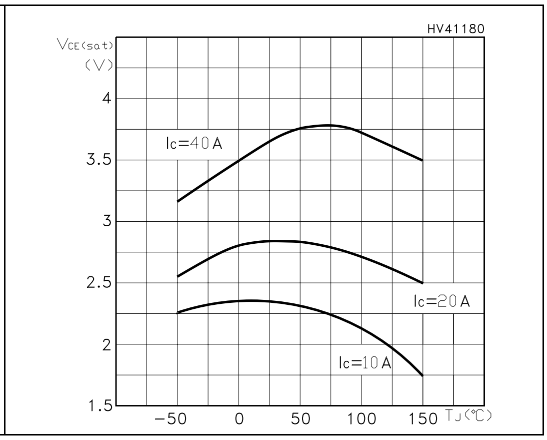


Figure 6. Gate charge vs. gate-source voltage

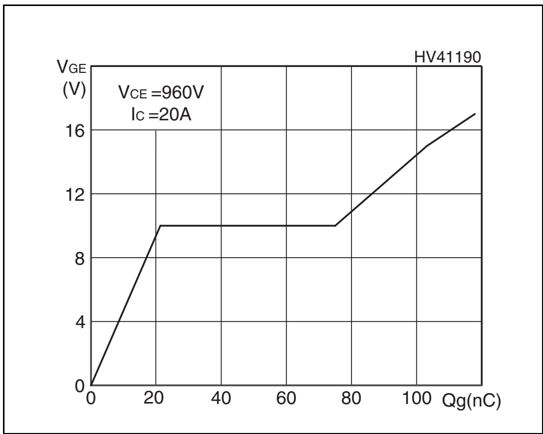


Figure 7. Capacitance variations

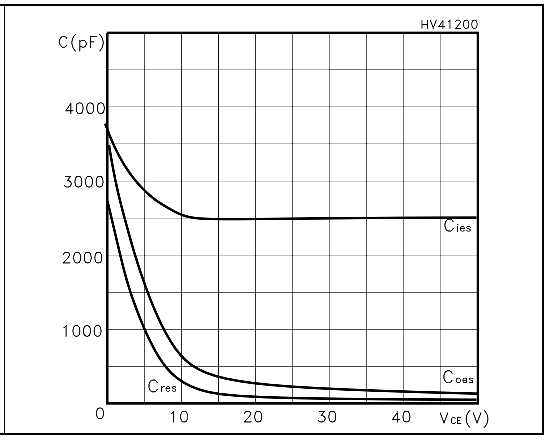


Figure 8. Normalized gate threshold voltage vs. temperature

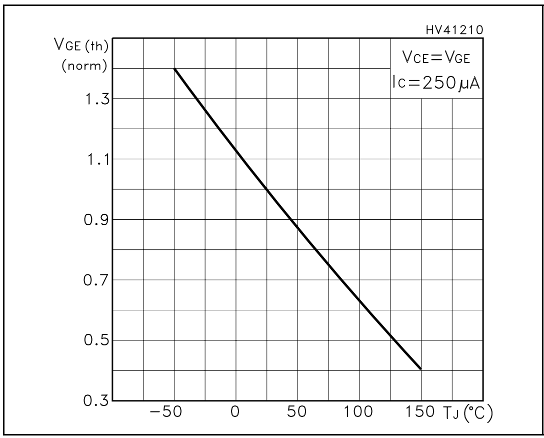


Figure 9. Collector-emitter on voltage vs. collector current

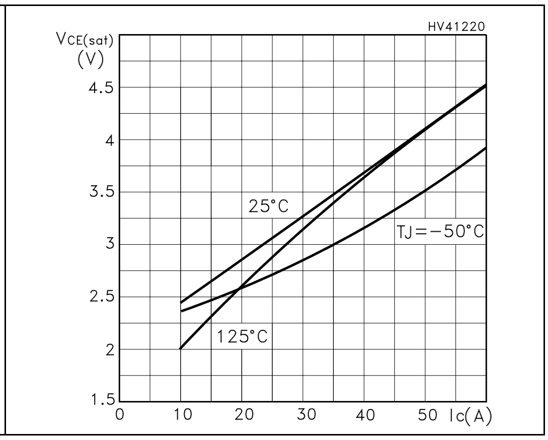


Figure 10. Normalized breakdown voltage vs. temperature

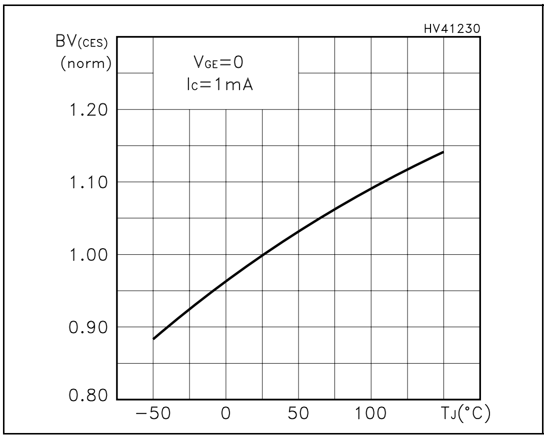


Figure 11. Switching losses vs. temperature

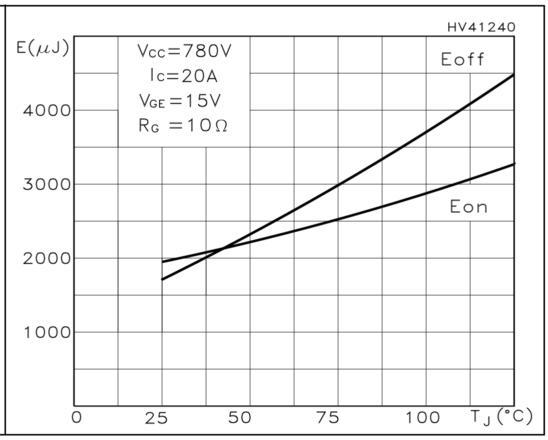


Figure 12. Switching losses vs. gate resistance

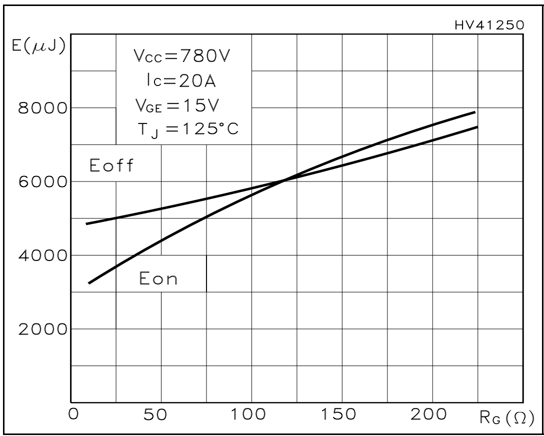


Figure 13. Switching losses vs. collector current

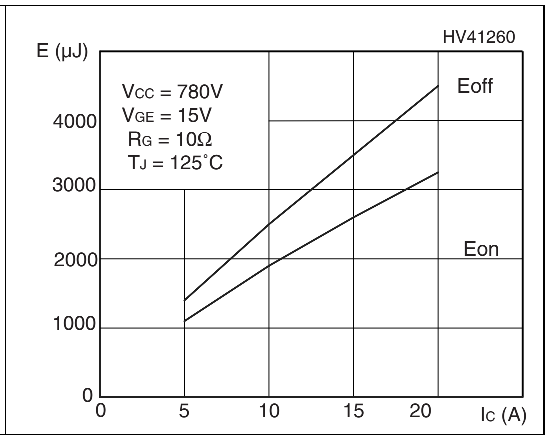


Figure 14. Thermal Impedance

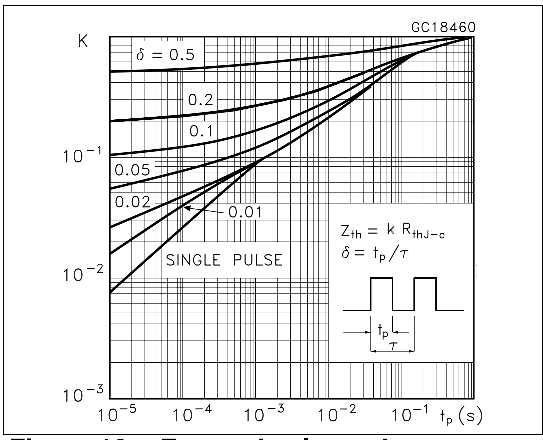


Figure 15. Turn-off SOA

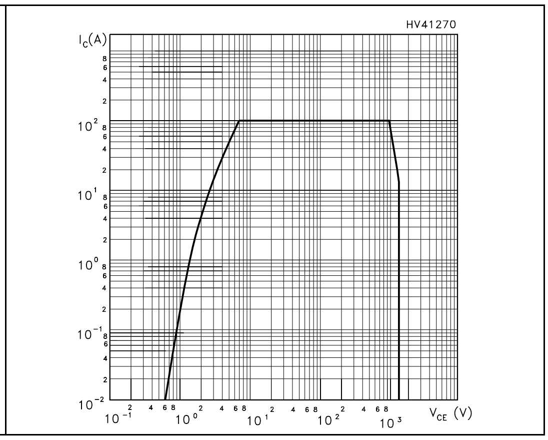
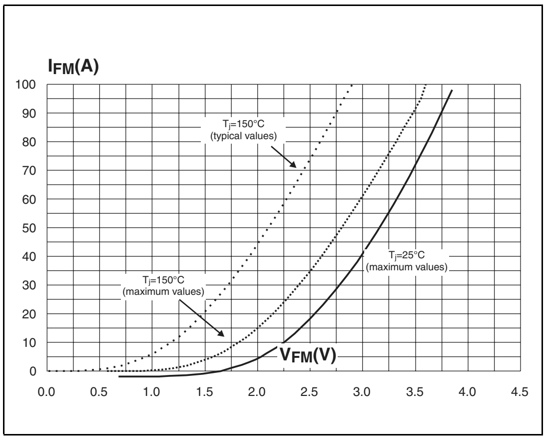


Figure 16. Forward voltage drop vs forward current



3 Test circuit

Figure 17. Test circuit for inductive load switching

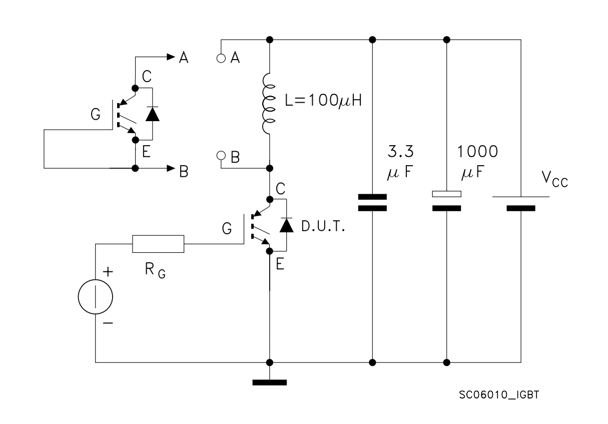


Figure 18. Gate charge test circuit

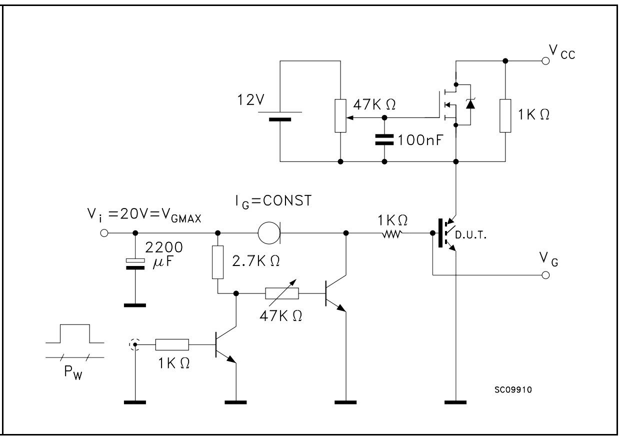


Figure 19. Switching waveform

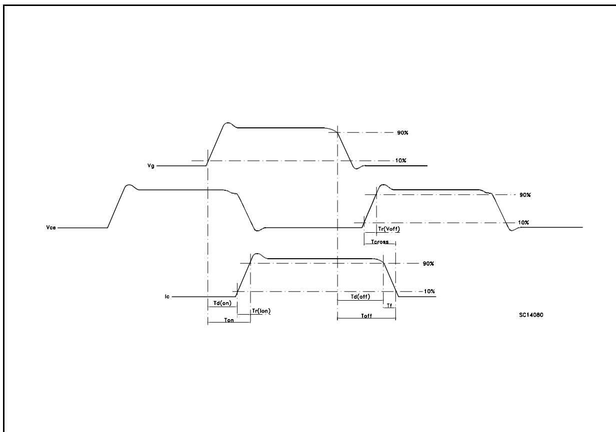
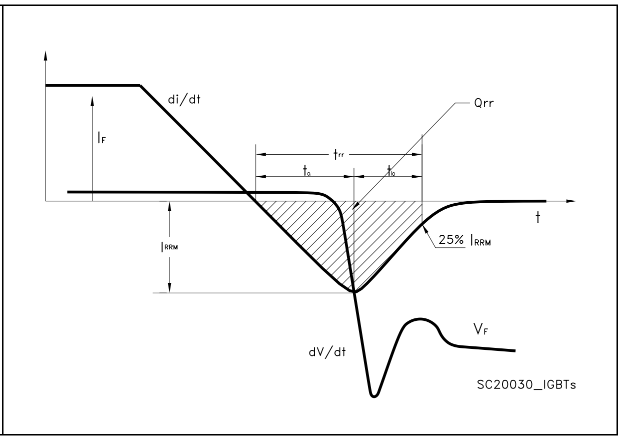


Figure 20. Diode recovery time waveform

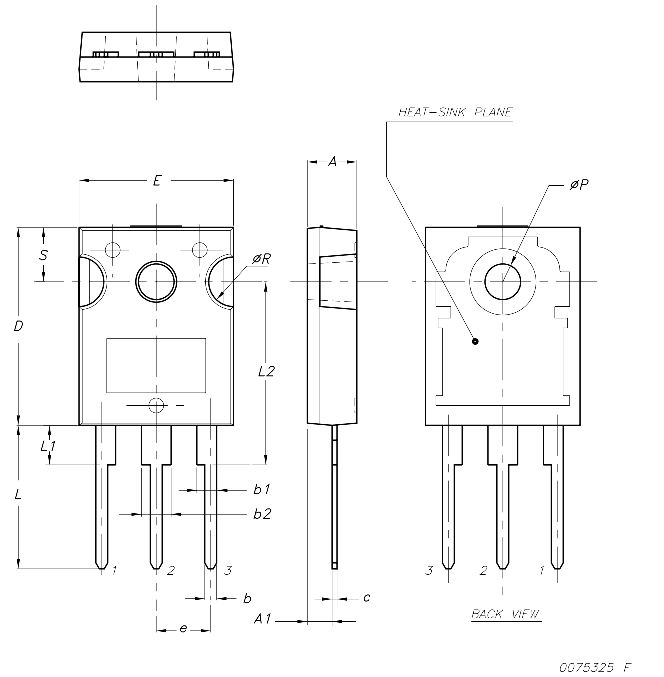


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
29-Jan-2008	1	Initial release
18-Jun-2008	2	Update values in *Table 2*