M66313FP

32-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

DESCRIPTION

The M66313FP is a semiconductor integrated circuit for LED array driver with 32-bit serial-input, parallel-output shift register, equipped with direct set input and output latches.

The M66313FP guarantees sufficient 24mA output current to drive anode common LED, allowing 32-bit simultaneous and continuous current output.

The parallel outputs are open-drain outputs.

The M66313FP employs CMOS technology, allowing considerable reduction of power dissipation, compared to previous BIPOLAR or Bi-CMOS products.

In addition, the pin configuration is suitable for easy wiring on the printed circuit board.

FEATURES

- High output current
  All parallel output I_{OL}=+24mA, LEDs can be turned on simultaneously.
- Low power dissipation : 200μW/package (max)
  (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin
  Employment of Schmitt-trigger circuit on all inputs allows application with long wiring.
- Direct set input ($\overline{S_D}$)
- Open-drain output ($\overline{Q_1}$~$\overline{Q_{32}}$)
- Serial data output for cascading (SQ_{32})
- Wide operating temperature range (T_a=−40~+85℃)
- Pin configuration for easy layout on PCB.
  (Pin configuration allows easy cascade connection or LED connection)

APPLICATION

LED array drive for eraser unit of a copying machine
LED array drive of a button telephone set
Various LED modules

FUNCTION

The employment of silicon gate CMOS process of the M66313FP guarantees low power dissipation and maintains high noise margin as well as high output current and high speed required to drive LEDs.

Each shift register bit consists of a flip-flop for shifting and an output latch.

The shift operation takes place when the clock input CK changes from low-level to high-level.

The serial data input A corresponds to the data input of the first-stage shift register, and the shift register is shifted in sequence when a pulse is applied to CK.

The parallel outputs $\overline{Q_1}$~$\overline{Q_{32}}$ are open-drain outputs.

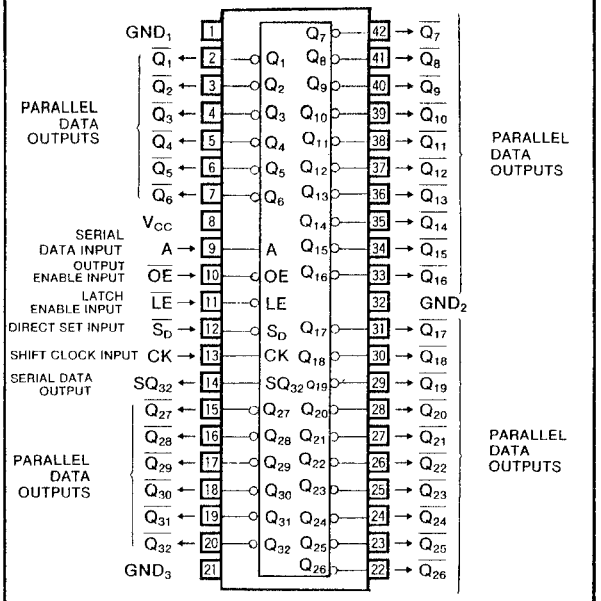
If the latch-enable input $\overline{LE}$ is turned high-level, the content of the shift register at that instant is latched.

To expand the number of bits, use the serial data output SQ_{32} which shows the output of the shift register of the 32nd bit.

If the direct set input $\overline{S_D}$ is turned low-level, shift register and latches are set.

If the high-level input is applied to the output enable input $\overline{OE}$, $\overline{Q_1}$~$\overline{Q_{32}}$ are set to the high-impedance state, but SQ_{32} is not set to the high-impedance state. The shift opration is not affected when $\overline{OE}$ is changed.

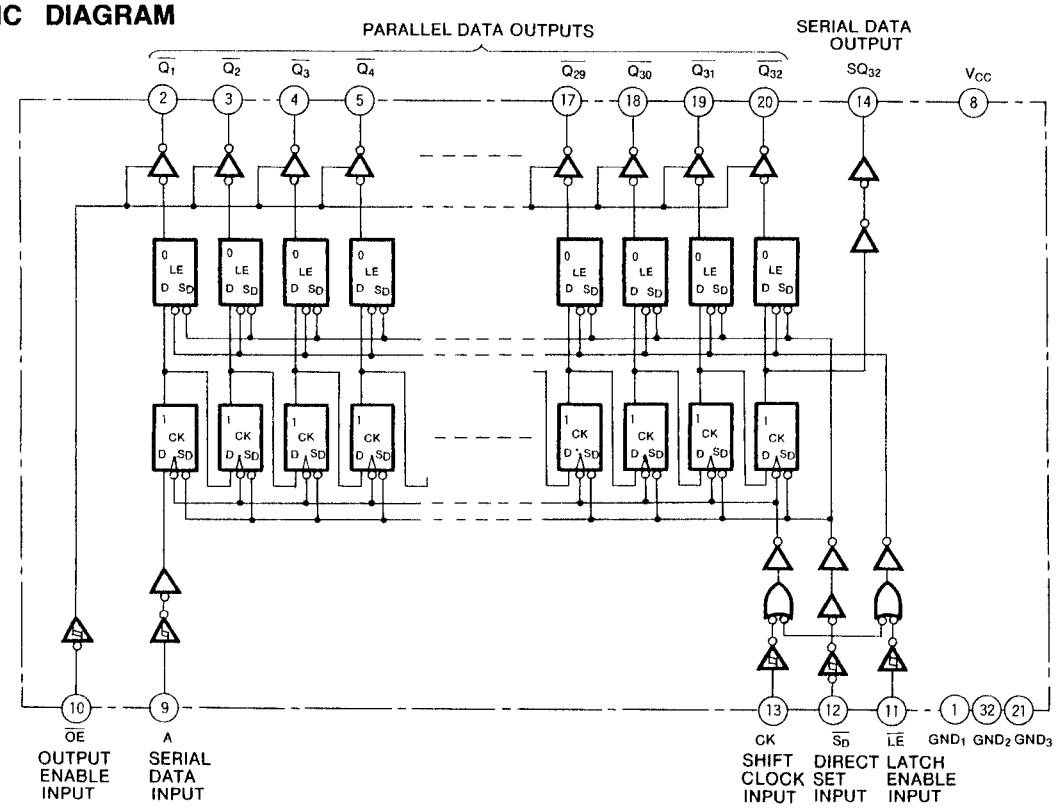
PIN CONFIGURATION (TOP VIEW)



Outline 42P2R-A

32-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

LOGIC DIAGRAM



FUNCTIONAL TABLE (Note 1)

OPERATION MODE	INPUT					PARALLEL OUTPUTS																																			SERIAL OUTPUT
	$\overline{S_D}$	CK	$\overline{LE}$	A	$\overline{OE}$	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{11}	Q_{12}	Q_{13}	Q_{14}	Q_{15}	Q_{16}	Q_{17}	Q_{18}	Q_{19}	Q_{20}	Q_{21}	Q_{22}	Q_{22}	Q_{23}	Q_{24}	Q_{25}	Q_{26}	Q_{27}	Q_{28}	Q_{29}	Q_{30}	Q_{31}	Q_{32}	SQ_{32}
SET	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
SHIFT	H	↑	L	H	L	L	$\overline{Q^0_1}$	$\overline{Q^0_2}$	$\overline{Q^0_3}$	$\overline{Q^0_4}$	$\overline{Q^0_5}$	$\overline{Q^0_6}$	$\overline{Q^0_7}$	$\overline{Q^0_8}$	$\overline{Q^0_9}$	$\overline{Q^0_{11}}$	$\overline{Q^0_{12}}$	$\overline{Q^0_{13}}$	$\overline{Q^0_{14}}$	$\overline{Q^0_{15}}$	$\overline{Q^0_{16}}$	$\overline{Q^0_{17}}$	$\overline{Q^0_{18}}$	$\overline{Q^0_{19}}$	$\overline{Q^0_{20}}$	$\overline{Q^0_{21}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{23}}$	$\overline{Q^0_{24}}$	$\overline{Q^0_{25}}$	$\overline{Q^0_{26}}$	$\overline{Q^0_{27}}$	$\overline{Q^0_{28}}$	$\overline{Q^0_{29}}$	$\overline{Q^0_{30}}$	$\overline{Q^0_{31}}$	q^0_{31}
	H	↑	L	L	L	Z	$\overline{Q^0_1}$	$\overline{Q^0_2}$	$\overline{Q^0_3}$	$\overline{Q^0_4}$	$\overline{Q^0_5}$	$\overline{Q^0_6}$	$\overline{Q^0_7}$	$\overline{Q^0_8}$	$\overline{Q^0_9}$	$\overline{Q^0_{11}}$	$\overline{Q^0_{12}}$	$\overline{Q^0_{13}}$	$\overline{Q^0_{14}}$	$\overline{Q^0_{15}}$	$\overline{Q^0_{16}}$	$\overline{Q^0_{17}}$	$\overline{Q^0_{18}}$	$\overline{Q^0_{19}}$	$\overline{Q^0_{20}}$	$\overline{Q^0_{21}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{23}}$	$\overline{Q^0_{24}}$	$\overline{Q^0_{25}}$	$\overline{Q^0_{26}}$	$\overline{Q^0_{27}}$	$\overline{Q^0_{28}}$	$\overline{Q^0_{29}}$	$\overline{Q^0_{30}}$	$\overline{Q^0_{31}}$	q^0_{31}
LATCH	H	X	H	X	L	$\overline{Q^0_1}$	$\overline{Q^0_2}$	$\overline{Q^0_3}$	$\overline{Q^0_4}$	$\overline{Q^0_5}$	$\overline{Q^0_6}$	$\overline{Q^0_7}$	$\overline{Q^0_8}$	$\overline{Q^0_9}$	$\overline{Q^0_{11}}$	$\overline{Q^0_{12}}$	$\overline{Q^0_{13}}$	$\overline{Q^0_{14}}$	$\overline{Q^0_{15}}$	$\overline{Q^0_{16}}$	$\overline{Q^0_{17}}$	$\overline{Q^0_{18}}$	$\overline{Q^0_{19}}$	$\overline{Q^0_{20}}$	$\overline{Q^0_{21}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{23}}$	$\overline{Q^0_{24}}$	$\overline{Q^0_{25}}$	$\overline{Q^0_{26}}$	$\overline{Q^0_{27}}$	$\overline{Q^0_{28}}$	$\overline{Q^0_{29}}$	$\overline{Q^0_{30}}$	$\overline{Q^0_{31}}$	$\overline{Q^0_{32}}$	q_{32}
OUTPUT DIS-ABLE	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q_{32}

Note 1 ↑ : Transition from low-to-high-level.
$\overline{Q^0}$: Shows the status of output Q before CK input changes.
X : Irrelevant
q^0 : The content of shift register before CK changes.
q : The content of the shift register.
Z : High-impedance state.

ABSOLUTE MAXIMUM RATINGS (T_a=−40∼+85℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5∼+7.0	V
V_I	Input voltage			−0.5∼V_{CC}+0.5	V
V_O	Output voltage			−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current		V_I < 0V	−20	mA
			V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current		V_O < 0V	−20	mA
			V_O > V_{CC}	20	
I_O	Output current	Q_1∼Q_{32}		50	mA
		SQ_{32}		±25	
I_{CC}	Supply/GND current		V_{CC}, GND	−920, +20	mA
P_d	Power dissipation			650	mW
Tstg	Storage temperature range			−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
Topr	Operating free-air ambient temperature range	−40		+85	℃

ELECTRICAL CHARACTERISTICS (V_{CC}=4.5~5.5V, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits					Unit
					T_a=25℃			T_a=−40~+85℃		
					Min	Typ*	Max	Min	Max	
V_{T+}	Positive-going threshold voltage		V_O=0.1V, V_{CC}−0.1V $\|I_O\|$=20μA		0.35XV_{CC}	2.8	0.7XV_{CC}	0.35XV_{CC}	0.7XV_{CC}	V
V_{T-}	Negative-going threshold voltage		V_O=0.1V, V_{CC}−0.1V $\|I_O\|$=20μA		0.2XV_{CC}	2	0.55XV_{CC}	0.2XV_{CC}	0.55XV_{CC}	V
V_{OH}	High-level output voltage	SQ_{32}	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OH}=−20μA	V_{CC}−0.1			V_{CC}−0.1		V
				I_{OH}=−4mA	3.83			3.66		
V_{OL}	Low-level output voltage	$\overline{Q_1}$~$\overline{Q_{32}}$	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OL}=20μA			0.1		0.1	V
				I_{OL}=24mA		0.20	0.41		0.50	
				I_{OL}=28mA		0.25	0.48		0.55(Note 2)	
		SQ_{32}		I_{OL}=20μA			0.1		0.1	
				I_{OL}=4mA			0.44		0.53	
I_{IH}	High-level input current		V_I=V_{CC}, V_{CC}=5.5V				0.5		5.0	μA
I_{IL}	Low-level input current		V_I=GND, V_{CC}=5.5V				−0.5		−5.0	μA
I_O	Maximum output leak current	$\overline{Q_1}$~$\overline{Q_{32}}$	V_I=V_{T+}, V_{T-} V_{CC}=5.5V	V_O=V_{CC}			1.0		10.0	μA
				V_O=GND			−1.0		−10.0	
I_{CC}	Quiescent state dissipation current		V_I=V_{CC}, GND V_{CC}=5.5V				40.0		400.0	μA

* : All typical values are at V_{CC}=5V, T_a=25℃
Note 2 : T_a=−40~+70℃

SWITCHING CHARACTERISTICS (V_{CC}= 5 V)

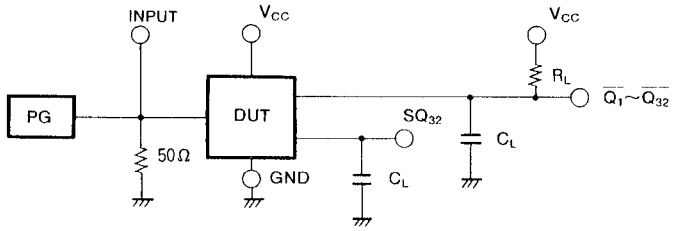
Symbol	Parameter		Test conditions	Limits					Unit
				T_a=25℃			T_a=−40~+85℃		
				Min	Typ	Max	Min	Max	
fmax	Maximum clock frequency		C_L=50pF R_L=1kΩ (Note 3)	5	30		4		MHz
t_{PZL}	Output enable time to low-level	CK-$\overline{Q_1}$~$\overline{Q_{32}}$(Turned on)			35	150		200	ns
t_{PLZ}	Output disable time from low-level	CK-$\overline{Q_1}$~$\overline{Q_{32}}$(Turned off)			35	200		250	ns
t_{PLH}	Low-to-high, high-to-low output propagation time	CK-SQ_{32}			35	100		130	ns
t_{PHL}					40	100		130	ns
t_{PZL}	Output enable time to low-level	$\overline{S_D}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned on)			35	150		200	ns
t_{PLH}	Low-to-high output propagation time	$\overline{S_D}$-SQ_{32}			40	100		130	ns
t_{PZL}	Output enable time to low-level	$\overline{LE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned on)			30	100		130	ns
t_{PLZ}	Output disable time from low-level	$\overline{LE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned off)			35	150		200	ns
t_{PZL}	Output enable time to low-level	$\overline{OE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned on)			30	100		130	ns
t_{PLZ}	Output disable time from low-level	$\overline{OE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned off)			35	150		200	ns
C_I	Input capacitance				3	10		10	pF
C_O	Output capacitance		$\overline{OE}$=V_{CC}		6	15		15	pF
C_{PD}	Power dissipation capacitance(Note 4)				160				pF

Note 4 : C_{PD} is the equivalent capacitance of IC calculated by the operating power dissipation without load. The operating power dissipation without load is given as follows:
P_D=C_{PD} · V_{CC}^2 · f_I+I_{CC} · V_{CC}

TIMING REQUIREMENT (V_{CC}= 5 V)

Symbol	Parameter	Test conditions	Limits					Unit
			T_a=25℃			T_a=−40～+85℃		
			Min	Typ	Max	Min	Max	
t_w	CK, $\overline{LE}$, $\overline{S_D}$ pulse width	(Note 3)	100	16		130		ns
t_{su}	Setup time A to CK		100	27		130		ns
t_h	Hold time A to CK		10	5		15		ns
	Hold time $\overline{LE}$ to CK		50	15		70		
t_{rec}	Recovery time CK to $\overline{S_D}$		50	20		70		ns

Note 3 : Test circuit



(1) Characteristics of pulse generator(PG): t_r= 6 ns, t_f= 6 ns
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM