I²C BUS compatible serial EEPROM

BR24C08 / BR24C08F / BR24C08FJ / BR24C08FV / BR24C16 / BR24C16F / BR24C16FJ / BR24C16FV / BR24E16 / BR24E16F / BR24E16FJ / BR24E16FV /

The BR24C08, BR24C16 and BR24E16 series are 2-wire (I²C BUS type) serial EEPROMs which are electrically programmable.

∗I²C BUS is a registered trademark of Philips.

●Features

1) 1k x 8 bits serial EEPROM.
   (BR24C08 / F / FJ / FV)
   2k x 8 bits serial EEPROM.
   (BR24C16 / F / FJ / FV, BR24E16 / F / FJ / FV)
2) Two wire serial interface.
   (2Byte Address : BR24E16)
3) Operating voltage range : 2.7V~5.5V
4) Low current consumption
   Active (at 5V) : 2.0mA (Typ.)
   Standby (at 5V) : 1.0μA (Typ.)
5) Auto erase and auto complete functions can be used during write operations.
6) Page write function : 16byte
7) DATA security
   Write protect feature
   Inhibit to WRITE at low Vcc
8) Noise filters at SCL and SDA pins.
9) Address can be incremented automatically during read operations.
10) Compact packages.
11) Rewriting possible up to 100,000 times.
12) Data can be stored for ten years without corruption.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	–0.3~+6.5	V
Power dissipation	Pd	300(SSOP–B8) ∗1	mW
		450(SOP8, SOP–J8) ∗2	
		800(DIP8) ∗3	
Storage temperature range	Tstg	–65~+125	°C
Operating temperature range	Topr	–40~+85	°C
Terminal voltage	–	–0.3~V_{CC}+0.3	V

∗1 Reduced by 3.0mW for each increase in Ta of 1°C over 25°C.
∗2 Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.
∗3 Reduced by 5.0mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	2.7~5.5	V
Input voltage	V_{IN}	0~V_{CC}	V

●Block diagram

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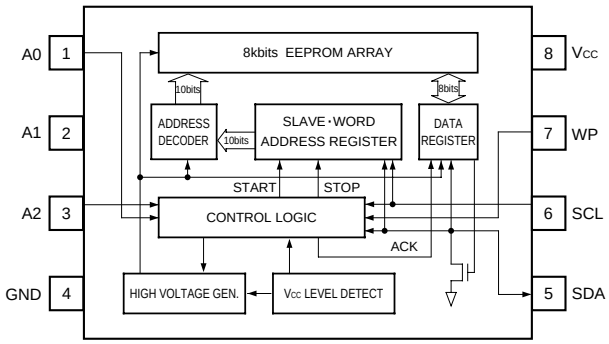

Pin name	I / O	Function
Vcc	–	Power supply
GND	–	Ground (0V)
A0, A1	–	Out of use. Please connect to GND.
A2	I	Slave address set
SCL	I	Serial clock input
SDA	I / O	Slave and word address, serial data input, serial data output *
WP	I	Wite protect pin

*An open drain output requires a pull-up resistor.

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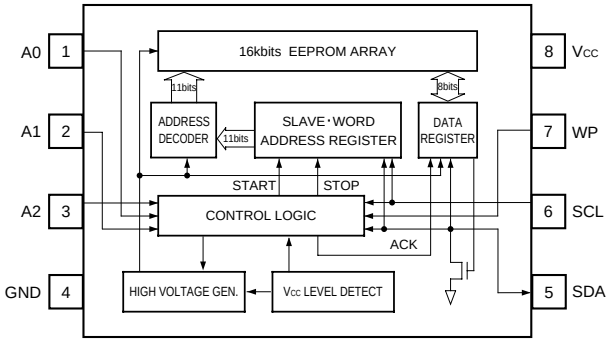

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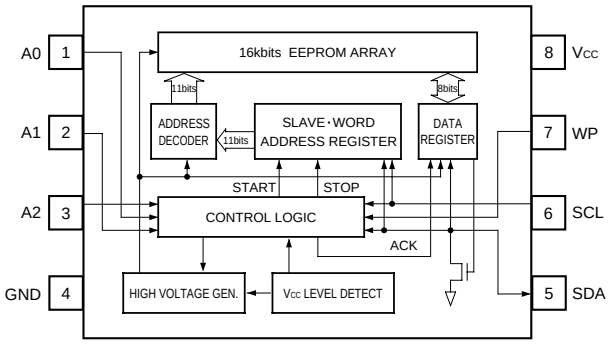
BR24E16 / F / FJ / FV



Pin name	I / O	Function
Vcc	–	Power supply
GND	–	Ground (0V)
A0, A1, A2	I	Slave address set
SCL	I	Serial clock input
SDA	I / O	Slave and word address, serial data input, serial data output *
WP	I	Wite protect pin

*An open drain output requires a pull-up resistor.

●Electrical characteristics

DC characteristics (Unless otherwise noted, Ta=–40~85°C, V_{CC}=2.7~5.5V)

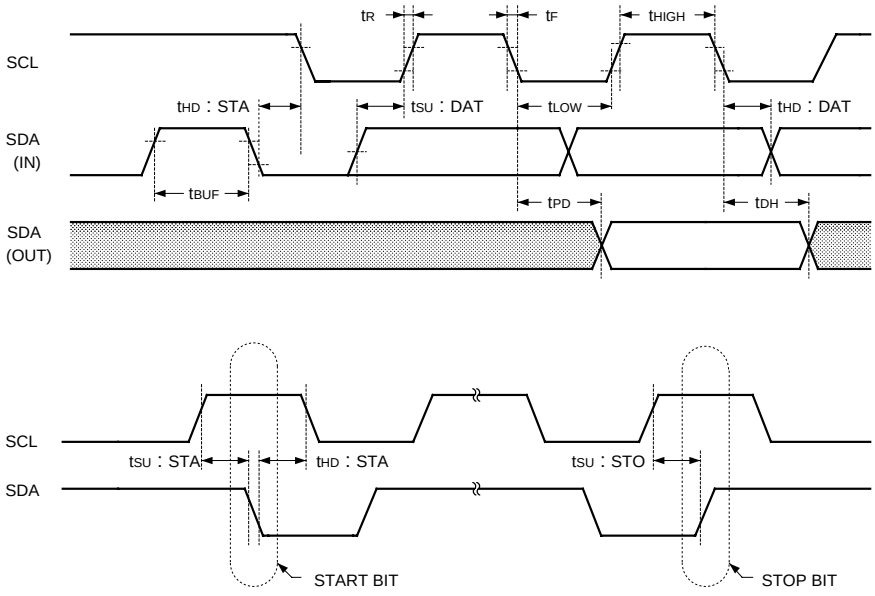
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
"HIGH" input voltage	V_{IH}	0.7V_{CC}	–	–	V	–
"LOW" input voltage	V_{IL}	–	–	0.3V_{CC}	V	–
"LOW" output voltage	V_{OL}	–	–	0.4	V	I_{OL}=3.0mA(SDA)
Input leakage current	I_{LI}	–1	–	1	µA	V_{IN}=0V~V_{CC}
Output leakage current	I_{LO}	–1	–	1	µA	V_{OUT}=0V~V_{CC}
operating current	I_{CC}	–	–	3.0	mA	V_{CC}=5.5V, f_{SCL}=400kHz
Standby current	I_{SB}	–	–	3.0	µA	V_{CC}=5.5V, SDA・SCL=V_{CC} A0, A1, A2=GND, WP=GND

◎ This product is not designed for protection against radioactive rays.

Operating timing characteristics (Unless otherwise noted, Ta=–40~85°C, V_{CC}=2.7~5.5V)

Parameter	Symbol	Vcc=5V±10%			Vcc=3V±10%			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL frequency	f_{SCL}	–	–	400	–	–	100	kHz
Dataclock "HIGH" time	t_{HIGH}	0.6	–	–	4.0	–	–	µs
Dataclock "LOW" time	t_{LOW}	1.2	–	–	4.7	–	–	µs
SDA / SCL rise time	t_R	–	–	0.3	–	–	1.0	µs
SDA / SCL fall time	t_F	–	–	0.3	–	–	0.3	µs
Start condition hold time	t_{HD} : STA	0.6	–	–	4.0	–	–	µs
Start condition setup time	t_{SU} : STA	0.6	–	–	4.7	–	–	µs
Input data hold time	t_{HD} : DAT	0	–	–	0	–	–	ns
Input data setup time	t_{SU} : DAT	100	–	–	250	–	–	ns
Output data delay time	t_{PD}	0.1	–	0.9	0.2	–	3.5	µs
Output data hold time	t_{DH}	0.1	–	–	0.2	–	–	µs
Stop condition setup time	t_{SU} : STO	0.6	–	–	4.7	–	–	µs
Bus open time before start or transfer	t_{BUF}	1.2	–	–	4.7	–	–	µs
Internal write cycle time	t_{WR}	–	–	10	–	–	10	ms
Noise erase valid time (SDA/SCL pins)	t_I	–	–	0.05	–	–	0.1	µs

●Timing charts



- Data is read on the rising edge of SCL.
- Data is output in synchronization with the falling edge of SCL.

Fig.1 Synchronized data input / output timing

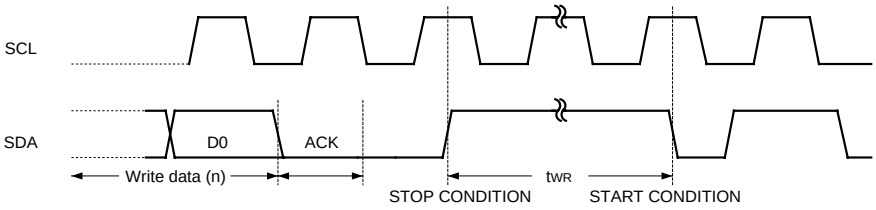


Fig.2 Write cycle timing

●Circuit operation

(1) Start condition (recognition of start bit)

Before executing any command, when SCL is HIGH, a start condition (start bit) is required to cause SDA to fall from HIGH to LOW. This IC is designed to constantly detect whether there is a start condition (start bit) for the SDA and SCL line, and no commands will be executed unless this condition is satisfied.
(See Fig.1 for the synchronized data input / output timing.)

(2) Stop condition (recognition of stop bit)

To stop any command, a stop condition (stop bit) is required. A stop condition is achieved when SDA goes from LOW to HIGH while SCL is HIGH. This enables commands to be completed.
(See Fig.1 for the synchronized data input / output timing.)

(3) Precautions concerning write commands

In the WRITE mode, the transferred data is not written to the memory unless the stop bit is executed.

(4) Device addressing

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1) Make sure the slave address is output from the master in continuation with the start condition.
2) The upper 4bits of the slave address are used to determine the device type. The device code for this IC is fixed at "1010".
3) The next 1bit of the slave address (A2 … device address) are used to select the device. This IC can address up to two devices on the same bus.
4) The next 2bits (P1, P0 … page select) are used by the master to select four 256 word page of memory.
   P1, P0 set to '0' '0' ····· 1 page (000 ~0FF)
   P1, P0 set to '0' '1' ····· 2 page (100 ~1FF)
   P1, P0 set to '1' '0' ····· 3 page (200 ~2FF)
   P1, P0 set to '1' '1' ····· 4 page (300 ~3FF)
5) The lowermost bit of the slave address (R / $\overline{W}$ … READ / $\overline{WRITE}$) is used to set the write or read mode as follows.
   R / $\overline{W}$ set to 0 … Write
   (Random read word address setting is also 0)
   R / $\overline{W}$ set to 1 … Read

1010	A2	P1	P0	R / $\overline{W}$

BR24C16 / F / FJ / FV

1) Make sure the slave address is output from the master in continuation with the start condition.
2) The upper 4bits of the slave address are used to determine the device type. The device code for this IC is fixed at "1010".
3) The next 3bits (P2, P1, P0 … page select) are used by the master to select four 256 word page of memory.
   P2, P1, P0 set to '0' '0' '0'····· 1 page (000 ~0FF)
   P2, P1, P0 set to '0' '0' '1'····· 2 page (100 ~1FF)
   : :
   P2, P1, P0 set to '1' '1' '1'····· 8 page (700 ~7FF)
4) The lowermost bit of the slave address (R / $\overline{W}$ … READ / $\overline{WRITE}$) is used to set the write or read mode as follows.
   R / $\overline{W}$ set to 0 … Write
   (Random read word address setting is also 0)
   R / $\overline{W}$ set to 1 … Read

1010	P2	P1	P0	R / $\overline{W}$

BR24E16 / F / FJ / FV

1) Make sure the slave address is output from the master in continuation with the start condition.
2) The upper 4bits of the slave address are used to determine the device type. The device code for this IC is fixed at "1010".
3) The next 3bits of the slave address (A2, A1, A0 … device address) are used to select the device. This IC can address up to eight devices on the same bus.
4) The lowermost bit of the slave address (R / $\overline{W}$ … READ / $\overline{WRITE}$) is used to set the write or read mode as follows.
   R / $\overline{W}$ set to 0 … Write
   (Random read word address setting is also 0)
   R / $\overline{W}$ set to 1 … Read

1010	A2	A1	A0	R / $\overline{W}$

(5) Write protect (WP)

When WP pin set to V_{CC} (High level), write protect is set by all address. When WP pin set to GND (Low level), enable to write to all address. Either control this pin or connect to GND (or V_{CC}). It is inhibited from being left unconnected.

(6) ACK signal

The acknowledge signal (ACK signal) is determined by software and is used to indicate whether or not a data transfer is proceeding normally. The transmitting device, whether the master or slave, opens the bus after an 8-bit data output (μ-COM when a write or read command of the slave address input ; this IC when reading data).

For the receiving device during the ninth clock cycle, SDA is set to LOW and an acknowledge signal (ACK signal) is sent to indicate that it received the 8-bit data (this IC when a write command or a read command of the slave address input, μ-COM when a read command data output).

The ICs output a LOW acknowledge signal (ACK signal) after recognizing the start condition and slave address (8 bits).

When data is being write to the ICs, a LOW acknowledge signal (ACK signal) is output after the receipt of each 8 bits of data (word address and write data).

When data is being read from the IC, 8bits of data (read data) are output and the IC waits for a returned LOW acknowledge signal (ACK signal). When an acknowledge signal (ACK signal) is detected and a stop condition is not sent from the master (μ-COM) side, the IC continues to output data. If an acknowledge signal (ACK signal) is not detected, the IC interrupts the data transfer and ceases reading operations after recognizing the stop condition (stop bit). The IC then enters the waiting or standby state.

(See Fig.3 for acknowledge signal (ACK signal) response.)

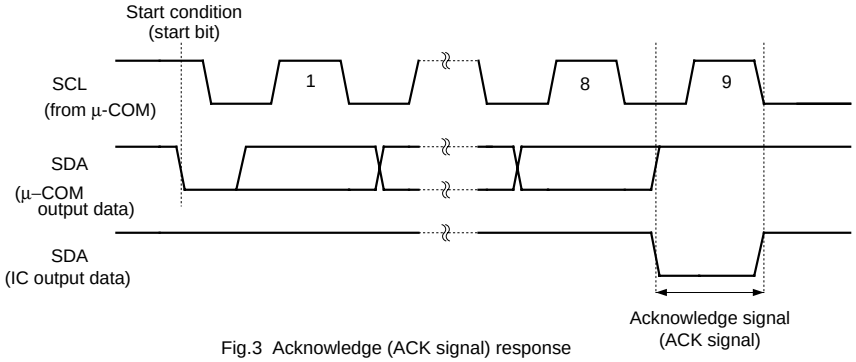

Fig.3 Acknowledge (ACK signal) response
(during write and read slave address input)

(7) Byte write

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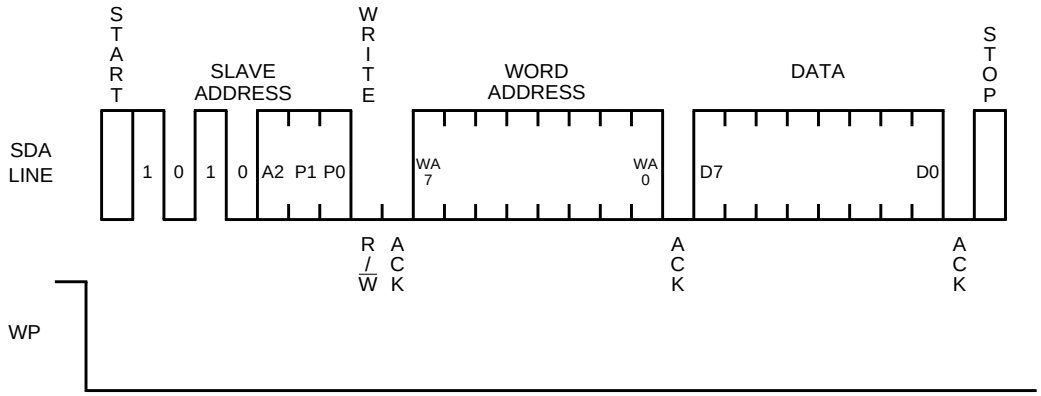

Fig.4

BR24C16 / F / FJ / FV

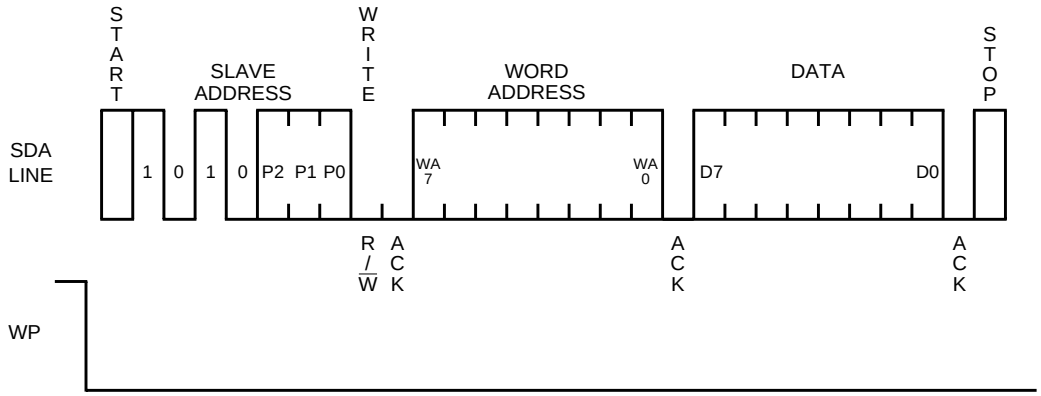

Fig.5

BR24E16 / F / FJ / FV

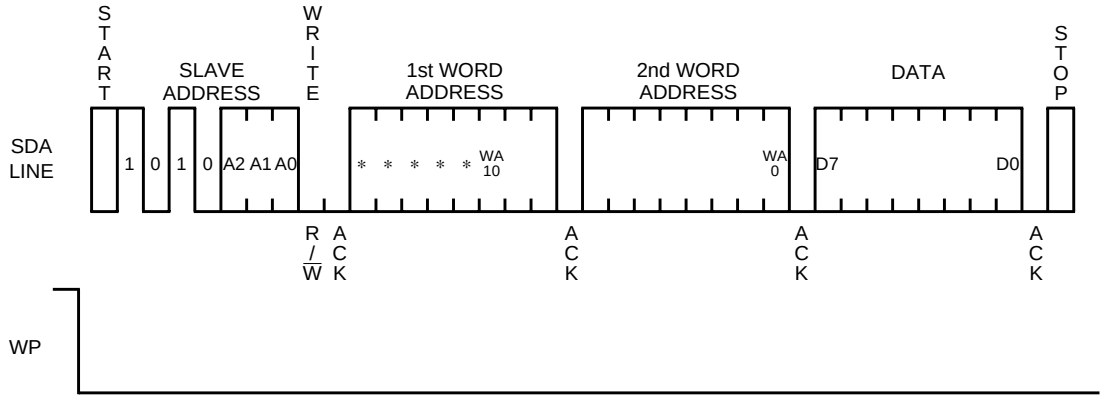

Fig.6

- Data is written to the address designated by the word address (n address).
- After 8 bits of data are input, the data is written to the memory cell by issuing the stop bit.

(8) Page write

BR24C08 / F / FJ / FV

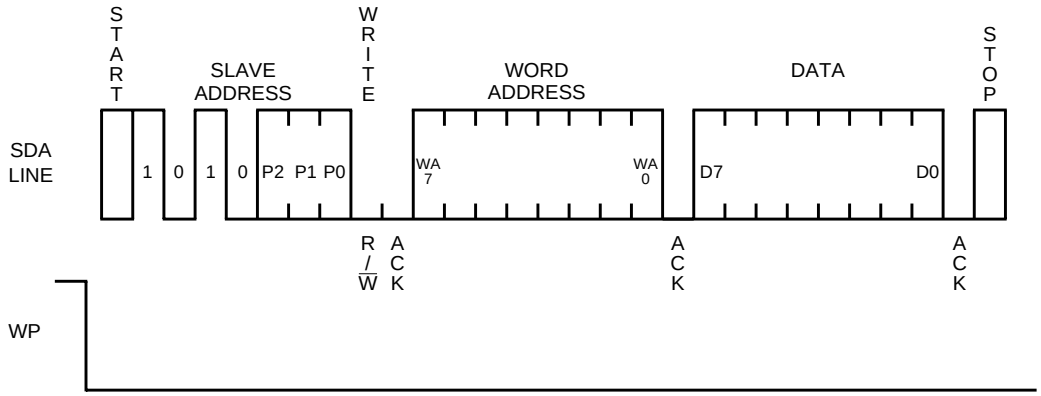

Fig.7

BR24C16 / F / FJ / FV

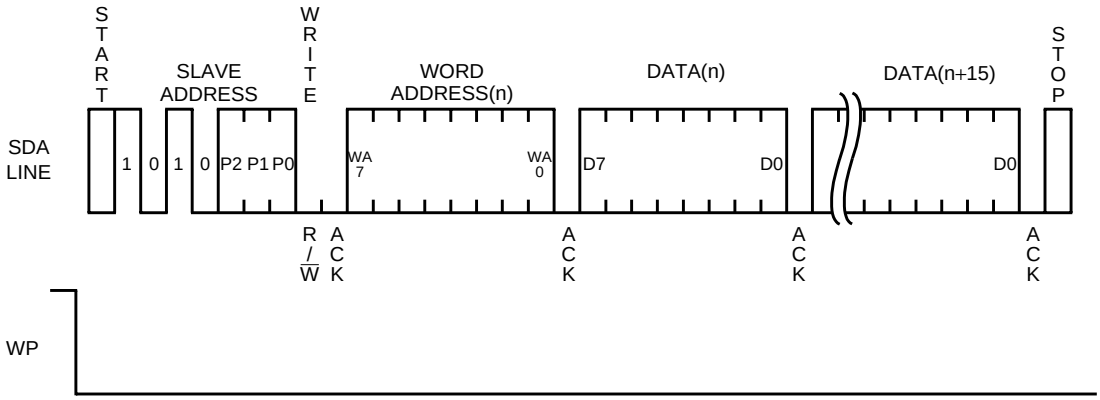

Fig.8

BR24E16 / F / FJ / FV

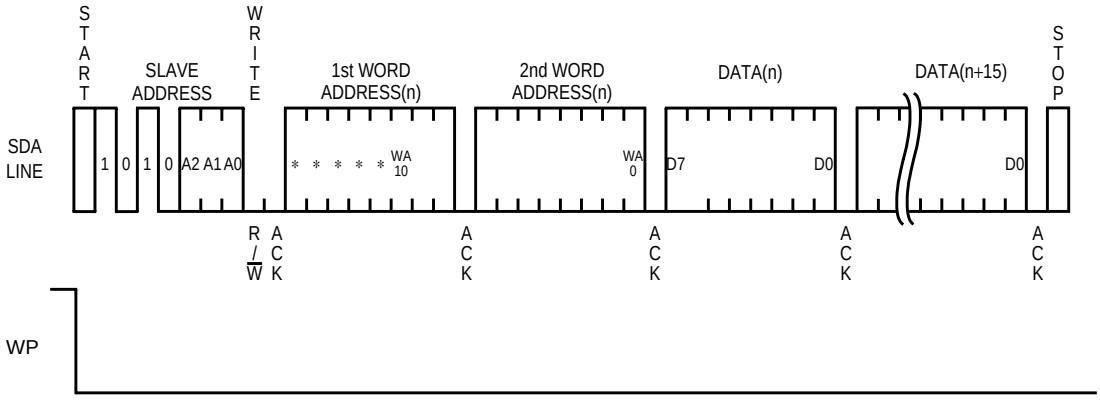

Fig.9

- A 16 byte write is possible using this command.
- The page write command arbitrarily sets the upper 4 bits (WA7 to WA4) of the word address.
  The lower 4 bits (WA3 and WA0) can write up to 16 bytes of data with the address being incremented internally.

(9) Current read

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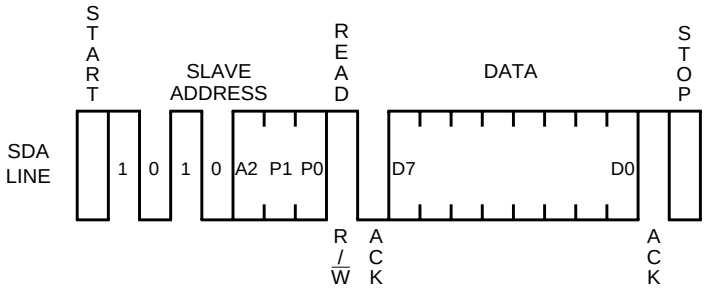

Fig.10

BR24C16 / F / FJ / FV

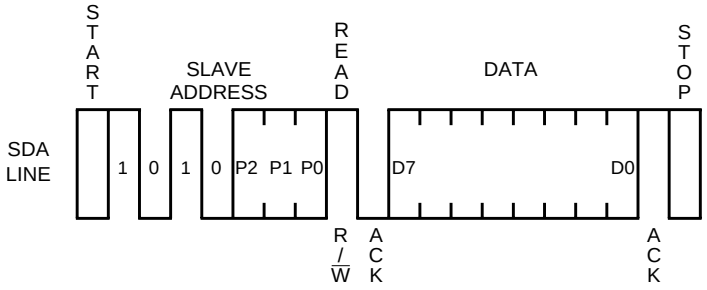

Fig.11

BR24E16 / F / FJ / FV

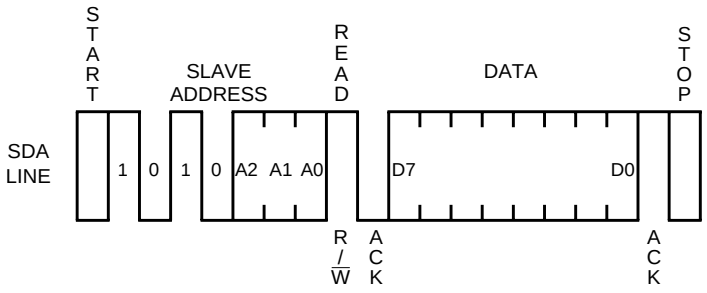

Fig.12

- In case the previous operation is random or current read (which includes sequential read respectively), the internal address counter is increased by one from the last accessed address (n). Thus current read outputs the data of the next word address (n+1).
  If the last command is byte or page write, the internal address counter stays at the last address (n). Thus current read outputs the data of the word address (n).
  If the master does not transfer the acknowledge but does generate a stop condition, the current address read operation only provides s single byte of data.
  At this point, this IC discontinues transmission.
- When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. [All words all read enabled]
  (See Fig.16 to 18 for the sequential read cycles.)
- This command is ended by inputting HIGH to the ACK signal after D0 and raising the SDA signal (stop condition) by setting SCL to HIGH.

(10) Random read

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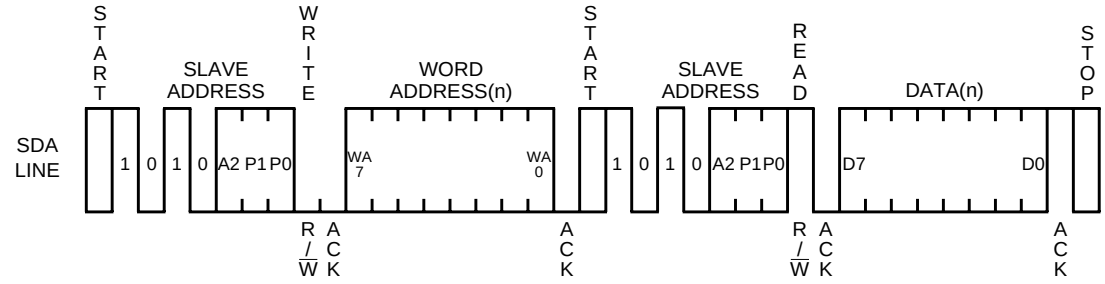


Fig.13

BR24C16 / F / FJ / FV

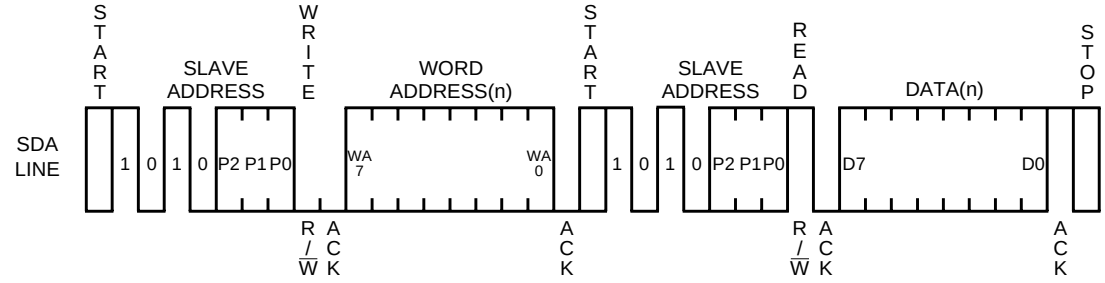


Fig.14

BR24E16 / F / FJ / FV

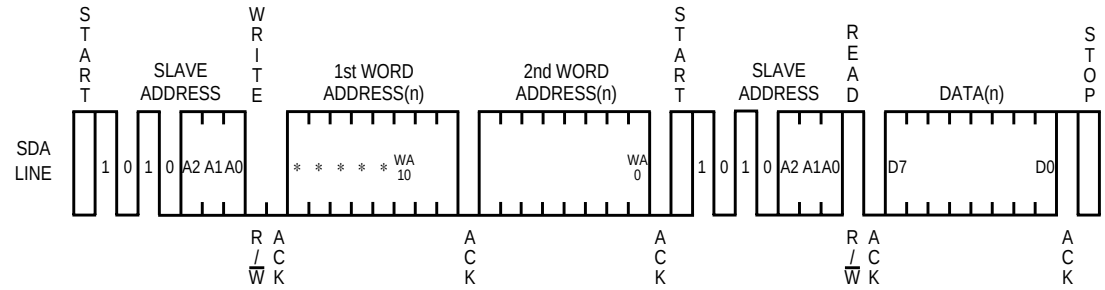


Fig.15

- This command can read the designated word address data.
- When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. [All words all read enabled]
  (See Fig.16 to 18 for the sequential read cycles.)
- This command is ended by inputting a HIGH signal to the ACK signal after D0 and raising the SDA signal (stop condition) by raising SCL to HIGH.

(11) Sequential read

BR24C08 / F / FJ / FV

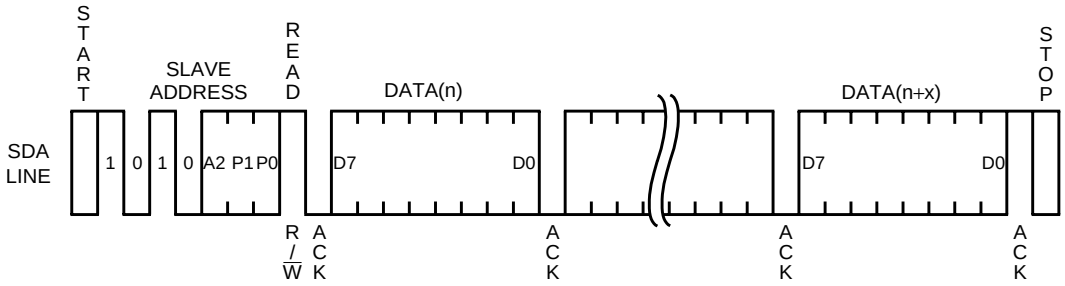


Fig.16

BR24C16 / F / FJ / FV

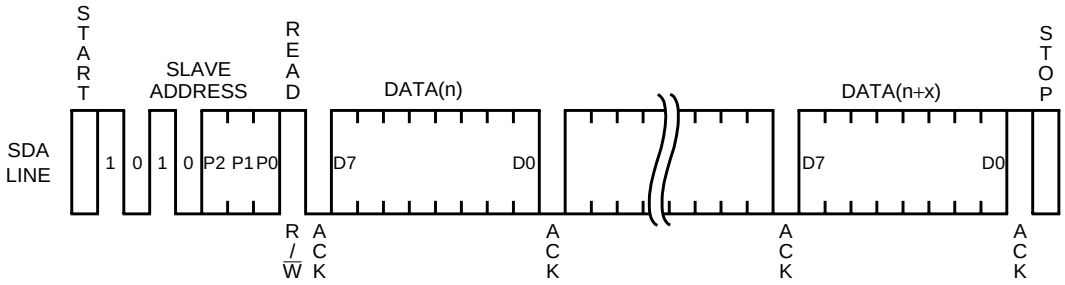


Fig.17

BR24E16 / F / FJ / FV

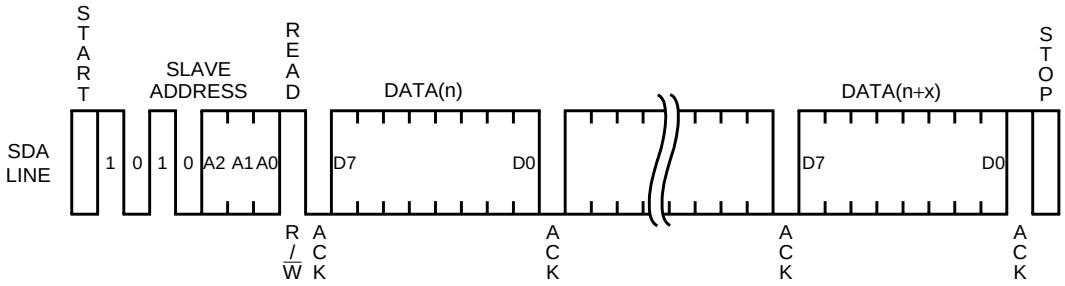
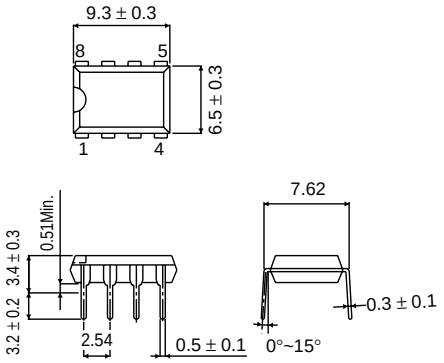


Fig.18

- When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master (μ-COM), the next word address data can be read. [All words can be read]
- This command is ended by inputting a HIGH signal to the ACK signal after D0 and raising the SDA signal (stop condition) using the SCL signal HIGH.
- Sequential reading can also be done with a random read.

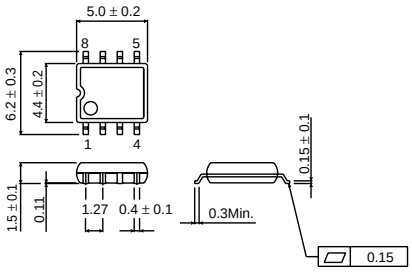
●**External dimensions** (Units : mm)

BR24C08
BR24C16
BR24E16



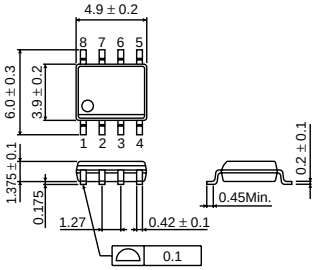
DIP8

BR24C08F
BR24C16F
BR24E16F



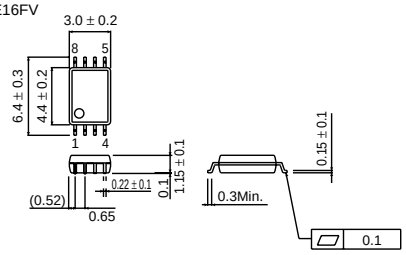
SOP8

BR24C08FJ
BR24C16FJ
BR24E16FJ



SOP-J8

BR24C08FV
BR24C16FV
BR24E16FV



SSOP-B8