TDA6650ATT; TDA6651ATT

5 V mixer/oscillator and low noise PLL synthesizer for hybrid terrestrial tuner (digital and analog)

Rev. 02 — 2 February 2007 Product data sheet

1. General description

The TDA6650ATT; TDA6651ATT is a programmable 3-band mixer/oscillator and low phase noise PLL synthesizer intended for pure 3-band tuner concepts applied to hybrid (digital and analog) or digital-only terrestrial and cable TV reception.

Table 1. Different versions are available, depending on the target application[1]

Application	Type version
Analog and digital (Hybrid ISDB-T/NTSC Japan)	TDA6650ATT/C3
	TDA6651ATT/C3
Digital only (ISDB-T)	TDA6650ATT/C3/S2
	TDA6651ATT/C3/S2
	TDA6651ATT/C3/S3

[1] See Table 20 “Characteristics” for differences between TDA6651ATT/C3/S2 and TDA6651ATT/C3/S3.

The device includes three double balanced mixers for low, mid and high bands, three oscillators for the corresponding bands, a switchable IF amplifier, a wideband AGC detector and a low noise PLL synthesizer. The frequencies of the three bands are shown in Table 2. Two pins are available between the mixer output and the IF amplifier input to enable IF filtering for improved signal handling and to improve the adjacent channel rejection.

Table 2. Recommended band limits

Band	RF input		Oscillator	
	Min (MHz)	Max (MHz)	Min (MHz)	Max (MHz)
ISDB-T and NTSC Japan hybrid tuners[1]				
Low	91.25	217.25	150	276
Mid	217.25	463.25	276	522
High	463.25	765.25	522	824
ISDB-T tuners for digital-only application[2]				
Low	93.00	219.00	150	276
Mid	219.00	465.00	276	522
High	465.00	767.00	522	824

[1] RF input frequency is the frequency of the corresponding picture carrier for analog standard.

[2] For bandwidth optimization please refer to *Application note AN01014*.

The IF amplifier is switchable in order to drive both symmetrical and asymmetrical outputs. When it is used as an asymmetrical amplifier, the IFOUTB pin needs to be connected to the supply voltage V_{CCA}.

Five open-drain PMOS ports are included on the IC. Two of them, BS1 and BS2, are also dedicated to the selection of the low, mid and high bands. PMOS port BS5 pin is shared with the ADC.

The AGC detector provides a control that can be used in a tuner to set the gain of the RF stage. Six AGC take-over points are available by software. Two programmable AGC time constants are available for search tuning and normal tuner operation.

The local oscillator signal is fed to the fractional-N divider. The divided frequency is compared to the comparison frequency into the fast phase detector which drives the charge pump. The loop amplifier is also on-chip, including the high-voltage transistor to drive directly the 33 V tuning voltage without the need to add an external transistor.

The comparison frequency is obtained from an on-chip crystal oscillator. The crystal frequency can be output to the XTOUT pin to drive the clock input of a digital demodulation IC.

Control data is entered via the I^2C-bus; six serial bytes are required to address the device, select the Local Oscillator (LO) frequency, select the step frequency, program the output ports and set the charge pump current or enable or disable the crystal output buffer, select the AGC take-over point and time constant and/or select a specific test mode. A status byte concerning the AGC level detector and the ADC voltage can be read out on the SDA line during a read operation. During a read operation, the loop ‘in-lock’ flag, the power-on reset flag and the automatic loop bandwidth control flag are read.

The device has 4 programmable addresses. Each address can be selected by applying a specific voltage to pin AS, enabling the use of multiple devices in the same system.

The I^2C-bus is fast mode compatible, except for the timing as described in the functional description and is compatible with 5 V, 3.3 V and 2.5 V microcontrollers depending on the voltage applied to pin BVS.

2. Features

- Single-chip 5 V mixer/oscillator and low phase noise PLL synthesizer for TV and VCR tuners, dedicated to hybrid (digital and analog) and pure digital applications for Japanese standards (NTSC and ISDB-T)
- Five possible step frequencies to cope with different digital terrestrial TV and analog TV standards
- Eight charge pump currents between 40 µA and 600 µA to reach the optimum phase noise performance over the bands
- I^2C-bus protocol compatible with 2.5 V, 3.3 V and 5 V microcontrollers:
  - Address + 5 data bytes transmission (I^2C-bus write mode)
  - Address + 1 status byte (I^2C-bus read mode)
  - Four independent I^2C-bus addresses
- Five PMOS open-drain ports with 15 mA source capability for band switching and general purpose; one of these ports is combined with a 5-step ADC
- Wideband AGC detector for internal tuner AGC:
  - Six programmable take-over points
  - Two programmable time constants
  - AGC flag

- In-lock flag
- Crystal frequency output buffer
- 33 V tuning voltage output
- Fractional-N programmable divider
- Balanced mixers with a common emitter input for the low band and for the mid band (each single input)
- Balanced mixer with a common base input for the high band (balanced input)
- 2-pin asymmetrical oscillator for the low band
- 2-pin symmetrical oscillator for the mid band
- 4-pin symmetrical oscillator for the high band
- Switched concept IF amplifier with both asymmetrical and symmetrical outputs to drive low impedance or SAW filters i.e. 500 Ω/40 pF

3. Applications

For all applications, the recommendations given in the latest *Application note AN10544* **must** be used.

3.1 Application summary

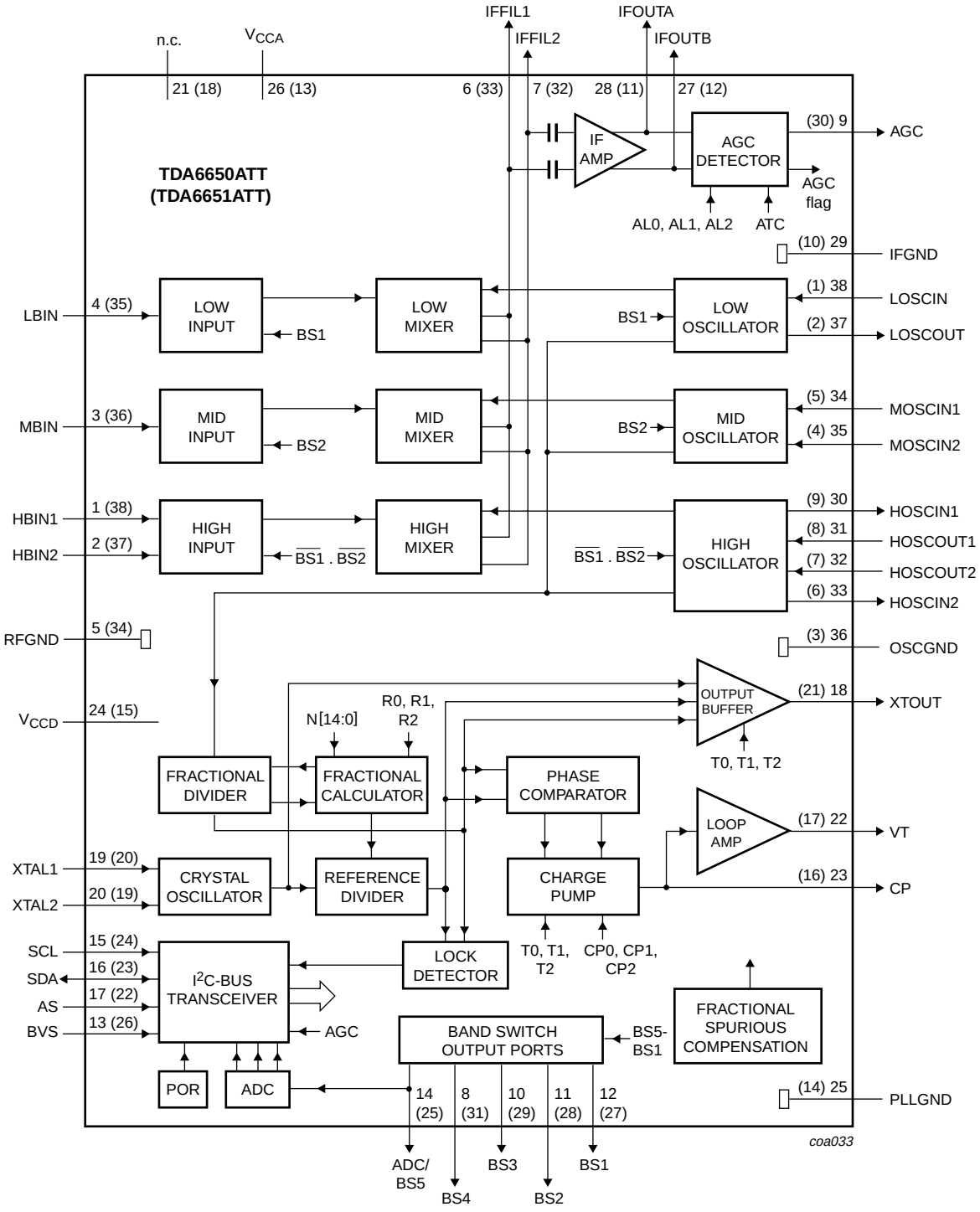
- Digital and analog terrestrial tuners (ISDB-T and NTSC Japan)
- Cable tuners (QAM)
- Digital TV sets
- Digital set-top boxes

4. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
TDA6650ATT/C3	TSSOP38	plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm	SOT510-1
TDA6650ATT/C3/S2			
TDA6651ATT/C3			
TDA6651ATT/C3/S2			
TDA6651ATT/C3/S3			

5. Block diagram



The pin numbers in parenthesis represent the TDA6651ATT.

Fig 1. Block diagram

6. Pinning information

6.1 Pin description

Table 4. Pin description

Symbol	Pin		Description
	TDA6650ATT	TDA6651ATT	
HBIN1	1	38	high band RF input 1
HBIN2	2	37	high band RF input 2
MBIN	3	36	mid band RF input
LBIN	4	35	low band RF input
RFGND	5	34	RF ground
IFFIL1	6	33	IF filter output 1
IFFIL2	7	32	IF filter output 2
BS4	8	31	PMOS open-drain output port 4 for general purpose
AGC	9	30	AGC output
BS3	10	29	PMOS open-drain output port 3 for general purpose
BS2	11	28	PMOS open-drain output port 2 to select the mid band
BS1	12	27	PMOS open-drain output port 1 to select the low band
BVS	13	26	bus voltage selection input
ADC/BS5	14	25	ADC input or PMOS open-drain output port 5 for general purpose
SCL	15	24	I^2C-bus serial clock input
SDA	16	23	I^2C-bus serial data input and output
AS	17	22	I^2C-bus address selection input
XTOUT	18	21	crystal frequency buffer output
XTAL1	19	20	crystal oscillator input 1
XTAL2	20	19	crystal oscillator input 2
n.c.	21	18	not connected
VT	22	17	tuning voltage output
CP	23	16	charge pump output
V_{CCD}	24	15	supply voltage for the PLL part
PLLGND	25	14	PLL ground
V_{CCA}	26	13	supply voltage for the analog part
IFOUTB	27	12	IF output B for symmetrical amplifier and asymmetrical IF amplifier switch input
IFOUTA	28	11	IF output A
IFGND	29	10	IF ground
HOSCIN1	30	9	high band oscillator input 1
HOSCOUT1	31	8	high band oscillator output 1
HOSCOUT2	32	7	high band oscillator output 2

Table 4. Pin description *...continued*

Symbol	Pin		Description
	TDA6650ATT	TDA6651ATT	
HOSCIN2	33	6	high band oscillator input 2
MOSCIN1	34	5	mid band oscillator input 1
MOSCIN2	35	4	mid band oscillator input 2
OSCGND	36	3	oscillators ground
LOSCOUT	37	2	low band oscillator output
LOSCIN	38	1	low band oscillator input

6.2 Pinning

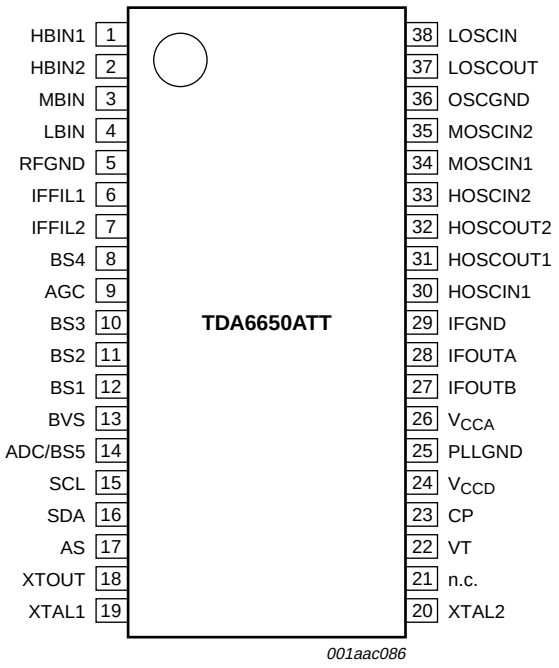


Fig 2. Pin configuration TDA6650ATT

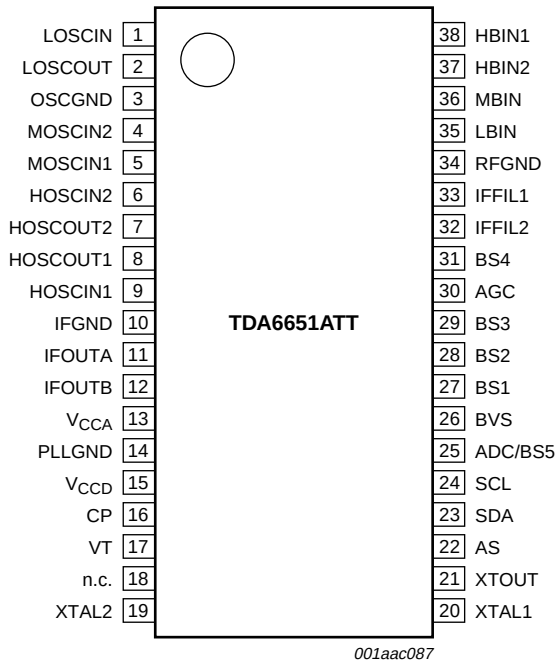


Fig 3. Pin configuration TDA6651ATT

7. Functional description

7.1 Mixer, Oscillator and PLL (MOPLL) functions

Bit BS1 enables the BS1 port, the low band mixer and the low band oscillator. Bit BS2 enables the BS2 port, the mid band mixer and the mid band oscillator. When both BS1 and BS2 bits are logic 0, the high band mixer and the high band oscillator are enabled.

The oscillator signal is applied to the fractional-N programmable divider. The divided signal f_{div} is fed to the phase comparator where it is compared in both phase and frequency with the comparison frequency f_{comp}. This frequency is derived from the signal present on the crystal oscillator f_{xtal} and divided in the reference divider. There is a fractional calculator on the chip that generates the data for the fractional divider as well as

the reference divider ratio, depending on the step frequency selected. The crystal oscillator requires a 4 MHz crystal in series with an 18 pF capacitor between pins XTAL1 and XTAL2.

The output of the phase comparator drives the charge pump and the loop amplifier section. This amplifier has an on-chip high voltage drive transistor. Pin CP is the output of the charge pump, and pin VT is the pin to drive the tuning voltage to the varicap diodes of the oscillators and the tracking filters. The loop filter has to be connected between pins CP and VT. The spurious signals introduced by the fractional divider are automatically compensated by the spurious compensation block.

It is possible to drive the clock input of a digital demodulation IC from pin XTOUT with the 4 MHz signal from the crystal oscillator. This output is also used to output $\frac{1}{2}f_{div}$ and f_{comp} signals in a specific test mode (see Table 9). It is possible to switch off this output, which is recommended when it is not used.

For test and alignment purposes, it is also possible to release the tuning voltage output by selecting the sinking mode (see Table 9), and by applying an external voltage on pin VT.

In addition to the BS1 and BS2 output ports that are used for the band selection, there are three general purpose ports BS3, BS4 and BS5. All five ports are PMOS open-drain type, each with 15 mA drive capability. The connection for port BS5 and the ADC input is combined on one pin. It is not possible to use the ADC if port BS5 is used.

The AGC detector compares the level at the IF amplifier output to a reference level which is selected from 6 different levels via the I^{2}C-bus. The time constant of the AGC can be selected via the I^{2}C-bus to cope with normal operation as well as with search operation.

When the output level on pin AGC is higher than the threshold V_{RMH}, then bit AGC = 1. When the output level on pin AGC is lower than the threshold V_{RML}, then bit AGC = 0. Between these two thresholds, bit AGC is not defined. The status of the AGC bit can be read via the I^{2}C-bus according to the read mode as described in Table 13.

7.2 I^{2}C-bus voltage

The I^{2}C-bus lines SCL and SDA can be connected to an I^{2}C-bus system tied to 2.5 V, 3.3 V or 5 V. The choice of the bus input threshold voltages is made with pin BVS that can be left open-circuit, connected to the supply voltage or to ground (see Table 5).

Table 5. I^{2}C-bus voltage selection

Pin BVS connection	Bus voltage	Logic level	
		LOW	HIGH
To ground	2.5 V	0 V to 0.75 V	1.75 V to 5.5 V
Open-circuit	3.3 V	0 V to 1.0 V	2.3 V to 5.5 V
To V_{CC}	5 V	0 V to 1.5 V	3.0 V to 5.5 V

7.3 Phase noise, I^{2}C-bus traffic and crosstalk

While the TDA6650ATT; TDA6651ATT is dedicated for hybrid terrestrial applications, the low noise PLL will clean up the noise spectrum of the VCOs close to the carrier to reach noise levels at 1 kHz offset from the carrier compatible with e.g. ISDB-T reception.

Linked to this noise improvement, some disturbances may become visible while they were not visible because they were hidden into the noise in analog dedicated applications and circuits.

This is especially true for disturbances coming from the I²C-bus traffic, whatever this traffic is intended for the MOPLL or for another slave on the bus.

To avoid this I²C-bus crosstalk and be able to have a clean noise spectrum, it is necessary to use a bus gate that enables the signal on the bus to drive the MOPLL only when the communication is intended for the tuner part (such a kind of I²C-bus gate is included into the NXP terrestrial channel decoders), and to avoid unnecessary repeated sending of the same information.

8. I²C-bus protocol

The TDA6650ATT; TDA6651ATT is controlled via the two-wire I²C-bus. For programming, there is one device address (7 bits) and the R/$\overline{W}$ bit for selecting read or write mode. To be able to have more than one MOPLL in an I²C-bus system, one of four possible addresses is selected depending on the voltage applied to address selection pin AS (see Table 8).

The TDA6650ATT; TDA6651ATT fulfils the fast mode I²C-bus, according to the NXP I²C-bus specification, except for the timing as described in Figure 4. The I²C-bus interface is designed in such a way that the pins SCL and SDA can be connected to 5 V, 3.3 V or to 2.5 V pulled-up I²C-bus lines, depending on the voltage applied to pin BVS (see Table 5).

8.1 Write mode; R/$\overline{W}$ = 0

After the address transmission (first byte), data bytes can be sent to the device (see Table 6). Five data bytes are needed to fully program the TDA6650ATT; TDA6651ATT. The I²C-bus transceiver has an auto-increment facility that permits programming the device within one single transmission (address + 5 data bytes).

The TDA6650ATT; TDA6651ATT can also be partly programmed on the condition that the first data byte following the address is byte 2 (divider byte 1) or byte 4 (control byte 1). The first bit of the first data byte transmitted indicates whether byte 2 (first bit = 0) or byte 4 (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. The fractional calculator is updated only at the end of the transmission (STOP condition). Each control byte is loaded after the 8th clock pulse of the corresponding control byte. Main divider data are valid only if no new I²C-bus transmission is started (START condition) during the computation period of 50 µs.

Both DB1 and DB2 need to be sent to change the main divider ratio. If the value of the ratio selection bits R2, R1 and R0 are changed, the bytes DB1 and DB2 have to be sent in the same transmission.

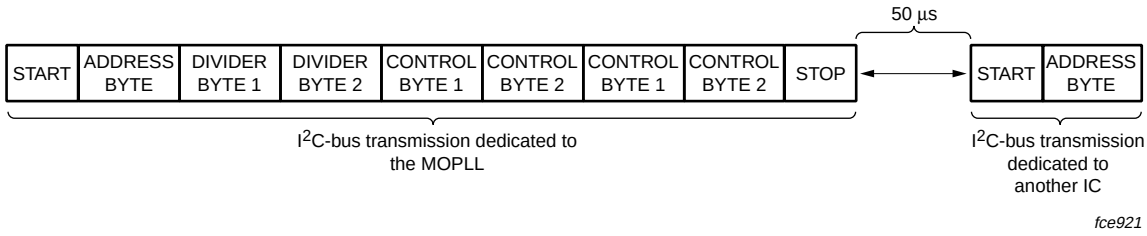


Fig 4. Example of I²C-bus transmission frame

Table 6. I²C-bus write data format

Name	Byte	Bit								Ack
		MSB[1]							LSB	
Address byte	1	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 0	A
Divider byte 1 (DB1)	2	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	3	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte 1 (CB1); see Table 7	4	1	T/A = 1	T2	T1	T0	R2	R1	R0	A
		1	T/A = 0	0	0	ATC	AL2	AL1	AL0	A
Control byte 2 (CB2)	5	CP2	CP1	CP0	BS5	BS4	BS3	BS2	BS1	A

[1] MSB is transmitted first.

Table 7. Description of write data format bits

Bit	Description
A	acknowledge
MA1 and MA0	programmable address bits; see Table 8
R/$\overline{W}$	logic 0 for write mode
N14 to N0	programmable LO frequency; $N = N14 \times 2^{14} + N13 \times 2^{13} + N12 \times 2^{12} + ... + N1 \times 2^{1} + N0$
T/A	test/AGC bit
	T/A = 0: the next 6 bits sent are AGC settings
	T/A = 1: the next 6 bits sent are test and reference divider ratio settings
T2, T1 and T0	test bits; see Table 9
R2, R1, and R0	reference divider ratio and programmable frequency step; see Table 10
ATC	AGC current setting and time constant; capacitor on pin AGC = 150 nF
	ATC = 0: AGC current = 220 nA; AGC time constant = 2 s
	ATC = 1: AGC current = 9 µA; AGC time constant = 50 ms
AL2, AL1 and AL0	AGC take-over point bits; see Table 11
CP2, CP1 and CP0	charge pump current; see Table 12
BS5, BS4, BS3, BS2 and BS1	PMOS ports control bits
	BSn = 0: corresponding port is off, high-impedance state (status at power-on reset)
	BSn = 1: corresponding port is on; $V_O = V_{CC} - V_{DS(sat)}$

8.1.1 I²C-bus address selection

The device address contains programmable address bits MA1 and MA0, which offer the possibility of having up to four MOPLL ICs in one system. Table 8 gives the relationship between the voltage applied to the AS input and the MA1 and MA0 bits.

Table 8. Address selection

Voltage applied to pin AS	MA1	MA0
0 V to $0.1V_{CC}$	0	0
$0.2V_{CC}$ to $0.3V_{CC}$ or open-circuit	0	1
$0.4V_{CC}$ to $0.6V_{CC}$	1	0
$0.9V_{CC}$ to V_{CC}	1	1

8.1.2 XTOUT output buffer and mode setting

The crystal frequency can be sent to pin XTOUT and used in the application, for example to drive the clock input of a digital demodulator, saving a quartz crystal in the bill of material. To output f_{xtal}, it is necessary to set T[2:0] to 001. If the output signal on this pin is not used, it is recommended to disable it, by setting T[2:0] to 000. This pin is also used to output $\frac{1}{2}f_{div}$ and f_{comp} in a test mode. At power-on, the XTOUT output buffer is set to on, supplying the f_{xtal} signal. The relation between the signal on pin XTOUT and the setting of the T[2:0] bits is given in Table 9.

Table 9. XTOUT buffer status and test modes

T2	T1	T0	Pin XTOUT	Mode
0	0	0	disabled	normal mode with XTOUT buffer off
0	0	1	f_{xtal} (4 MHz)	normal mode with XTOUT buffer on
0	1	0	$\frac{1}{2}f_{div}$	charge pump off
0	1	1	f_{xtal} (4 MHz)	not used[1]
1	0	0	f_{comp}	test mode
1	0	1	$\frac{1}{2}f_{div}$	test mode
1	1	0	f_{xtal} (4 MHz)	charge pump sinking current[2]
1	1	1	disabled	charge pump sourcing current

[1] This is an on-chip function that automatically sets internal values for the PLL. This function is not optimized for ISDB-T and NTSC Japan and therefore must not be used.

[2] This is the default mode at power-on reset. This mode disables the tuning voltage.

8.1.3 Step frequency setting

The step frequency is set by three bits, giving five steps to cope with different application requirements.

The reference divider ratio is automatically set depending on bits R2, R1 and R0. The phase detector works at either 4 MHz, 2 MHz or 1 MHz.

Table 10 shows the step frequencies and corresponding reference divider ratios. When the value of bits R2, R1 and R0 are changed, it is necessary to re-send the data bytes DB1 and DB2.

Table 10. Reference divider ratio select bits

R2	R1	R0	Reference divider ratio	Frequency comparison	Frequency step
0	0	0	2	2 MHz	62.5 kHz
0	0	1	1	4 MHz	142.86 kHz
0	1	0	1	4 MHz	166.67 kHz
0	1	1	4	1 MHz	50 kHz
1	0	0	1	4 MHz	125 kHz
1	0	1	-	-	reserved
1	1	0	-	-	reserved
1	1	1	-	-	reserved

8.1.4 AGC detector setting

The AGC take-over point can be selected out of 6 levels according to Table 11.

Table 11. AGC programming

AL2	AL1	AL0	Typical take-over point level
0	0	0	[1] 124 dBµV (p-p)
0	0	1	[1] 121 dBµV (p-p)
0	1	0	[1] 118 dBµV (p-p)
0	1	1	[2] 115 dBµV (p-p)
1	0	0	[2] 112 dBµV (p-p)
1	0	1	[2] 109 dBµV (p-p)
1	1	0	[3] I_{AGC} = 0 A
1	1	1	[4] V_{AGC} = 3.5 V

[1] This take-over point is available for both symmetrical and asymmetrical modes.

[2] This take-over point is available for asymmetrical mode only.

[3] The AGC current sources are disabled. The AGC output goes into a high-impedance state and an external AGC source can be connected in parallel and will not be influenced.

[4] The AGC detector is disabled and I_{AGC} = 9 µA.

8.1.5 Charge pump current setting

The charge pump current can be chosen from 8 values depending on the value of bits CP2, CP1 and CP0 bits; see Table 12.

Table 12. Charge pump current

CP2	CP1	CP0	Charge pump current number	Typical current (absolute value in µA)
0	0	0	1	38
0	0	1	2	54
0	1	0	3	83
0	1	1	4	122
1	0	0	5	163

Table 12. Charge pump current *...continued*

CP2	CP1	CP0	Charge pump current number	Typical current (absolute value in μA)
1	0	1	6	254
1	1	0	7	400
1	1	1	8	580

8.2 Read mode; R/$\overline{W}$ = 1

Data can be read from the device by setting the R/$\overline{W}$ bit to 1 (see Table 13). After the device address has been recognized, the device generates an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH level of the SCL clock signal.

A second data byte can be read from the device if the microcontroller generates an acknowledge on the SDA line (master acknowledge). End of transmission will occur if no master acknowledge occurs. The device will then release the data line to allow the microcontroller to generate a STOP condition.

Table 13. I²C-bus read data format

Name	Byte	Bit								Ack
		MSB[1]							LSB	
Address byte	1	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 1	A
Status byte	2	POR	FL	0	1	AGC	A2	A1	A0	-

[1] MSB is transmitted first.

Table 14. Description of read data format bits

Bit	Description
A	acknowledge
POR	power-on reset flag
	POR = 0, normal operation
	POR = 1, power-on reset
FL	in-lock flag
	FL = 0, not locked
	FL = 1, the PLL is locked
AGC	internal AGC flag
	AGC = 0 when internal AGC is active ($V_{AGC} < V_{RML}$)
	AGC = 1 when internal AGC is not active ($V_{AGC} > V_{RMH}$)
A2, A1, A0	digital outputs of the 5-level ADC; see Table 15

Table 15. ADC levels

Voltage applied to pin ADC[1]	A2	A1	A0
$0.6V_{CC}$ to V_{CC}	1	0	0
$0.45V_{CC}$ to $0.6V_{CC}$	0	1	1

Table 15. ADC levels *…continued*

Voltage applied to pin ADC[1]	A2	A1	A0
$0.3V_{CC}$ to $0.45V_{CC}$	0	1	0
$0.15V_{CC}$ to $0.3V_{CC}$	0	0	1
0 V to $0.15V_{CC}$	0	0	0

[1] Accuracy is $\pm 0.03V_{CC}$. Bit BS5 must be set to logic 0 to disable the BS5 output port. The BS5 output port uses the same pin as the ADC and can not be used when the ADC is in use.

8.3 Status at power-on reset

At power on or when the supply voltage drops below approximately 2.85 V (at T_{amb} = 25 °C), internal registers are set according to Table 16.

At power on, the charge pump current is set to 580 µA, the test bits T[2:0] are set to 110 which means that the charge pump is sinking current, the tuning voltage output is disabled. The XTOUT buffer is on, driving the 4 MHz signal from the crystal oscillator and all the ports are off. As a consequence, the high band is selected by default.

Table 16. Default setting at power-on reset

Name	Byte	Bit[1]							
		MSB							LSB
Address byte	1	1	1	0	0	0	MA1	MA0	X
Divider byte 1 (DB1)	2	0	N14 = X	N13 = X	N12 = X	N11 = X	N10 = X	N9 = X	N8 = X
Divider byte 2 (DB2)	3	N7 = X	N6 = X	N5 = X	N4 = X	N3 = X	N2 = X	N1 = X	N0 = X
Control byte 1 (CB1)	4	1	T/A = X[2]	T2 = 1	T1 = 1	T0 = 0	R2 = X	R1 = X	R0 = X
		1	T/A = X[3]	0	0	ATC = 0	AL2 = 0	AL1 = 1	AL0 = 0
Control byte 2 (CB2)	5	CP2 = 1	CP1 = 1	CP0 = 1	BS5 = 0	BS4 = 0	BS3 = 0	BS2 = 0	BS1 = 0

[1] X means that this bit is not set or reset at power-on reset.

[2] The next six bits are written, when bit T/A = 1 in a write sequence.

[3] The next six bits are written, when bit T/A = 0 in a write sequence.

9. Internal circuitry

Table 17. Internal pin configuration

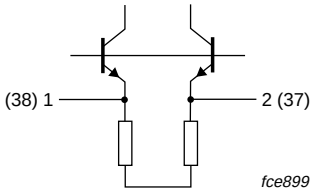
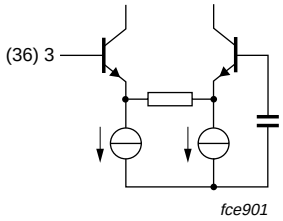
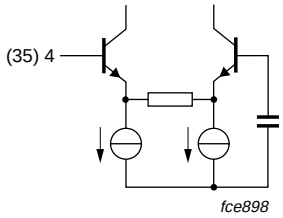
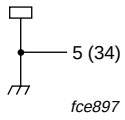
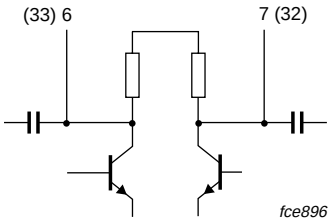
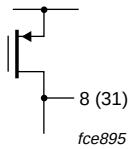
Symbol	Pin		Average DC voltage versus band selection			Description[1]
	TDA6650ATT	TDA6651ATT	Low	Mid	High	
HBIN1	1	38	n.a.	n.a.	1.0 V	
HBIN2	2	37	n.a.	n.a.	1.0 V	
MBIN	3	36	n.a.	1.8 V	n.a.	
LBIN	4	35	1.8 V	n.a.	n.a.	
RFGND	5	34	-	-	-	
IFFIL1	6	33	3.7 V	3.7 V	3.7 V	
IFFIL2	7	32	3.7 V	3.7 V	3.7 V	
BS4	8	31	high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$	

Table 17. Internal pin configuration *…continued*

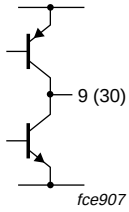
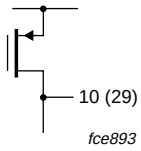
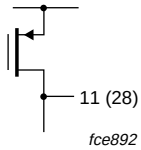
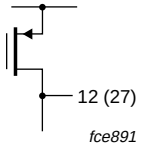
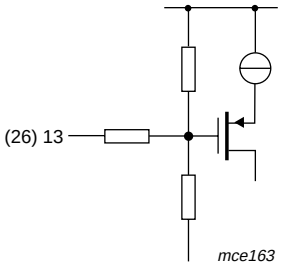
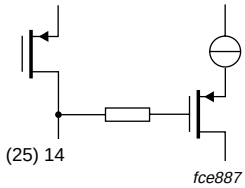
Symbol	Pin		Average DC voltage versus band selection			Description[1]
	TDA6650ATT	TDA6651ATT	Low	Mid	High	
AGC	9	30	0 V or 3.5 V	0 V or 3.5 V	0 V or 3.5 V	
BS3	10	29	high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$	
BS2	11	28	high-Z	$V_{CC} - V_{DS}$	high-Z	
BS1	12	27	$V_{CC} - V_{DS}$	high-Z	high-Z	
BVS	13	26	2.5 V	2.5 V	2.5 V	
ADC/BS5	14	25	V_{CEsat} or high-Z	V_{CEsat} or high-Z	V_{CEsat} or high-Z	

Table 17. Internal pin configuration *...continued*

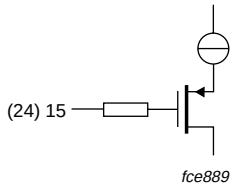
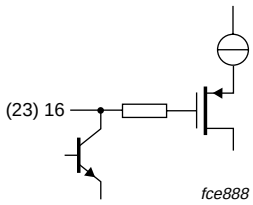
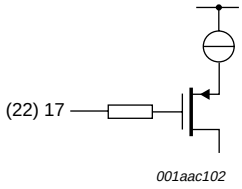
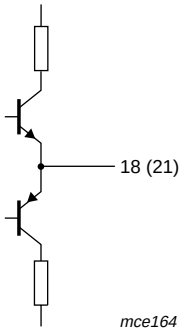
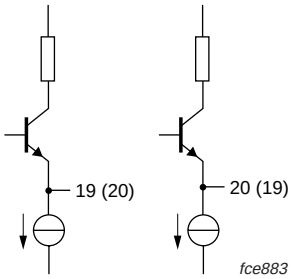
Symbol	Pin		Average DC voltage versus band selection			Description[1]
	TDA6650ATT	TDA6651ATT	Low	Mid	High	
SCL	15	24	high-Z	high-Z	high-Z	
SDA	16	23	high-Z	high-Z	high-Z	
AS	17	22	1.25 V	1.25 V	1.25 V	
XTOUT	18	21	3.45 V	3.45 V	3.45 V	
XTAL1	19	20	2.2 V	2.2 V	2.2 V	
XTAL2	20	19	2.2 V	2.2 V	2.2 V	
n.c.	21	18	n.a.	n.a.	n.a.	not connected

Table 17. Internal pin configuration *...continued*

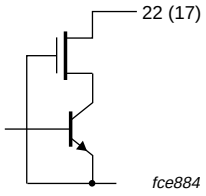
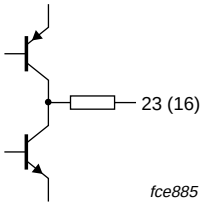
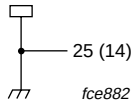
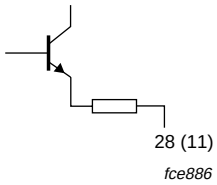
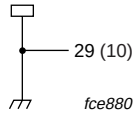
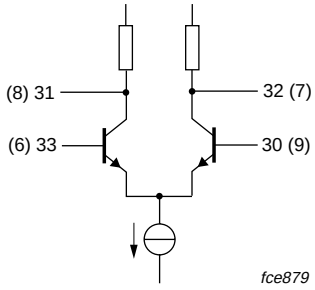
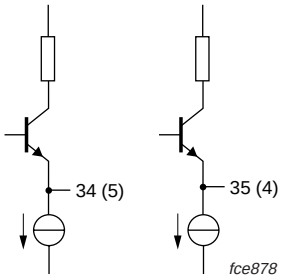
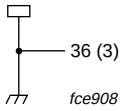
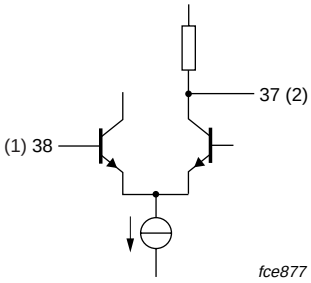
Symbol	Pin		Average DC voltage versus band selection			Description[1]
	TDA6650ATT	TDA6651ATT	Low	Mid	High	
VT	22	17	V_{VT}	V_{VT}	V_{VT}	
CP	23	16	1.8 V	1.8 V	1.8 V	
V_{CCD}	24	15	5 V	5 V	5 V	
PLLGND	25	14	-	-	-	
V_{CCA}	26	13	5 V	5 V	5 V	
IFOUTB	27	12	2.1 V	2.1 V	2.1 V	
IFOUTA	28	11	2.1 V	2.1 V	2.1 V	
IFGND	29	10	-	-	-	
HOSCIN1	30	9	2.2 V	2.2 V	1.8 V	
HOSCOUT1	31	8	5 V	5 V	2.5 V	
HOSCOUT2	32	7	5 V	5 V	2.5 V	
HOSCIN2	33	6	2.2 V	2.2 V	1.8 V	

Table 17. Internal pin configuration *...continued*

Symbol	Pin		Average DC voltage versus band selection			Description[1]
	TDA6650ATT	TDA6651ATT	Low	Mid	High	
MOSCIN1	34	5	2.3 V	1.3 V	2.3 V	
MOSCIN2	35	4	2.3 V	1.3 V	2.3 V	
OSCGND	36	3	-	-	-	
LOSCOUT	37	2	1.7 V	1.4 V	1.4 V	
LOSCIN	38	1	2.9 V	3.5 V	3.5 V	

[1] The pin numbers in parenthesis refer to the TDA6651ATT.

10. Limiting values

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Positive currents are entering the IC and negative currents are going out of the IC; all voltages are referenced to ground (GND)[1].

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCA}	analog supply voltage		–0.3	+6	V
V_{CCD}	digital supply voltage		–0.3	+6	V
V_{VT}	tuning voltage output		–0.3	+35	V
V_{SDA}	serial data input and output voltage		–0.3	+6	V
I_{SDA}	serial data output current	during acknowledge	0	10	mA
V_{SCL}	serial clock input voltage		–0.3	+6	V
V_{AS}	address selection input voltage		–0.3	+6	V

Table 18. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Positive currents are entering the IC and negative currents are going out of the IC; all voltages are referenced to ground (GND)[1].

Symbol	Parameter	Conditions		Min	Max	Unit
V_n	voltage on all other inputs, outputs and combined inputs and outputs, except GNDs	4.5 V < V_{CC} < 5.5 V	[2]	–0.3	V_{CC} + 0.3	V
I_{BSn}	PMOS port output current	corresponding port on; open-drain		–20	0	mA
$I_{BS(tot)}$	sum of all PMOS port output currents	open-drain		–50	0	mA
$t_{sc(max)}$	maximum short-circuit time	each pin to V_{CC} or to GND		-	10	s
T_{stg}	storage temperature			–40	+150	°C
T_{amb}	ambient temperature		[3]	–20	$T_{amb(max)}$	°C
T_j	junction temperature			-	150	°C

[1] Maximum ratings cannot be exceeded, not even momentarily without causing irreversible IC damage. Maximum ratings cannot be accumulated.

[2] V_{CC} refers to the operating supply voltage.

[3] The maximum allowed ambient temperature $T_{amb(max)}$ depends on the assembly conditions of the package and especially on the design of the printed-circuit board. The application mounting must be done in such a way that the maximum junction temperature is never exceeded. An estimation of the junction temperature can be obtained through measurement of the temperature of the top center of the package ($T_{package}$). The temperature difference junction to case (ΔT_{j-c}) is estimated at about 13 °C on the demo board (PCB 827-3). The junction temperature $T_j = T_{package} + \Delta T_{j-c}$.

11. Thermal characteristics

Table 19. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1][2][3]		
	TDA6650ATT			82	K/W
	TDA6651ATT			74	K/W

[1] Measured in free air as defined by JEDEC standard JESD51-2.

[2] These values are given for information only. The thermal resistance depends strongly on the nature and design of the printed-circuit board used in the application. The thermal resistance given corresponds to the value that can be measured on a multilayer printed-circuit board (4 layers) as defined by JEDEC standard.

[3] The junction temperature influences strongly the reliability of an IC. The printed-circuit board used in the application contributes in a large part to the overall thermal characteristic. It must therefore be insured that the junction temperature of the IC never exceeds $T_{j(max)}$ = 150 °C at the maximum ambient temperature.

12. Characteristics

Table 20. Characteristics

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{CC}	supply voltage			4.5	5.0	5.5	V
I_{CC}	supply current	PMOS ports off		80	96	115	mA
		one PMOS port on: sourcing 15 mA		96	112	131	mA
		two PMOS ports on: one port sourcing 15 mA and one other port sourcing 5 mA		101	117	136	mA
General functions							
V_{POR}	power-on reset supply voltage	power-on reset active if $V_{CC} < V_{POR}$		-	2.85	3.5	V
Δf_{lock}	frequency range the PLL is able to synthesize			64	-	1024	MHz
Crystal oscillator[1]							
f_{xtal}	crystal frequency			-	4.0	-	MHz
$\lvert Z_{xtal} \rvert$	input impedance (absolute value)	f_{xtal} = 4 MHz; V_{CC} = 4.5 V to 5.5 V T_{amb} = –20 °C to $T_{amb(max)}$, see Section 10		350	430	-	Ω
P_{xtal}	crystal drive level	f_{xtal} = 4 MHz	[2]	-	70	-	µW
PMOS ports: pins BS1, BS2, BS3, BS4 and BS5							
$I_{LO(off)}$	output leakage current in off state	V_{CC} = 5.5 V; V_{BS} = 0 V		–10	-	-	µA
$V_{DS(sat)}$	output saturation voltage	only corresponding buffer is on, sourcing 15 mA; $V_{DS(sat)} = V_{CC} - V_{BS}$		-	0.2	0.4	V
ADC input: pin ADC							
V_i	ADC input voltage	see Table 15		0	-	5.5	V
I_{IH}	HIGH-level input current	$V_{ADC} = V_{CC}$		-	-	10	µA
I_{IL}	LOW-level input current	V_{ADC} = 0 V		–10	-	-	µA
Address selection input: pin AS							
I_{IH}	HIGH-level input current	V_{AS} = 5.5 V		-	-	10	µA
I_{IL}	LOW-level input current	V_{AS} = 0 V		–10	-	-	µA
Bus voltage selection input: pin BVS							
I_{IH}	HIGH-level input current	V_{BVS} = 5.5 V		-	-	100	µA
I_{IL}	LOW-level input current	V_{BVS} = 0 V		–100	-	-	µA
Buffered output: pin XTOUT							
$V_{o(p-p)}$	square wave AC output voltage (peak-to-peak value)		[3]	-	400	-	mV
Z_o	output impedance			-	175	-	Ω

Table 20. Characteristics *...continued*

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C-bus						
Inputs: pins SCL and SDA						
f_{clk}	clock frequency	frequency on SCL	-	-	400	kHz
V_{IL}	LOW-level input voltage	V_{BVS} = 0 V	0	-	0.75	V
		V_{BVS} = 2.5 V or open-circuit	0	-	1.0	V
		V_{BVS} = 5 V	0	-	1.5	V
V_{IH}	HIGH-level input voltage	V_{BVS} = 0 V	1.75	-	5.5	V
		V_{BVS} = 2.5 V or open-circuit	2.3	-	5.5	V
		V_{BVS} = 5 V	3.0	-	5.5	V
I_{IH}	HIGH-level input current	V_{CC} = 0 V; V_{BUS} = 5.5 V	-	-	10	µA
		V_{CC} = 5.5 V; V_{BUS} = 5.5 V	-	-	10	µA
I_{IL}	LOW-level input current	V_{CC} = 0 V; V_{BUS} = 1.5 V	-	-	10	µA
		V_{CC} = 5.5 V; V_{BUS} = 0 V	–10	-	-	µA
Output: pin SDA						
I_{LH}	leakage current	V_{SDA} = 5.5 V	-	-	10	µA
$V_{O(ack)}$	output voltage during acknowledge	I_{SDA} = 3 mA	-	-	0.4	V
Charge pump output: pin CP						
$\lvert I_o \rvert$	output current (absolute value)	see Table 12	-	-	-	µA
$I_{L(off)}$	off-state leakage current	charge pump off (T[2:0] = 010)	–15	0	+15	nA
Tuning voltage output: pin VT						
$I_{L(off)}$	leakage current when switched-off	tuning supply voltage = 33 V	-	-	10	µA
$V_{o(cl)}$	output voltage when the loop is closed	tuning supply voltage = 33 V; R_L = 15 kΩ	0.3	-	32.7	V
Noise performance						
$J_{\phi(rms)}$	phase jitter (RMS value)	integrated between 1 kHz and 1 MHz offset from the carrier				
		digital application: TDA6650ATT/C3/S2, TDA6651ATT/C3/S2, TDA6651ATT/C3/S3	-	0.5	-	deg
		hybrid application: TDA6650ATT/C3, TDA6651ATT/C3	-	0.6	-	deg

Table 20. Characteristics *...continued*

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Low band mixer, including IF amplifier							
f_{RF}	RF frequency	picture carrier for hybrid application TDA6650ATT/C3, TDA6651ATT/C3	[4]	91.25	-	219.143	MHz
		picture carrier for digital-only application TDA6650ATT/C3/S2, TDA6651ATT/C3/S2, TDA6651ATT/C3/S3	[4]	93.00	-	220.893	MHz
G_v	voltage gain	asymmetrical IF output; R_L = 75 Ω; see Figure 14					
		f_{RF} = 91.25 MHz		20	23.5	26	dB
		f_{RF} = 219.143 MHz		20	24.0	26	dB
		symmetrical IF output; R_L = 1.25 kΩ; see Figure 15					
		f_{RF} = 91.25 MHz		25	27.5	31	dB
		f_{RF} = 219.143 MHz		25	27.5	31	dB
NF	noise figure	f_{RF} = 150 MHz		-	7	10	dB
V_o	output voltage causing 1 % cross modulation in channel	asymmetrical application; see Figure 18	[5]				
		f_{RF} = 91.25 MHz		107	110	-	dBμV
		f_{RF} = 219.143 MHz		107	110	-	dBμV
		symmetrical application; see Figure 19	[5]				
		f_{RF} = 91.25 MHz		117	120	-	dBμV
		f_{RF} = 219.143 MHz		117	120	-	dBμV
V_i	input voltage causing 750 Hz frequency deviation pulling in channel	asymmetrical IF output		-	85	-	dBμV
$V_{i(lock)}$	input level without lock-out	see Figure 25	[7]	-	-	120	dBμV
G_i	input conductance	f_{RF} = 91.25 MHz; see Figure 5		-	0.15	-	mS
		f_{RF} = 219.43 MHz; see Figure 5		-	0.20	-	mS
C_i	input capacitance	f_{RF} = 91.25 MHz to 219.43 MHz; see Figure 5		-	1.60	-	pF
Mid band mixer, including IF amplifier							
f_{oper}	operating frequency	for hybrid application TDA6650ATT/C3, TDA6651ATT/C3		163.25	-	465.143	MHz
		picture carrier for digital only application TDA6650ATT/C3/S2, TDA6651ATT/C3/S2, TDA6651ATT/C3/S3		165.00	-	466.893	MHz

Table 20. Characteristics *…continued*

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{RF}	RF frequency	picture carrier for hybrid application TDA6650ATT/C3, TDA6651ATT/C3	[4]	223.25	-	465.143	MHz
		picture carrier for digital only application TDA6650ATT/C3/S2, TDA6651ATT/C3/S2, TDA6651ATT/C3/S3	[4]	225.00	-	466.893	MHz
G_v	voltage gain	asymmetrical IF output; load = 75 Ω; see Figure 14					
		f_{RF} = 223.25 MHz		20	23.5	26	dB
		f_{RF} = 465.143 MHz		20	24	26	dB
		symmetrical IF output; load = 1.25 kΩ; see Figure 15					
		f_{RF} = 223.25 MHz		25	27	31	dB
		f_{RF} = 465.143 MHz		25	27.5	31	dB
NF	noise figure	f_{RF} = 300 MHz; see Figure 17		-	8	11	dB
V_o	output voltage causing 1 % cross modulation in channel	asymmetrical application; see Figure 18	[5]				
		f_{RF} = 223.25 MHz		107	110	-	dBµV
		f_{RF} = 465.143 MHz		107	110	-	dBµV
		symmetrical application; see Figure 19	[5]				
		f_{RF} = 223.25 MHz		117	120	-	dBµV
		f_{RF} = 465.143 MHz		117	120	-	dBµV
V_i	input voltage causing 750 Hz frequency deviation pulling in channel	asymmetrical IF output		-	87	-	dBµV
$V_{i(lock)}$	input level without lock-out	see Figure 25	[7]	-	-	120	dBµV
G_i	input conductance	see Figure 6		-	0.3	-	mS
C_i	input capacitance	see Figure 6		-	1.1	-	pF
High band mixer, including IF amplifier							
f_{oper}	operating frequency	for hybrid application TDA6650ATT/C3, TDA6651ATT/C3		355.25	-	767.143	MHz
		picture carrier for digital only application TDA6650ATT/C3/S2, TDA6651ATT/C3/S2, TDA6651ATT/C3/S3		357.00	-	768.893	MHz

Table 20. Characteristics *...continued*

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{RF}	RF frequency	picture carrier for hybrid application TDA6650ATT/C3, TDA6651ATT/C3	[4]	471.25	-	767.143	MHz
		picture carrier for digital only application TDA6650ATT/C3/S2, TDA6651ATT/C3/S2, TDA6651ATT/C3/S3	[4]	473.00	-	768.893	MHz
G_v	voltage gain	asymmetrical IF output; load = 75 Ω; see Figure 20					
		f_{RF} = 471.25 MHz		31.5	35	37.5	dB
		f_{RF} = 767.143 MHz		31.5	33.5	37.5	dB
		symmetrical IF output; load = 1.25 kΩ; see Figure 21					
		f_{RF} = 471.25 MHz		35.5	38.5	41.5	dB
		f_{RF} = 767.143 MHz		35.5	37	41.5	dB
NF	noise figure, not corrected for image	see Figure 22					
		f_{RF} = 471.25 MHz		-	6	8	dB
		f_{RF} = 767.143 MHz		-	7	9	dB
V_o	output voltage causing 1 % cross modulation in channel	asymmetrical application; see Figure 23	[5]				
		f_{RF} = 471.25 MHz		107	110	-	dBμV
		f_{RF} = 767.143 MHz		107	110	-	dBμV
		symmetrical application; see Figure 24	[5]				
		f_{RF} = 471.25 MHz		117	120	-	dBμV
		f_{RF} = 767.143 MHz		117	120	-	dBμV
$V_{i(lock)}$	input level without lock-out	see Figure 26	[7]	-	-	120	dBμV
V_i	input voltage causing 750 Hz frequency deviation pulling in channel	asymmetrical IF output		-	75	-	dBμV
Z_i	input impedance (R_S + jL_Sω)	f_{RF} = 471.25 MHz; see Figure 7					
		R_S		-	35	-	Ω
		L_S		-	8	-	nH
		f_{RF} = 767.143 MHz; see Figure 7					
		R_S		-	36	-	Ω
		L_S		-	8	-	nH
Low band oscillator							
f_{osc}	oscillator frequency		[7]	150	-	276.143	MHz
$\Delta f_{osc(V)}$	oscillator frequency shift with supply voltage		[8]	-	110	300	kHz

Table 20. Characteristics *...continued*

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta f_{osc(T)}$	oscillator frequency drift with temperature	ΔT = 25 °C; V_{CC} = 5 V with compensation	[9]	-	900	-	kHz
$\Phi_{osc(dig)}$	phase noise, carrier to sideband noise in digital application	TDA6650ATT/C3/S2; TDA6651ATT/C3/S2; TDA6651ATT/C3/S3					
		±1 kHz frequency offset; f_{comp} = 4 MHz; see Figure 8, 27 and 28		82	90	-	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figure 9, 27 and 28		87	94	-	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figure 10, 27 and 28		104	115	-	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figure 27 and 28		-	117	-	dBc/Hz
$\Phi_{osc(hyb)}$	phase noise, carrier to sideband noise in hybrid application	TDA6650ATT/C3; TDA6651ATT/C3					
		±1 kHz frequency offset; f_{comp} = 4 MHz; see Figure 11, 29 and 30		75	81	-	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figure 12, 29 and 30		85	92	-	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figure 13, 29 and 30		104	115	-	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figure 29 and 30		-	117	-	dBc/Hz
RSC_{p-p}	ripple susceptibility of V_{CC} (peak-to-peak value)	V_{CC} = 5 V ± 5 %; worst case in the frequency range; ripple frequency 500 kHz	[10]	15	200	-	mV
Mid band oscillator							
f_{osc}	oscillator operating frequency			222	-	522.143	MHz
	oscillator frequency		[7]	276	-	522.143	MHz
$\Delta f_{osc(V)}$	oscillator frequency shift with supply voltage		[8]	-	300	-	kHz
$\Delta f_{osc(T)}$	oscillator frequency drift with temperature	ΔT = 25 °C; V_{CC} = 5 V with compensation	[9]	-	1500	-	kHz

Table 20. Characteristics *...continued*

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Phi_{osc(dig)}$	phase noise, carrier to sideband noise in digital application	TDA6650ATT/C3/S2; TDA6651ATT/C3/S2; TDA6651ATT/C3/S3					
		±1 kHz frequency offset; f_{comp} = 4 MHz; see Figure 8, 27 and 28		85	90	-	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figure 9, 27 and 28		87	94	-	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figure 10, 27 and 28		104	112	-	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figure 27 and 28		-	116	-	dBc/Hz
$\Phi_{osc(hyb)}$	phase noise, carrier to sideband noise in hybrid application	TDA6650ATT/C3; TDA6651ATT/C3					
		±1 kHz frequency offset; f_{comp} = 4 MHz; see Figure 11, 29 and 30		80	86	-	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figure 12, 29 and 30		85	92	-	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figure 13, 29 and 30		104	115	-	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figure 29 and 30		-	115	-	dBc/Hz
RSC_{p-p}	ripple susceptibility of V_{CC} (peak-to-peak value)	V_{CC} = 5 V ± 5 %; worst case in the frequency range; ripple frequency 500 kHz	[10]	15	140	-	mV
High band oscillator							
f_{osc}	oscillator operating frequency			414	-	824.143	MHz
	oscillator frequency		[7]	522	-	824.143	MHz
$\Delta f_{osc(V)}$	oscillator frequency shift with supply voltage		[8]	-	300	-	kHz
$\Delta f_{osc(T)}$	oscillator frequency drift with temperature	ΔT = 25 °C; V_{CC} = 5 V; with compensation	[9]	-	1100	-	kHz

Table 20. Characteristics *...continued*

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Phi_{osc(dig)}$	phase noise, carrier to sideband noise in digital application	TDA6650ATT/C3/S2; TDA6651ATT/C3/S2; TDA6651ATT/C3/S3					
		±1 kHz frequency offset; f_{comp} = 4 MHz; see Figure 8, 27 and 28		80	85	-	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figure 9, 27 and 28		85	91	-	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figure 11, 27 and 28		104	112	-	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figure 27 and 28		-	117	-	dBc/Hz
$\Phi_{osc(hyb)}$	phase noise, carrier to sideband noise in hybrid application	TDA6650ATT/C3; TDA6651ATT/C3					
		±1 kHz frequency offset; f_{comp} = 4 MHz; see Figure 11, 29 and 30		80	86	-	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figure 12, 29 and 30		82	88	-	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figure 13, 29 and 30		104	112	-	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figure 29 and 30		-	117	-	dBc/Hz
RSC_{p-p}	ripple susceptibility of V_{CC} (peak-to-peak value)	V_{CC} = 5 V ± 5 %; worst case in the frequency range; ripple frequency 500 kHz	[10]	15	40	-	mV
IF amplifier							
Z_o	output impedance	asymmetrical IF output					
		R_S at 57 MHz		-	50	-	Ω
		L_S at 57 MHz		-	4.7	-	nH
		symmetrical IF output					
		R_S at 57 MHz		-	100	-	Ω
		L_S at 57 MHz		-	10	-	nH
Rejection at the IF output (IF amplifier in asymmetrical mode)							
INT_{div}	divider interferences in IF level	worst case	[11]	-	-	20	dBµV
INT_{xtal}	crystal oscillator interferences rejection	V_{IF} = 100 dBµV; worst case in the frequency range	[12]	-	-	–50	dBc

Table 20. Characteristics *...continued*

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$INT_{f(step)}$	step frequency rejection	V_{IF} = 100 dBμV; worst case in the frequency range	[13]				
		digital application TDA6650ATT/C3/S2, TDA6651ATT/C3/S2		-	-	–50	dBc
		digital application TDA6651ATT/C3/S3		-	-	–35	dBc
		hybrid application TDA6650ATT/C3, TDA6651ATT/C3		-	-	–57	dBc
INT_{XTH}	crystal oscillator harmonics in the IF frequency		[14]	-	-	50	dBμV
AGC output (IF amplifier in asymmetrical mode): pin AGC							
$AGC_{TOP(p-p)}$	AGC take-over point (peak-to-peak level)	bits AL[2:0] = 000		122.5	124	125.5	dBμV
$I_{source(fast)}$	source current fast			7.5	9.0	11.6	μA
$I_{source(slow)}$	source current slow			185	220	280	nA
V_o	output voltage	maximum level					
		TDA6650ATT/C3; TDA6651ATT/C3; TDA6650ATT/C3/S2; TDA6651ATT/C3/S2		3.45	3.55	3.8	V
		TDA6651ATT/C3/S3		3.3	3.55	3.8	V
		minimum level		0	-	0.1	V
$V_{o(dis)}$	output voltage with AGC disabled	bits AL[2:0] = 111					
		TDA6650ATT/C3; TDA6651ATT/C3; TDA6650ATT/C3/S2; TDA6651ATT/C3/S2		3.45	3.55	3.8	V
		TDA6651ATT/C3/S3		3.3	3.55	3.8	V
$V_{RF(slip)}$	RF voltage range to switch the AGC from active to not active mode			-	-	0.5	dB
V_{RML}	low threshold AGC output voltage	AGC bit = 0 or AGC not active		0	-	2.8	V
V_{RMH}	high threshold AGC output voltage	AGC bit = 1 or AGC active		3.2	3.55	3.8	V
I_{LO}	leakage current	bits AL[2:0] = 110; 0 < V_{AGC} < 3.5 V	[15]	–50	-	+50	nA

[1] Important recommendation: to obtain the performances mentioned in this specification, the serial resistance of the crystal used with this oscillator must never exceed 120 Ω. The crystal oscillator is guaranteed to operate at any supply voltage between 4.5 V and 5.5 V and at any temperature between –20 °C and $T_{amb(max)}$, as defined in Section 10.

[2] The drive level is expected with a 50 Ω series resistance of the crystal at series resonance. The drive level will be different with other series resistance values.

[3] The V_{XTOUT} level is measured when the pin XTOUT is loaded with 5 kΩ in parallel with 10 pF.

[4] The RF frequency range is defined by the oscillator frequency range and the Intermediate Frequency (IF).

[5] The 1 % cross modulation performance is measured with AGC detector turned off (AGC bits set to 110).

[6] The IF output signal stays stable within the range of the step frequency for any RF input level up to 120 dBμV.

[7] Limits are related to the tank circuits used in Figure 27 and 28 for digital application or Figure 29 and 30 for hybrid application. Frequency bands may be adjusted by the choice of external components.

[8] The frequency shift is defined as a change in oscillator frequency when the supply voltage varies from V_{CC} = 5 V to 4.5 V or from V_{CC} = 5 V to 5.25 V. The oscillator is free running during this measurement.

[9] The frequency drift is defined as a change in oscillator frequency when the ambient temperature varies from T_{amb} = 25 °C to 50 °C or from T_{amb} = 25 °C to 0 °C. The oscillator is free running during this measurement.

[10] The supply ripple susceptibility is measured in the measurement circuit according to Figure 27 to Figure 30 using a spectrum analyzer connected to the IF output. An unmodulated RF signal is applied to the test board RF input. A sine wave signal with a frequency of 500 kHz is superimposed onto the supply voltage. The amplitude of this ripple signal is adjusted to bring the 500 kHz sidebands around the IF carrier to a level of –53.5 dB with respect to the carrier.

[11] This is the level of divider interferences close to the IF frequency. The low and mid band inputs must be left open (i.e. not connected to any load or cable); the high band inputs are connected to an hybrid.

[12] Crystal oscillator interference means the 4 MHz sidebands caused by the crystal oscillator.

[13] The step frequency rejection is the level of step frequency sidebands related to the carrier. The measurement is done for V_{IF} = 100 dBμV. This specification point corresponds to the worst case observed in the frequency range. This parameter is specified for f_{step} = 142.86 kHz in digital applications and f_{step} = 62.5 kHz, 50 kHz or 142.86 kHz in hybrid application.

[14] This is the level of the 13rd and 15th harmonics of the 4 MHz crystal oscillator into the IF output.

[15] The AGC pin (pin 9 for TDA6650ATT and pin 30 for TDA6651ATT) must not be connected to a voltage higher than 3.6 V.

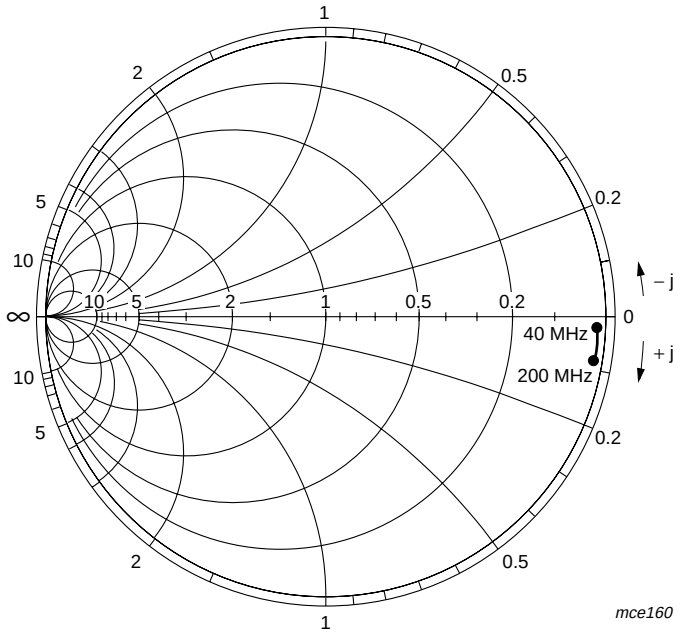


Fig 5. Input admittance (s_{11}) of the low band mixer (40 MHz to 200 MHz); Y_o = 20 mS

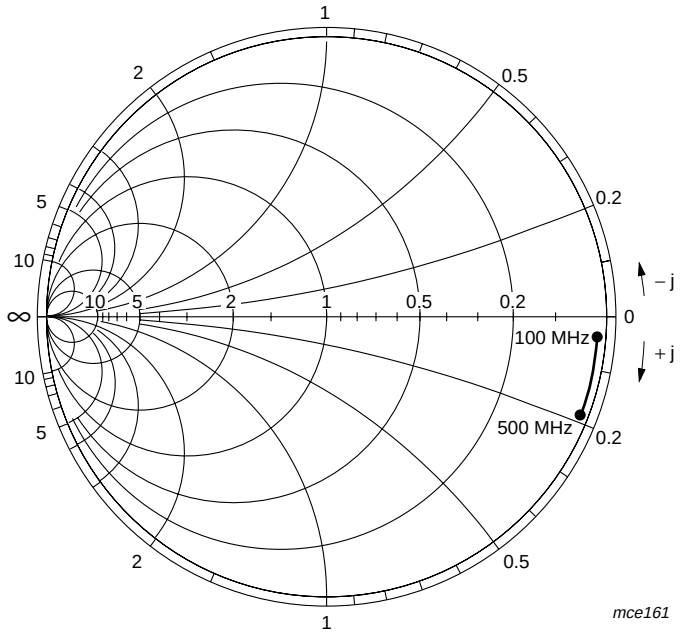


Fig 6. Input admittance (s_{11}) of the mid band mixer (100 MHz to 500 MHz); Y_o = 20 mS

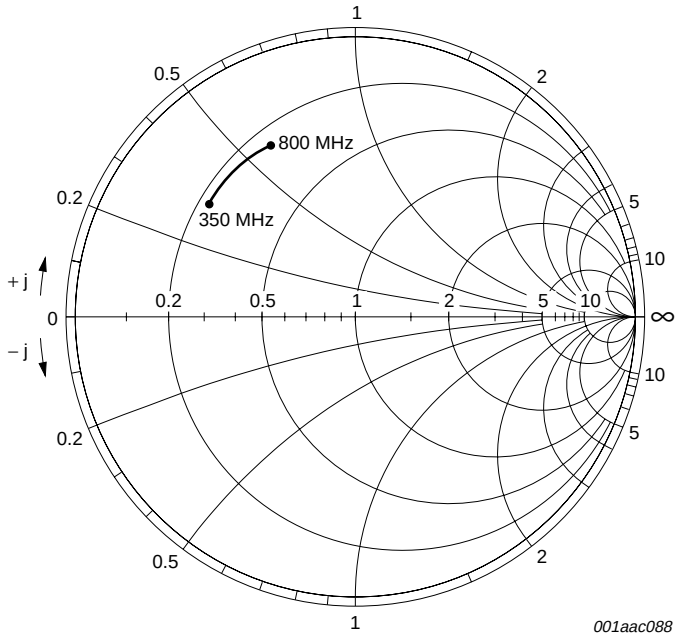
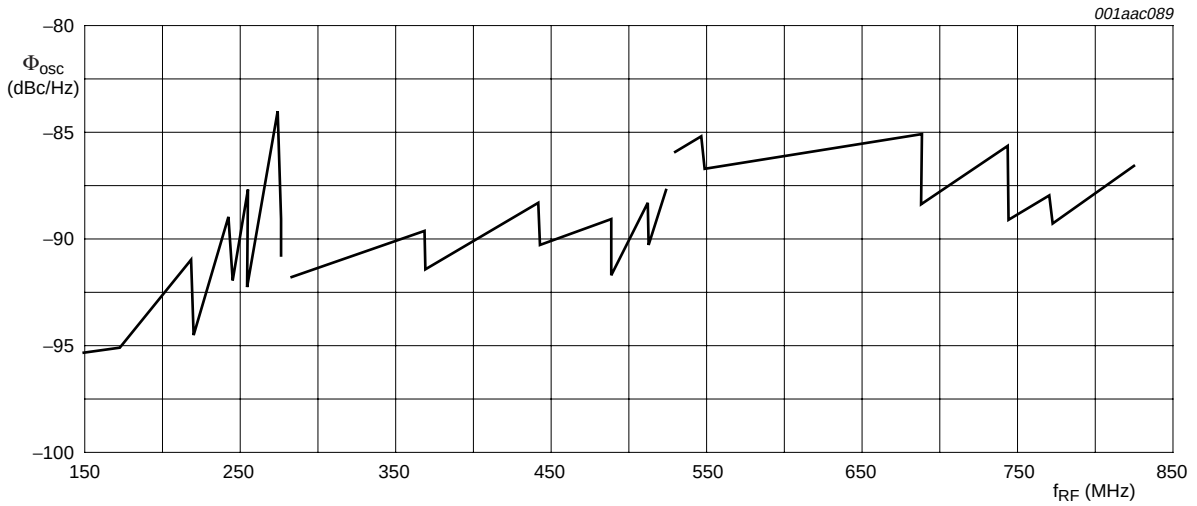
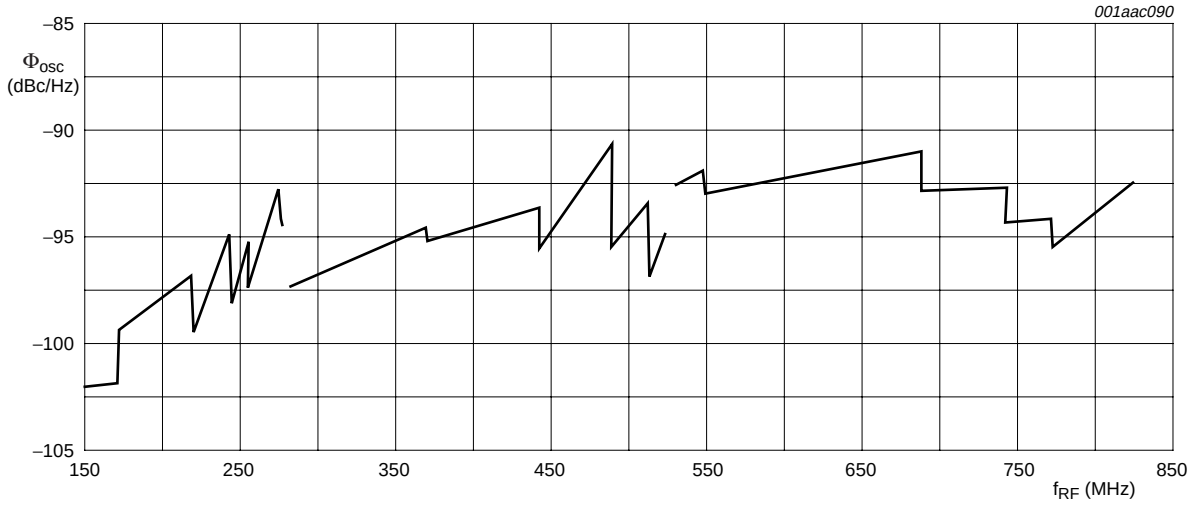


Fig 7. Input impedance (s_{11}) of the high band mixer (350 MHz to 800 MHz); Z_o = 100 Ω



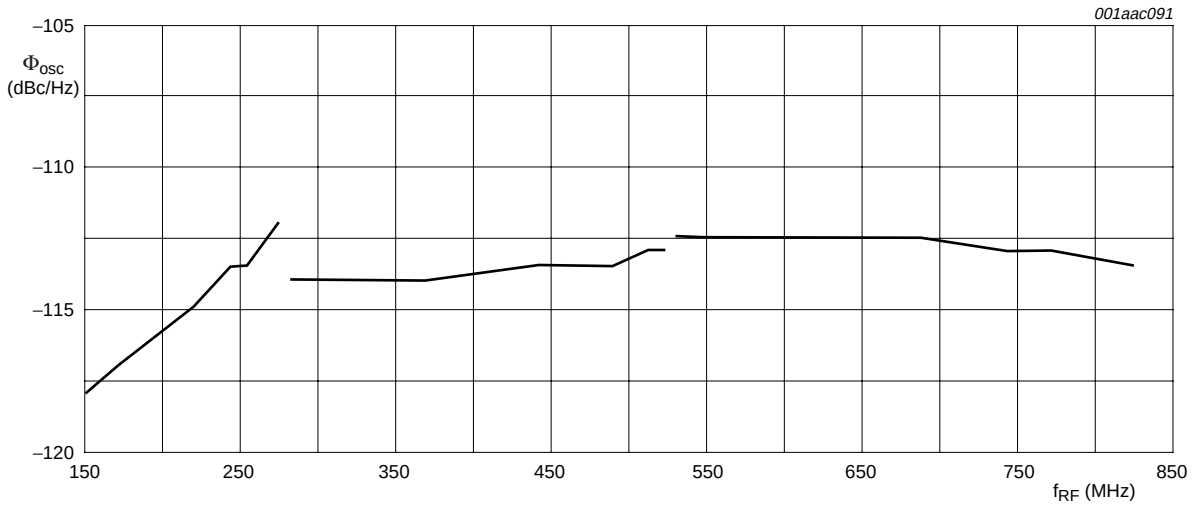
For measurement circuit see Figure 27 and Figure 28

Fig 8. 1 kHz phase noise typical performance in digital application



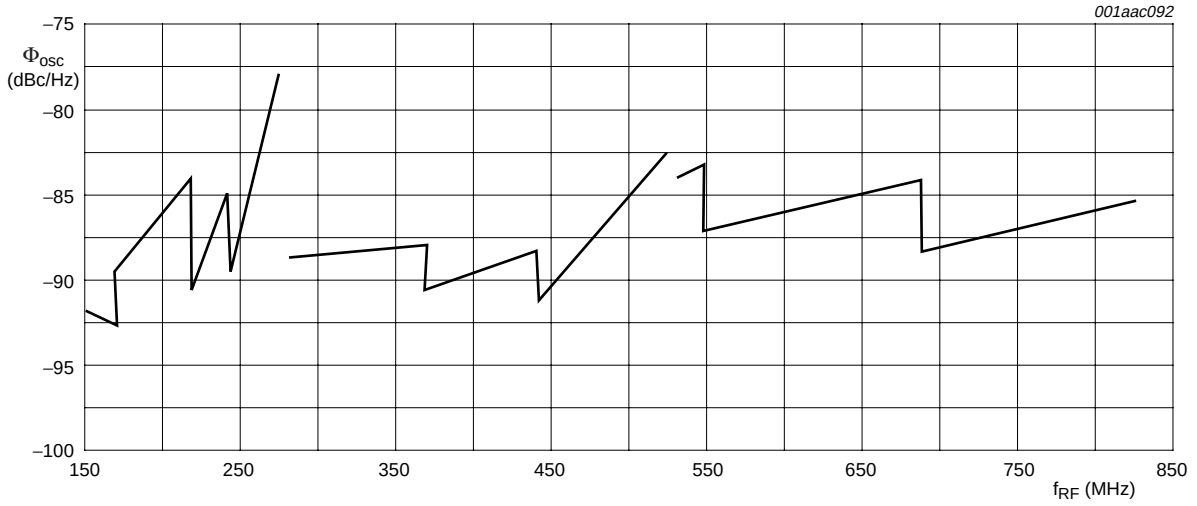
For measurement circuit see Figure 27 and Figure 28

Fig 9. 10 kHz phase noise typical performance in digital application



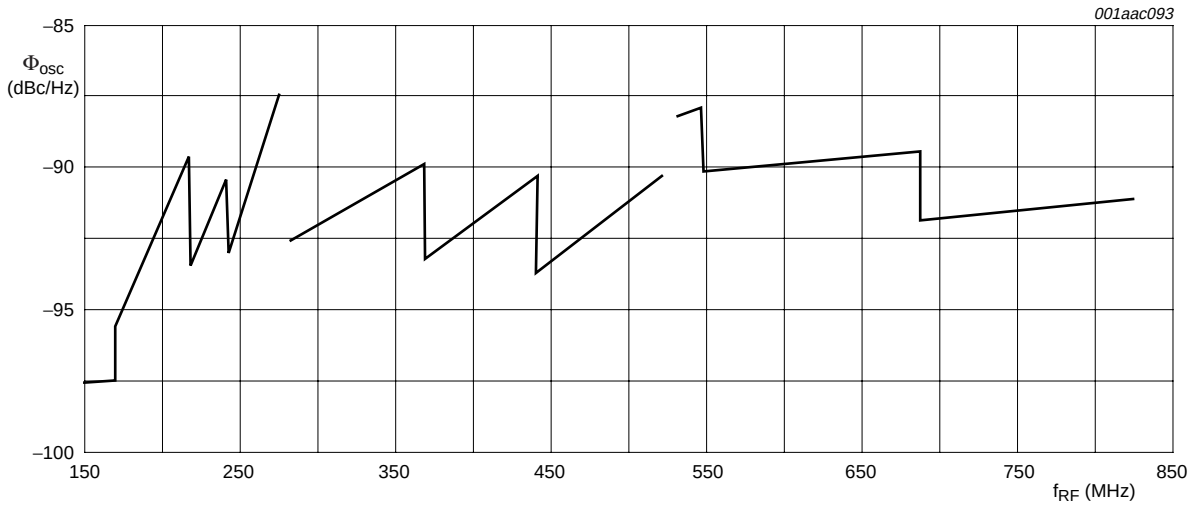
For measurement circuit see Figure 27 and Figure 28

Fig 10. 100 kHz phase noise typical performance in digital application



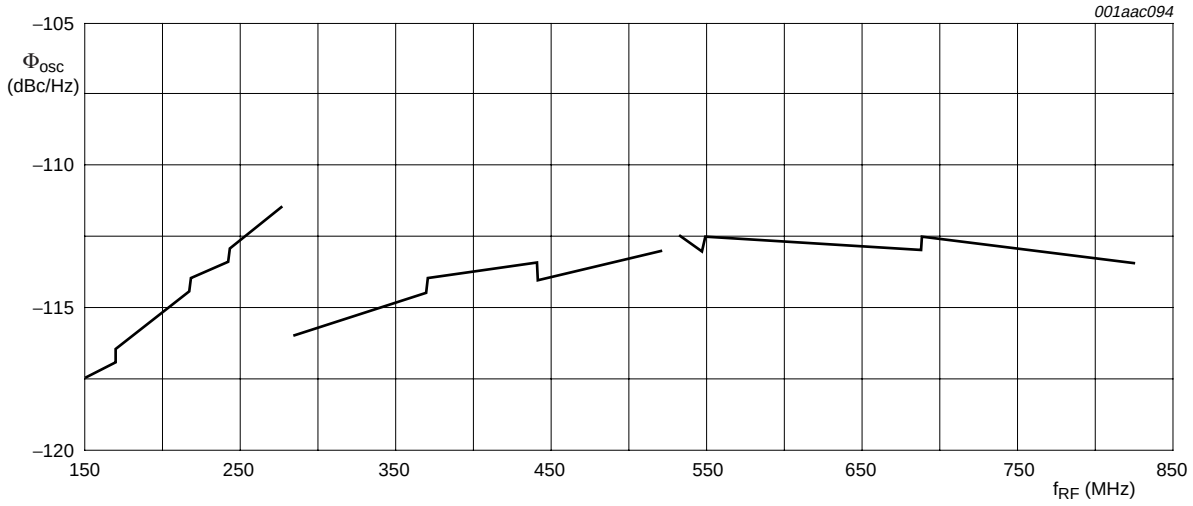
For measurement circuit see Figure 29 and Figure 30

Fig 11. 1 kHz phase noise typical performance in hybrid application



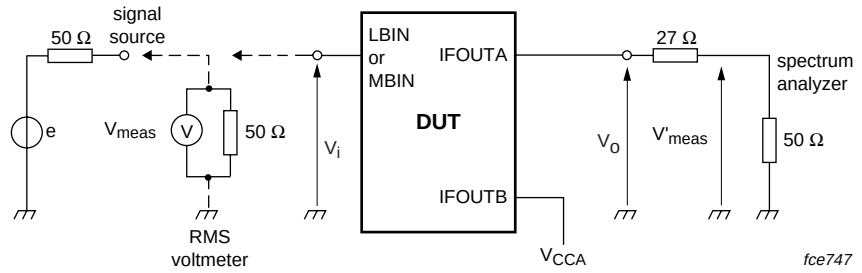
For measurement circuit see Figure 29 and Figure 30

Fig 12. 10 kHz phase noise typical performance in hybrid application



For measurement circuit see Figure 29 and Figure 30

Fig 13. 100 kHz phase noise typical performance in hybrid application



$Z_i >> 50\ \Omega \rightarrow V_i = 2 \times V_{meas} = 70\ dB\mu V.$

$V_i = V_{meas} + 6\ dB = 70\ dB\mu V.$

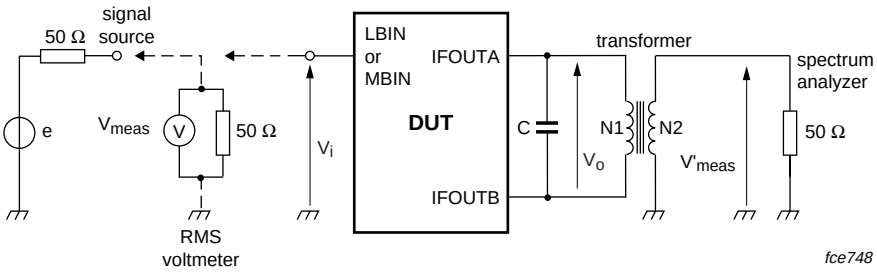
$V_o = V'_{meas} + 3.75\ dB.$

$$G_v = 20log\frac{V_o}{V_i}.$$

ISDB-T and NTSC Japan.

IF = 57 MHz.

Fig 14. Gain (G_V) measurement in low and mid band with asymmetrical IF output



$Z_i >> 50\ \Omega \rightarrow V_i = 2 \times V_{meas} = 70\ dB\mu V.$

$V_i = V_{meas} + 6\ dB = 70\ dB\mu V.$

$V_o = V'_{meas} + 15\ dB$ (transformer ratio N1/N2 = 5 and transformer loss).

$$G_v = 20log\frac{V_o}{V_i}.$$

ISDB-T and NTSC Japan.

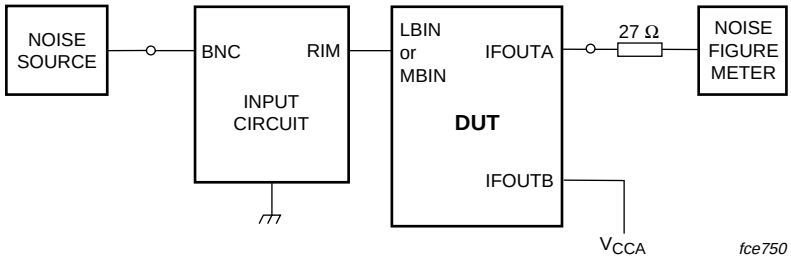
IF = 57 MHz.

N1 = 10 turns.

N2 = 2 turns.

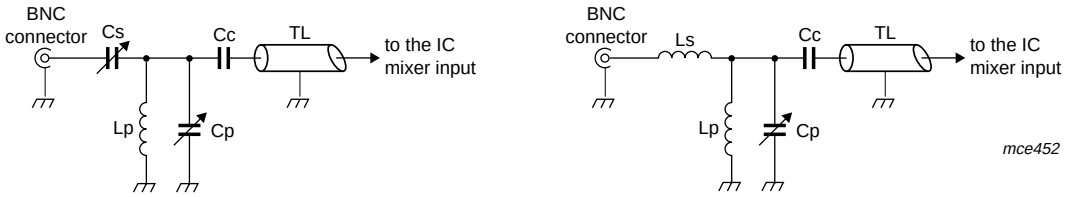
N1/N2 = 5.

Fig 15. Gain (G_V) measurement in low and mid band with symmetrical IF output



NF = NF_{meas} – loss of input circuit (dB).

Fig 16. Noise figure (NF) measurement in low and mid band with asymmetrical IF output



a. Schematic 1

For f_{RF} = 150 MHz

Loss = 0 dB.

Cs = 0.8 pF to 8 pF trimmer.

Cp = 0.4 pF to 2.5 pF trimmer.

Lp = 4 turns, 4.5 mm, 0.4 mm wire air coil.

Cc = 4.7 nF.

TL: 50 Ω semi rigid cable length = 75 mm.

b. Schematic 2

For f_{RF} = 300 MHz

Loss = 0.5 dB.

Ls = 2 turns, 1.5 mm, 0.4 mm wire air coil.

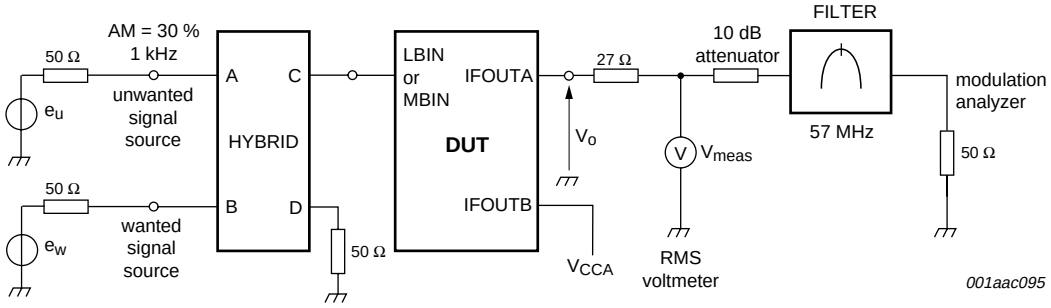
Cp = 8.2 pF in parallel with a 0.8 pF to 8 pF trimmer.

Lp = 2 turns, 1.5 mm, 0.4 mm wire air coil.

Cc = 4.7 nF.

TL: 50 Ω semi rigid cable length = 75 mm.

Fig 17. Input circuit for optimum noise figure measurement



$V_o = V_{meas} + 3.75$ dB.

$V'_{meas} = V_o$ – (transformer ratio N1/N2 = 5 and loss).

Wanted signal source at f_{RFpix} is 80 dBµV.

Unwanted output signal at f_{snd}.

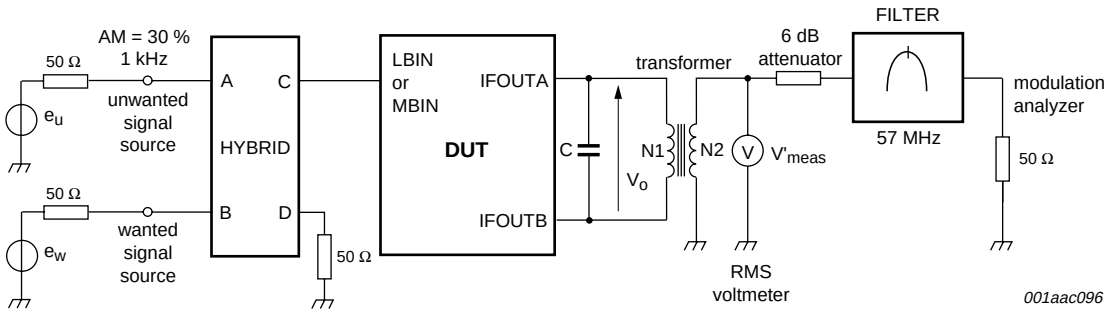
The level of unwanted signal is measured by causing 0.3 % AM modulation in the wanted signal.

N1 = 10 turns.

N2 = 2 turns.

N1/N2 = 5.

Fig 18. Cross modulation measurement in low and mid band with asymmetrical IF output



$V'_{meas} = V_o$ – (transformer ratio N1/N2 = 5 and loss).

Wanted signal source at f_{RFpix} is 80 dBµV.

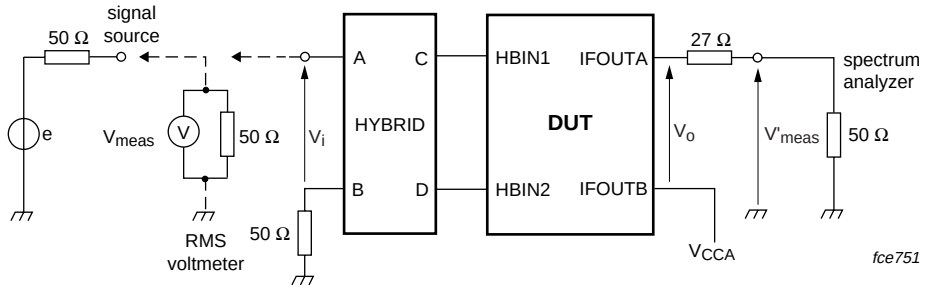
The level of unwanted signal V_o at f_{snd} is measured by causing 0.3 % AM modulation in the wanted output signal.

N1 = 10 turns.

N2 = 2 turns.

N1/N2 = 5.

Fig 19. Cross modulation measurement in low and mid band with symmetrical IF output



Loss in hybrid = 1 dB.

$V_i = V_{meas}$ – loss = 70 dBµV.

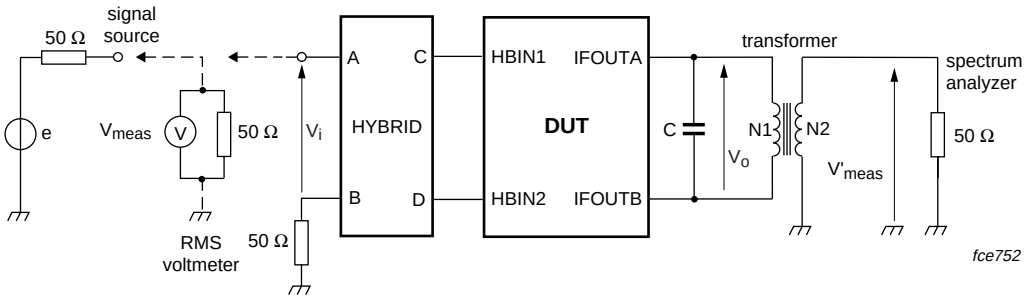
$V_o = V'_{meas}$ + 3.75 dB.

$$G_v = 20 log \frac{V_o}{V_i}.$$

ISDB-T and NTSC Japan.

IF = 57 MHz.

Fig 20. Gain (G_V) measurement in high band with asymmetrical IF output



Loss in hybrid = 1 dB.

$V_i = V_{meas}$ – loss = 70 dBµV.

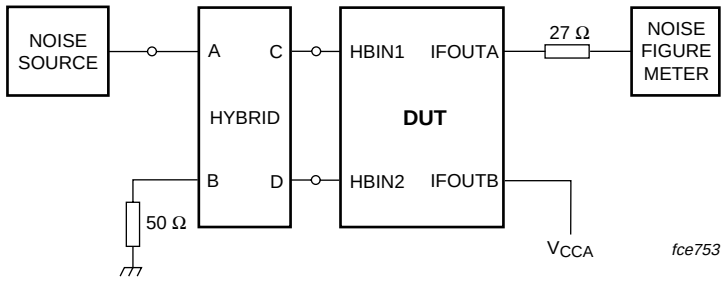
$V_o = V'_{meas}$ + 15 dB (transformer ratio N1/N2 = 5 and transformer loss).

$$G_v = 20 log \frac{V_o}{V_i}.$$

ISDB-T and NTSC Japan.

IF = 57 MHz.

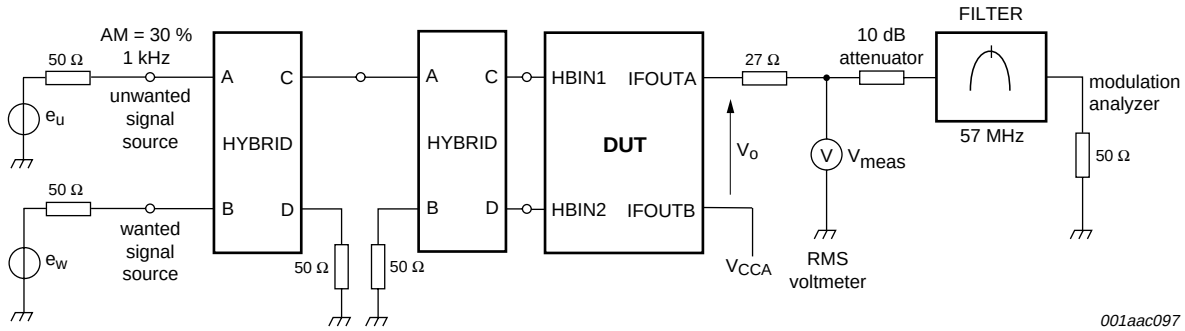
Fig 21. Gain (G_V) measurement in high band with symmetrical IF output



Loss in hybrid = 1 dB.

NF = NF_{meas} – loss.

Fig 22. Noise figure (NF) measurement in high band with asymmetrical IF output



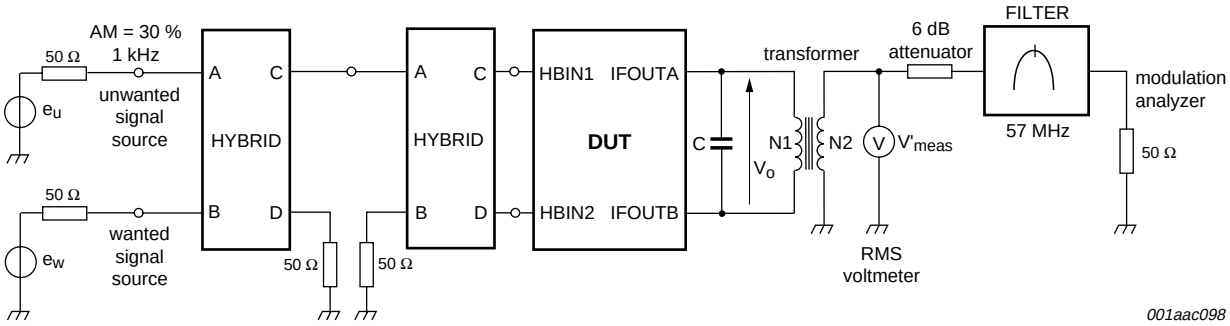
$V_o = V_{meas}$ + 3.75 dB.

Wanted signal source at f_{RFpix} is 70 dBµV.

Unwanted output signal at f_{snd}.

The level of unwanted signal is measured by causing 0.3 % AM modulation in the wanted signal.

Fig 23. Cross modulation measurement in high band with asymmetrical IF output



$V'_{meas} = V_o$ – (transformer ratio N1/N2 = 5 and loss).

Wanted signal source at f_{RFpix} is 70 dBµV.

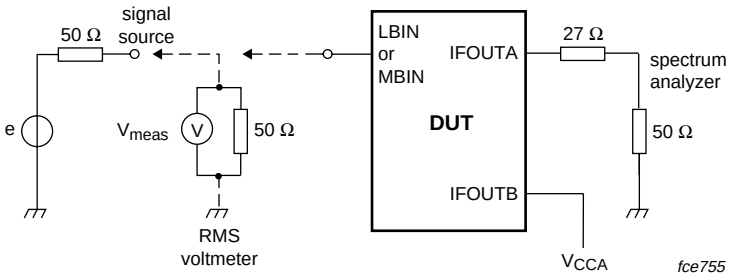
The level of unwanted signal V_o at f_{snd} is measured by causing 0.3 % AM modulation in the wanted output signal.

N1 = 10 turns.

N2 = 2 turns.

N1/N2 = 5.

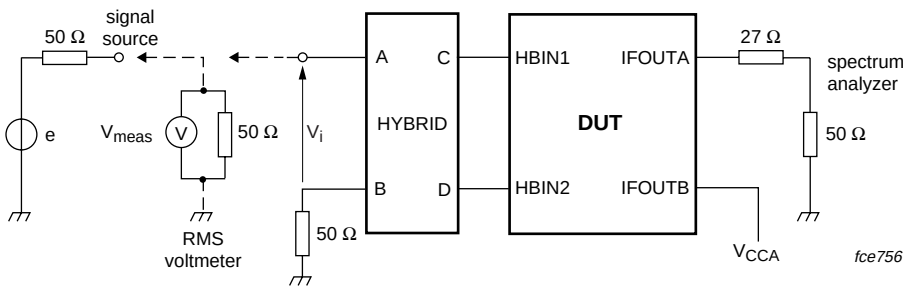
Fig 24. Cross modulation measurement in high band with symmetrical IF output



$Z_i >> 50\ \Omega \rightarrow V_i = 2 \times V_{meas}$.

$V_i = V_{meas} + 6$ dB.

Fig 25. Maximum RF input level without lock-out in low and mid band with asymmetrical IF output



Loss in hybrid = 1 dB.

$V_i = V_{meas}$ – loss.

Fig 26. Maximum RF input level without lock-out in high band with asymmetrical IF output

The TDA6650ATT; TDA6651ATT PLL loop stability is guaranteed in the configuration of the Figure 27 to Figure 30. In this configuration, the external supply source is 30 V minimum, the pull-up resistor, R19 is 15 kΩ and all of the local oscillators are aligned to operate at a maximum tuning voltage of 26 V. If the configuration is changed, there might be an impact on the loop stability.

For any other configurations, a stability analysis must be performed. The conventional PLL AC model used for the stability analysis, is valid provided the external source (DC supply source or DC-to-DC converter) is able to deliver a minimum current that is equal to the charge pump current in use.

The delivered current can be simply calculated with the following formula:

$$I_{delivered} = \left(\frac{V_{DC} - V_T}{R_{pu}}\right) > I_{CP} \quad (1)$$

where:

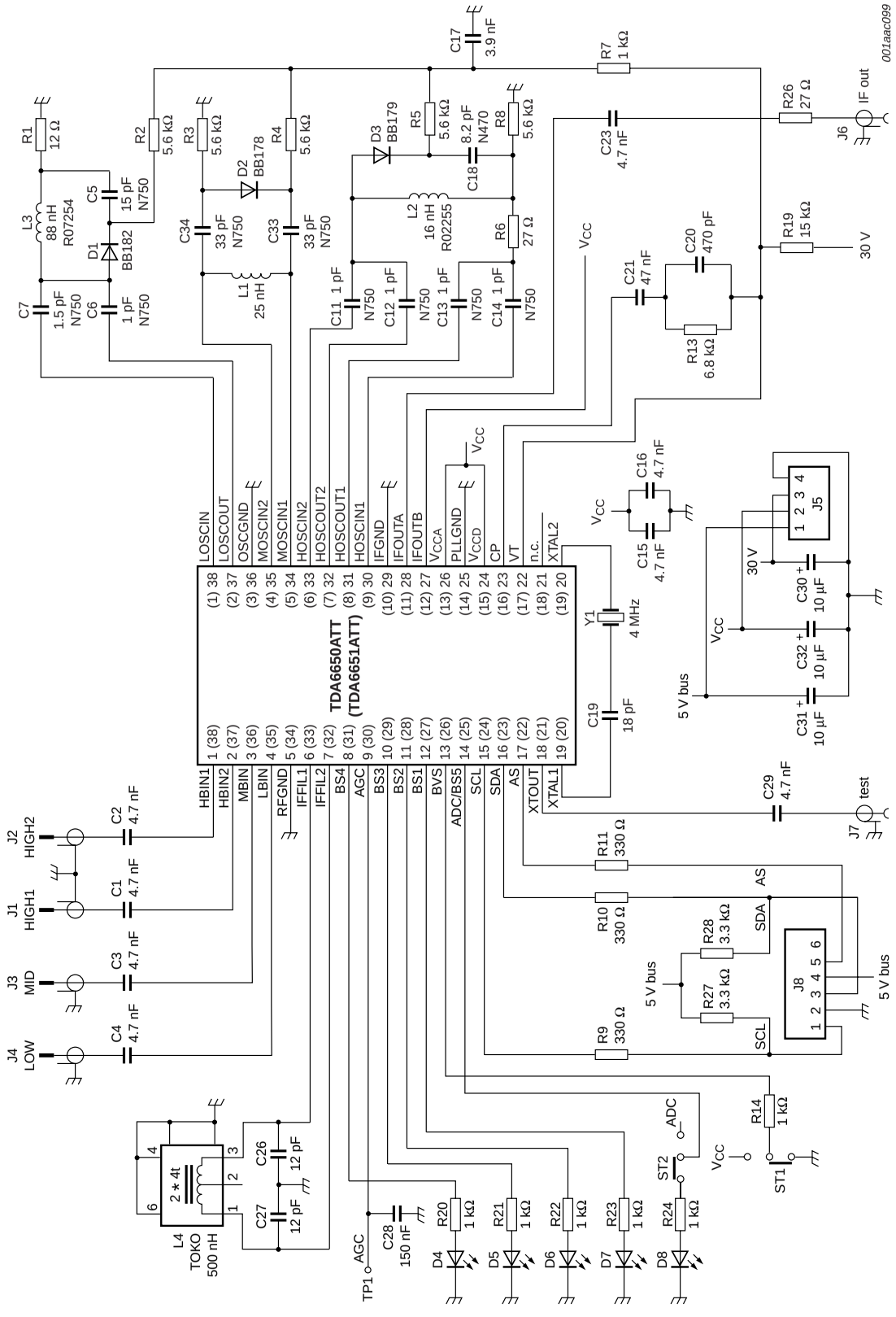
$I_{delivered}$ is the delivered current.

V_{DC} is the supply source voltage or DC-to-DC converter output voltage.

V_T is the tuning voltage.

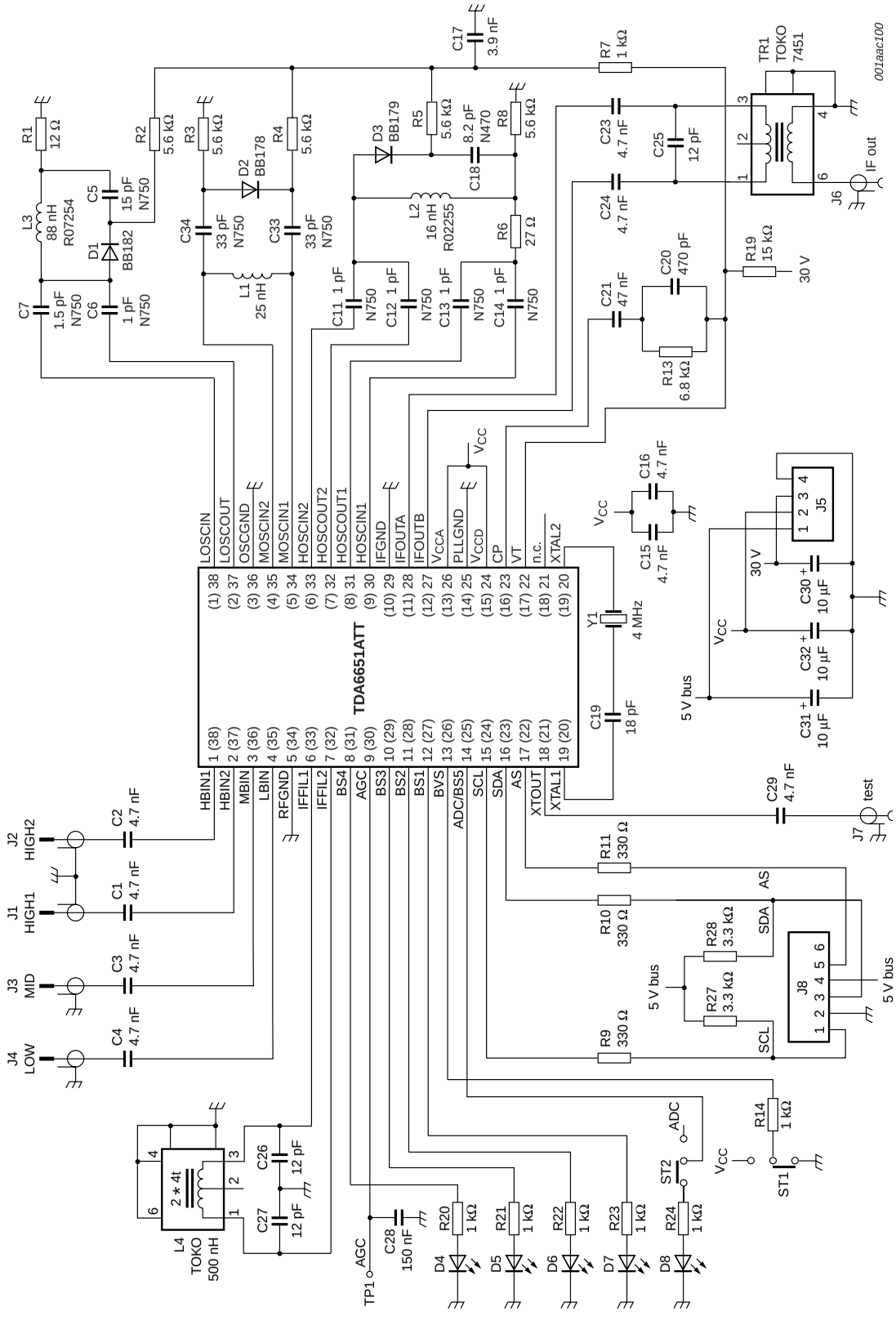
R_{pu} is the pull-up resistor between the DC supply source (or the DC-to-DC converter output) and the tuning line (R19 in Figure 27 to Figure 30).

I_{CP} is the charge pump current in use.



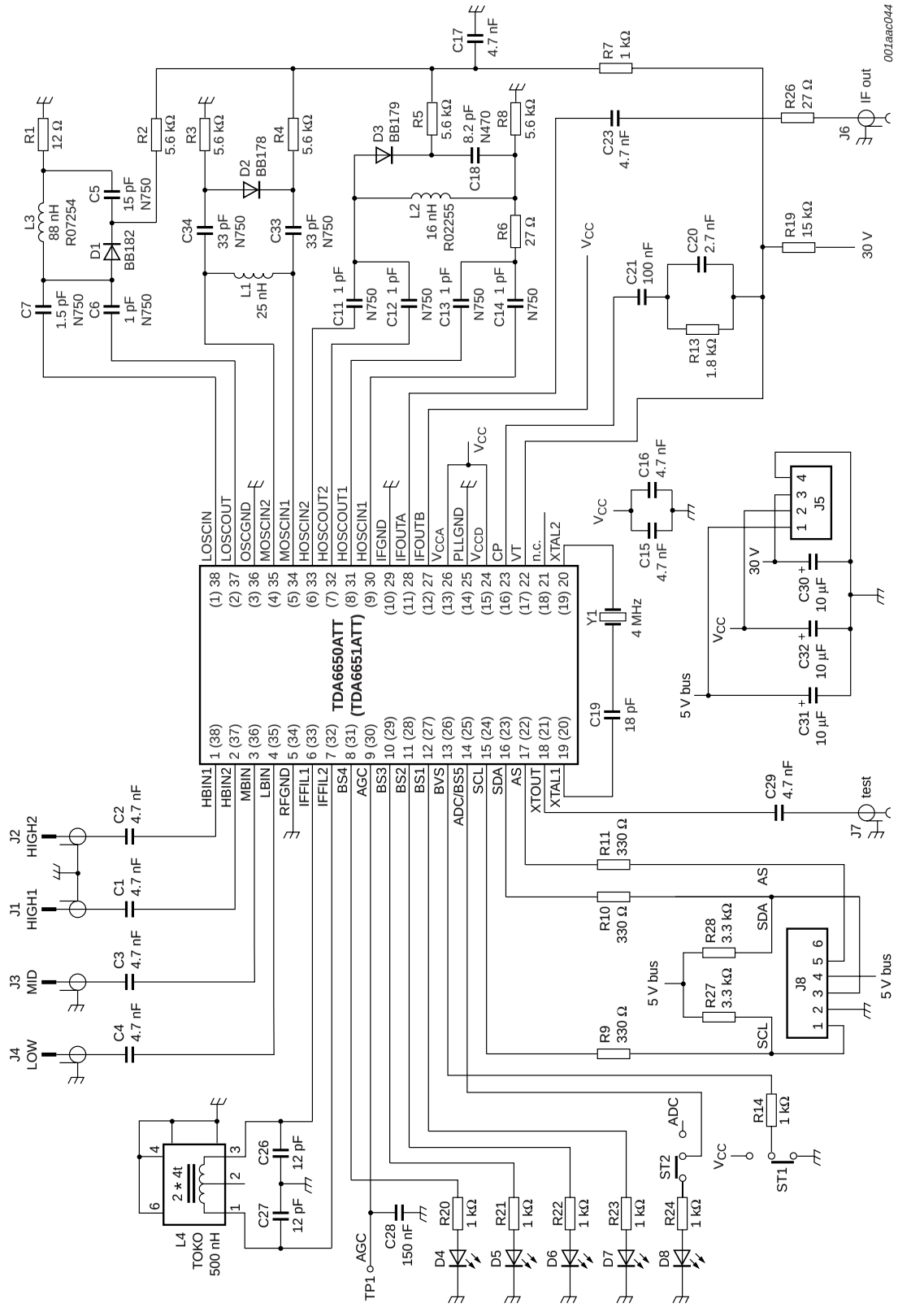
The pin numbers in parenthesis represent the TDA6651ATT.

Fig 27. Measurement circuit for digital application, with asymmetrical IF output and ISDB-T compliant loop filter



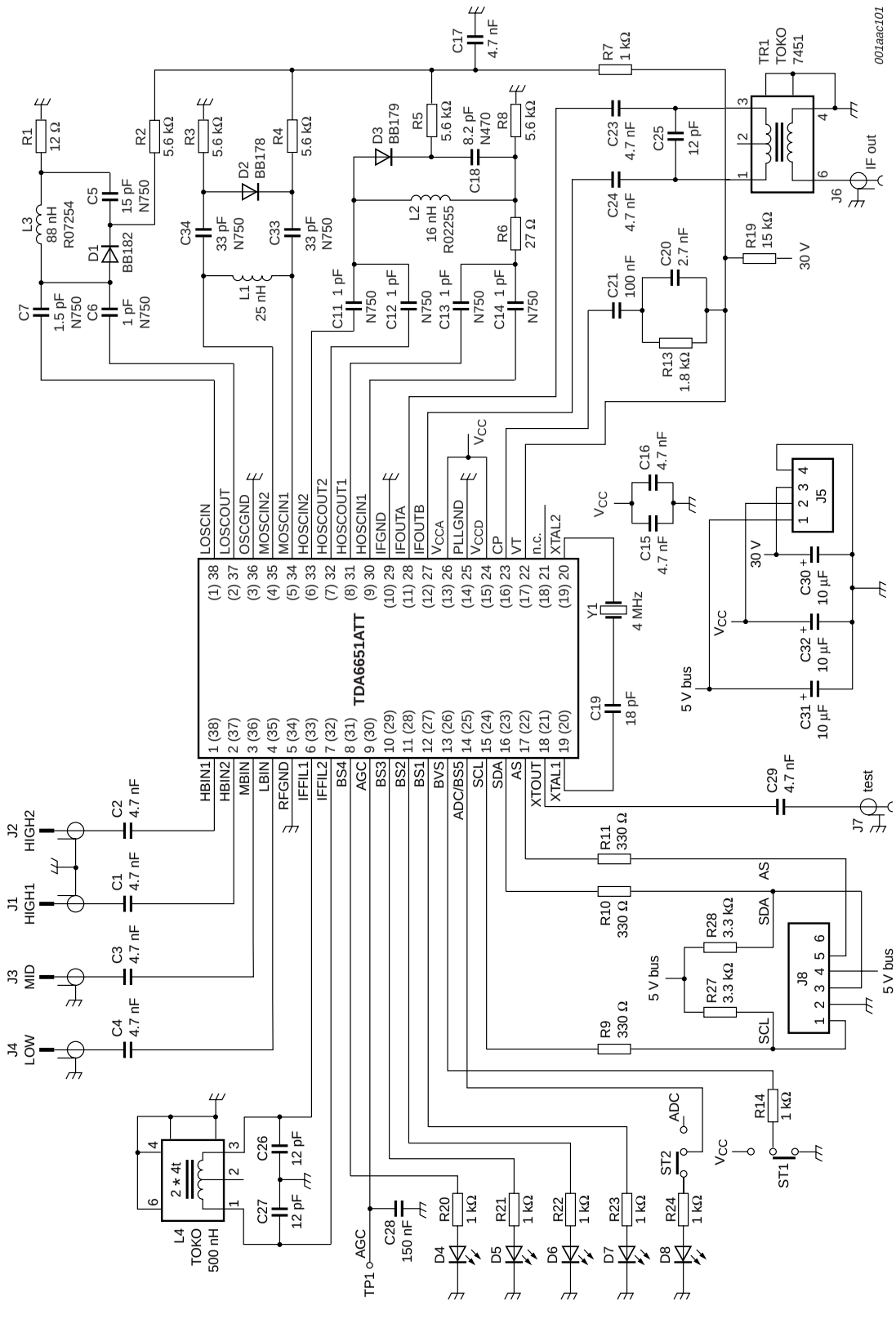
The pin numbers in parenthesis represent the TDA6651ATT.

Fig 28. Measurement circuit for digital application, with symmetrical IF output and ISDB-T compliant loop filter



The pin numbers in parenthesis represent the TDA6651ATT.

Fig 29. Measurement circuit for hybrid application, with asymmetrical IF output and loop filter for NTSC Japan and ISDB-T standards



The pin numbers in parenthesis represent the TDA6651ATT.

Fig 30. Measurement circuit for hybrid application, with symmetrical IF output and loop filter for NTSC Japan and ISDB-T standards

13. Application information

13.1 Tuning amplifier

The tuning amplifier is capable of driving the varicap voltage without an external transistor. The tuning voltage output must be connected to an external load of 15 kΩ which is connected to the tuning voltage supply rail. The loop filter design depends on the oscillator characteristics and the selected reference frequency as well as the required PLL loop bandwidth.

Applications with the TDA6650ATT; TDA6651ATT have a large loop bandwidth, in the order of a few tens of kHz. The calculation of the loop filter elements has to be done for each application, it depends on the reference frequency and charge pump current.

13.2 Crystal oscillator

The TDA6650ATT; TDA6651ATT needs to be used with a 4 MHz crystal in series with a capacitor with a typical value of 18 pF, connected between pin XTAL1 and pin XTAL2. Philips crystal 4322 143 04093 is recommended. When choosing a crystal, take care to select a crystal able to withstand the drive level of the TDA6650ATT; TDA6651ATT without suffering from accelerated ageing. For optimum performances, it is highly recommended to connect the 4 MHz crystal without any serial resistance.

The crystal oscillator of the TDA6650ATT; TDA6651ATT should not be driven (forced) from an external signal. Do not use the signal on pins XTAL1 or XTAL2, or the signal present on the crystal, to drive an external IC or for any other use as this may dramatically degrade the phase noise performance of the TDA6650ATT; TDA6651ATT.

13.3 Examples of I²C-bus program sequences

Table 21 to Table 26 show various sequences where:

S = START

A = acknowledge

P = STOP.

The following conditions apply:

LO frequency is 800 MHz

f_{comp} = 142.86 kHz

N = 5600

BS3 output port is on and all other ports are off: thus the high band is selected

Charge pump current I_{CP} = 600 µA

Normal mode, with XTOUT buffer on

I_{AGC} = 220 nA

AGC take-over point is set to 112 dBµV (p-p)

Address selection is adjusted to make address C2 valid.

To fully program the device, either sequence of Table 21 or Table 22 can be used, while other arrangements of the bytes are also possible.

Table 21. Complete sequence 1

Start	Address byte		Divider byte 1		Divider byte 2		Control byte 1[1]		Control byte 2		Control byte 1[2]		Stop
S	C2	A	15	A	E0	A	C9	A	E4	A	84	A	P

[1] Control byte 1 with bit T/A = 1, to program test bits T2, T1 and T0 and reference divider ratio bits R2, R1 and R0.

[2] Control byte 1 with bit T/A = 0, to program AGC time constant bit ATC and AGC take-over point bits AL2, AL1 and AL0.

Table 22. Complete sequence 2

Start	Address byte		Control byte 1[1]		Control byte 2		Divider byte 1		Divider byte 2		Control byte 1[2]		Stop
S	C2	A	C9	A	E4	A	15	A	E0	A	84	A	P

[1] Control byte 1 with bit T/A = 1, to program test bits T2, T1 and T0 and reference divider ratio bits R2, R1 and R0.

[2] Control byte 1 with bit T/A = 0, to program AGC time constant bit ATC and AGC take-over point bits AL2, AL1 and AL0.

Table 23. Sequence to program only the main divider ratio

Start	Address byte		Divider byte 1		Divider byte 2		Stop
S	C2	A	15	A	E0	A	P

Table 24. Sequence to change the charge pump current, the ports and the test mode. If the reference divider ratio is changed, it is necessary to send the DB1 and DB2 bytes

Start	Address byte		Control byte 1[1]		Control byte 2		Stop
S	C2	A	C9	A	E4	A	P

[1] Control byte 1 with bit T/A = 1, to program test bits T2, T1 and T0 and reference divider ratio bits R2, R1 and R0.

Table 25. Sequence to change the test mode. If the reference divider ratio is changed, it is necessary to send the DB1 and DB2 bytes

Start	Address byte		Control byte 1[1]		Stop
S	C2	A	C9	A	P

[1] Control byte 1 with bit T/A = 1, to program test bits T2, T1 and T0 and reference divider ratio bits R2, R1 and R0.

Table 26. Sequence to change the charge pump current, the ports and the AGC data

Start	Address byte		Control byte 1[1]		Control byte 2		Stop
S	C2	A	82	A	E4	A	P

[1] Control byte 1 with bit T/A = 0, to program AGC time constant bit ATC and AGC take-over point bits AL2, AL1 and AL0.

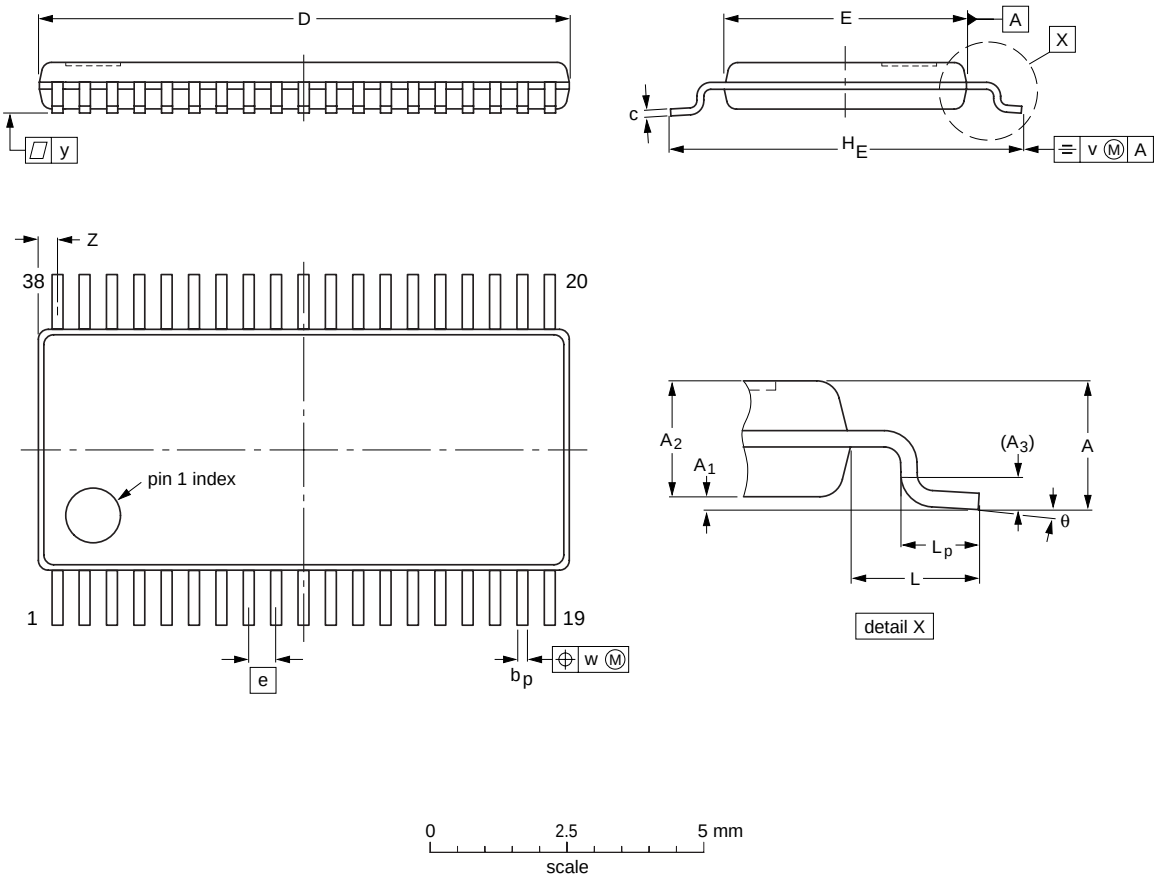
Table 27. Sequence to change only the AGC data

Start	Address byte		Control byte 1[1]		Stop
S	C2	A	84	A	P

[1] Control byte 1 with bit T/A = 0, to program AGC time constant bit ATC and AGC take-over point bits AL2, AL1 and AL0.

14. Package outline

TSSOP38: plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm **SOT510-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.27 0.17	0.20 0.09	9.8 9.6	4.5 4.3	0.5	6.4	1	0.7 0.5	0.2	0.08	0.08	0.49 0.21	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT510-1		MO-153				~~03-02-18~~ 05-11-02

Fig 31. Package outline SOT510-1 (TSSOP38)

15. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

16. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 32) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 28 and 29

Table 28. SnPb eutectic process (from J-STD-020C)

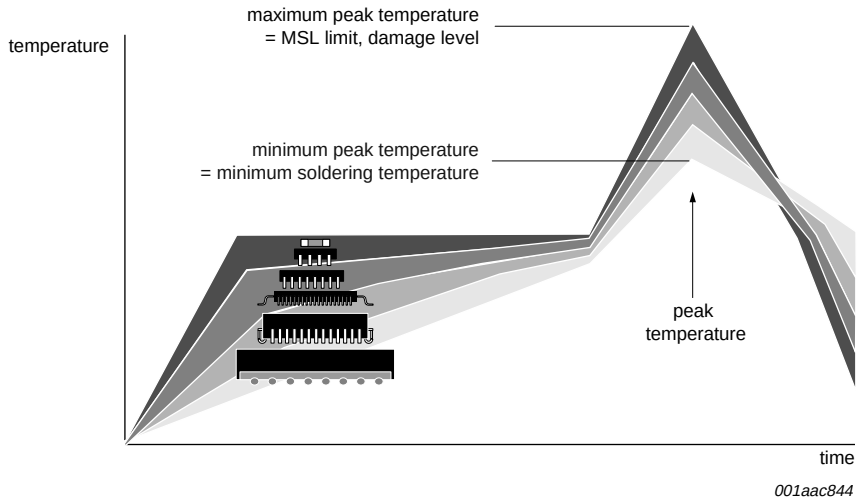
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 29. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 32.



MSL: Moisture Sensitivity Level

Fig 32. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 30. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
ISDB-T	Integrated Services Digital Broadcasting - Terrestrial
NTSC	National Telecommunications Standards Committee
PLL	Phase-Locked Loop
PMOS	Positive Channel Metal Oxide Semiconductor
QAM	Quadrature Amplitude Modulation
VCO	Voltage-Controlled Oscillator
VCR	Video Cassette Recorder

18. Revision history

Table 31. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA6650ATT_6651ATT_2	20070202	Product data sheet	-	TDA6650ATT_6651ATT_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Created Table 1 and updated Table 3 and 20 with new type numbers, emphasizing the different types for hybrid and digital only applications. • Two values changed in Table 20; page 27 $V_{AGC} < V_{CC}$ replaced with $V_{AGC} < 3.5$ V and for $V_{o(dis)}$ new minimum value of 3.3 V added.			
TDA6650ATT_6651ATT_1 (9397 750 14179)	20041214	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contents

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