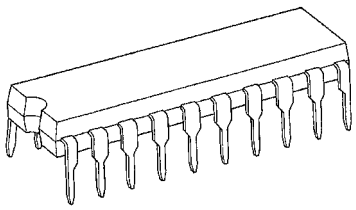
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC90A49P,TC90A49F

3LINE DIGITAL Y / C SEPARATOR IC (MULTICOLOR TYPE)

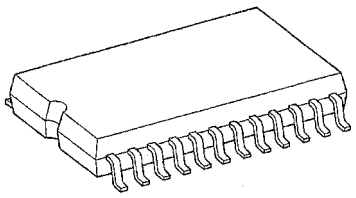
The TC90A49P / F is a 3-line digital Y / C (luminance / chrominance) separation IC for PAL, NTSC, M-PAL and N-PAL format.

TC90A49P



DIP20-P-300-2.54A

TC90A49F



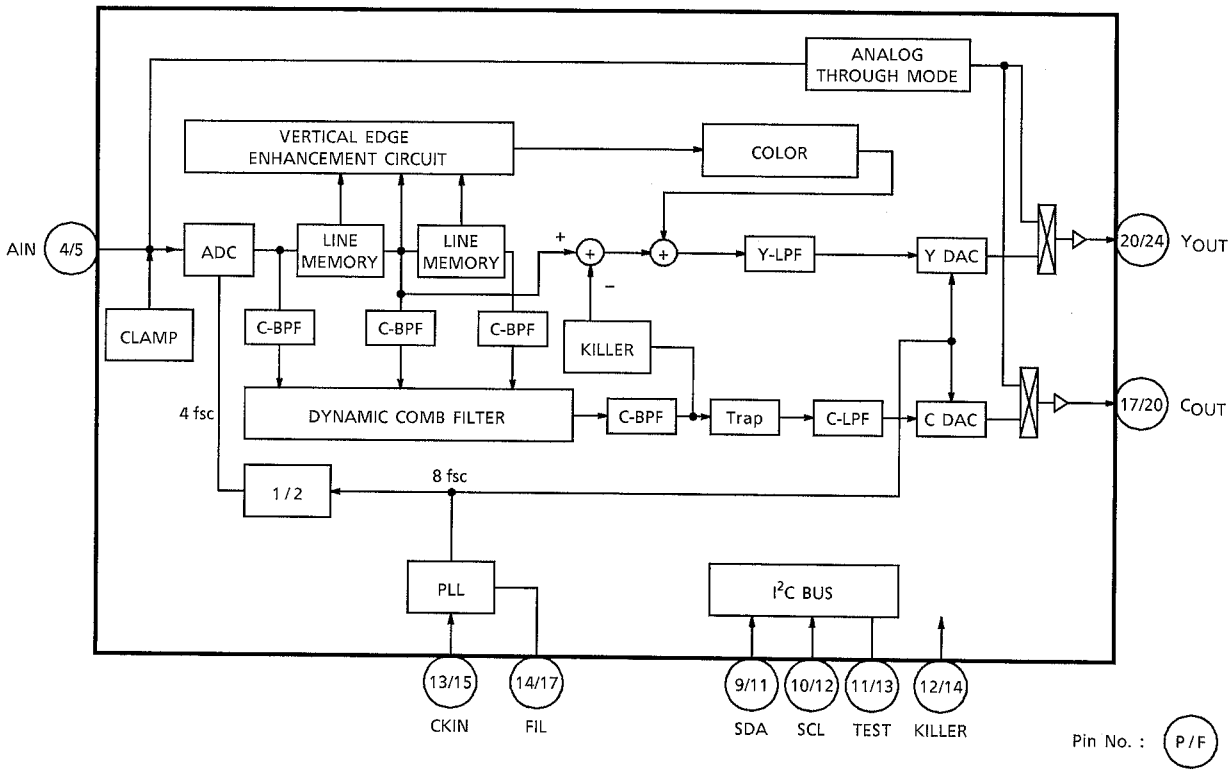
SOP24-P-450-1.27B

Weight
DIP20-P-300-2.54A : 1.11 g (Typ.)
SOP24-P-450-1.27B : 0.44 g (Typ.)

FEATURES

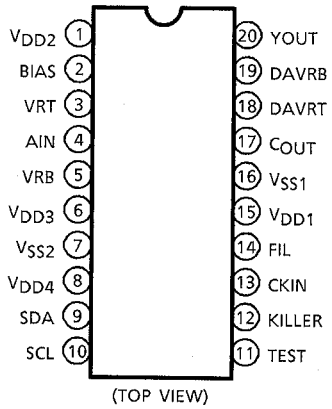
- TV format : NTSC (3.58), PAL, M-PAL, and N-PAL
- Dynamic comb filter
- Vertical edge enhancement circuit
- PLL 8 × multiplier circuit
- Internal 8-bit 4 fsc AD converter
- Internal 8-bit precision 8 fsc DA converter (2 ch)
- Sync tip clamp circuit
- Internal 4H-line memory
- I^2C bus interface
- Package : DIP 20-pin and SOP 24-pin
- 5 V single power supply

BLOCK DIAGRAM

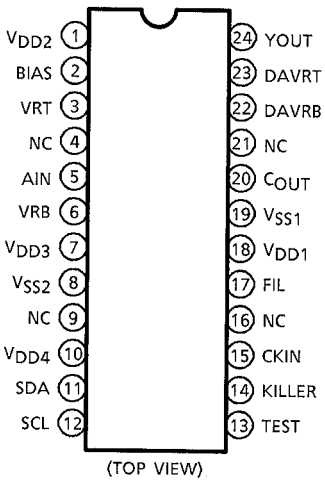


PIN ASSIGNMENT

TC90A49P

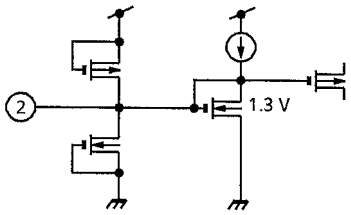
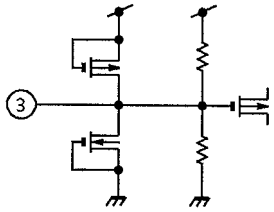
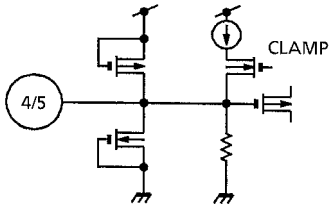
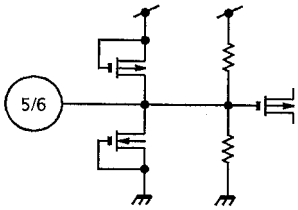
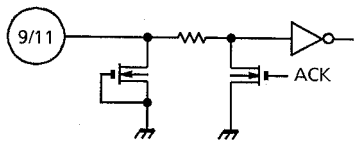
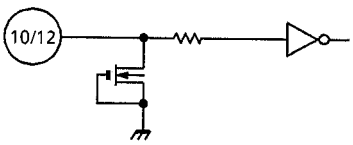


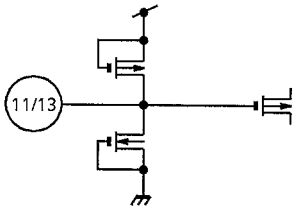
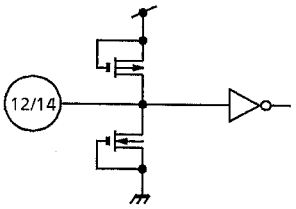
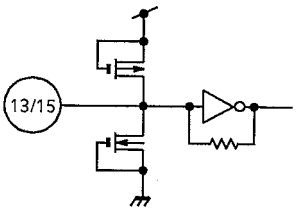
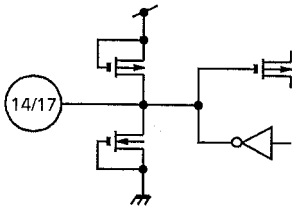
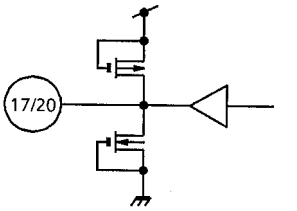
TC90A49F

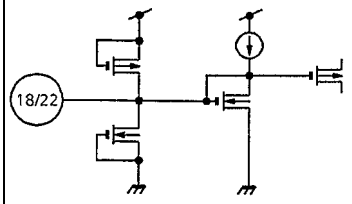
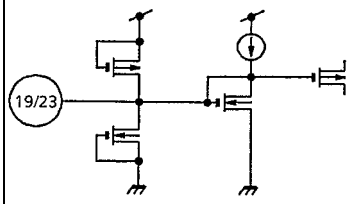
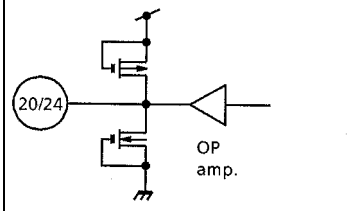


The NC which was writting in PIN ASSIGNMENT must use the open condition.

PIN DESCRIPTION (no. before / indicates DIP package pin no. no. after / indicates SOP package pin no.)

PIN No.	PIN NAME	FUNCTION	I / O	INTERFACE
1	V_{DD2}	ADC and DAC analog power supply.	–	–
2	BIAS	ADC bias voltage. Stabilize by attaching a 0.01μF capacitor.	–	
3	VRT	ADC input range D upper limit voltage. Stabilize by attaching a 0.01μF capacitor.	–	
4 / 5	AIN	ADC input. Inputs 1.0 V_{p-p} video signal. Sync tip clamp is performed.	I	
5 / 6	VRB	ADC input range D lower limit voltage. Stabilize by attaching a 0.01μF capacitor.	–	
6 / 7	V_{DD3}	ADC and DAC logic power supply.	–	–
7 / 8	V_{SS2}	Logic and internal DRAM GND (digital).	–	–
8 / 10	V_{DD4}	Internal DRAM power supply.	–	–
9 / 11	SDA	I^2C BUS SDA	I / O	
10 / 12	SCL	I^2C BUS SCL	I	

PIN No.	PIN NAME	FUNCTION	I / O	INTERFACE
11 / 13	TEST	Shipment test mode switch or I^2C bus setting reset pin. When High, test mode, setting all I^2C bus settings to 0. Hold High for at least 100μs. Send I^2C bus settings when this pin is Low.	I	
12 / 14	KILLER	Y signal comb function ON / OFF switch. When High, comb OFF. When Low, comb ON. When [data 3 : bit 0] is 1, used as vertical edge enhancement circuit ON / OFF switch.	I	
13 / 15	CKIN	Clock input pin. Pin 13 put a sine wave which is locked to the frequency of the burst signal in the input video signal. Amplitude is 300 mV $_{p-p}$ to 2 V_{p-p}. Input as high an amplitude as possible without affecting peripheral circuits.	I	
14 / 17	FIL	Connect the APC filter in the 8 fsc PLL circuit.	−	
15 / 18	V_{DD1}	PLL power supply.	−	−
16 / 19	V_{SS1}	ADC, DAC, and PLL GND (analog).	−	−
17 / 20	C_{OUT}	Outputs chrominance signal. External simple LPF for clock elimination recommended.	O	

PIN No.	PIN NAME	FUNCTION	I / O	INTERFACE
18 / 22	DAVRT	DAC output range D upper limit voltage. Stabilize by attaching a 0.01μF capacitor.	–	
19 / 23	DAVRB	DAC output range D lower limit voltage. Stabilize by attaching a 0.01μF capacitor.	–	
20 / 24	Y_{OUT}	Outputs luminance signal. External simple LPF for clock elimination recommended.	O	

FUNCTION DESCRIPTION (Pin no. in this section refers to DIP package pin no.)

1. AD converter (ADC)

High-speed 8-bit AD converter. The input dynamic range is 1.3 V_{p-p} (max) = 256 steps. They recommends input of video signals of 1.0 V_{p-p} (from sync tip level to 100% white level).

2. Clamp circuit

Performs sync tip clamp of the input video signal. The clamp level is determined internally to use the ADC dynamic range efficiently.

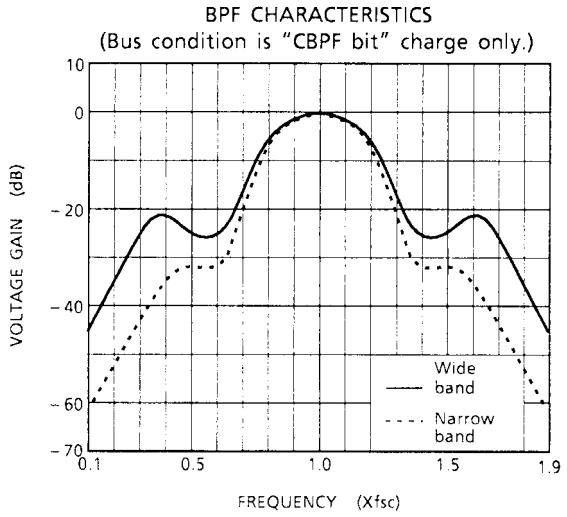
3. Line memory

Incorporates DRAM-resident, four 1-H delay circuits. Combination of delay circuits and delay times are determined according to the signal format selected by the I^2C bus.

TV Format	NTSC	PAL	N-PAL	M-PAL
Delay Amount (clock)	910	1135	917	909

4. Band pass filter (BPF)

Extracts the chrominance signal from the line-memory-delayed composite video signal. The same filter is used by NTSC, PAL, M-PAL, and N-PAL formats. The center frequency is fsc. The characteristics differ depending on the TV format. BPFs are provided for both input and output sides of the dynamic comb filter. The input side can be set to a wide band. The output side can be set to either a wide or a narrow band using the I^2C bus control.



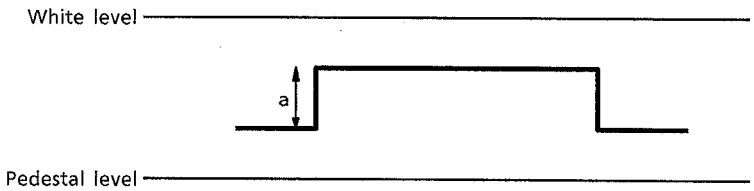
5. Dynamic comb filter (DCF)

Using Toshiba's original decision logic, detects a correlation of the three consecutive vertical lines for NTSC, every other three lines for PAL, and extracts the chrominance signal accordingly.

6. Vertical edge enhancement circuit

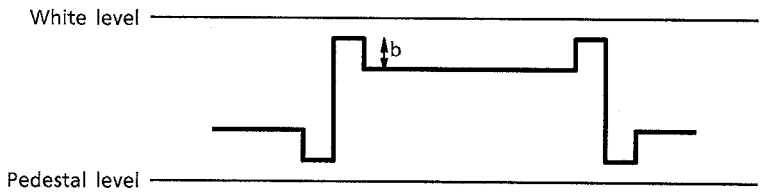
Generates edge components in proportion to the luminance differential signal of the three consecutive vertical lines and adds the components to the luminance signal output. There are eight enhancement levels selected by the I^2C bus. The coring circuit eliminates differential signals caused by noise ; thus, increase in noise due to edge enhancement is reduced. Signals lower than the pedestal level due to the addition of the edge enhancement signal may be generated ; however, such signals are eliminated by the pedestal clip circuit at a later stage. Therefore, there is no adverse effect on the sync processor circuit. The coring circuit regards small edge components as noise and does not perform enhancement.

(1) Input signal with edge component



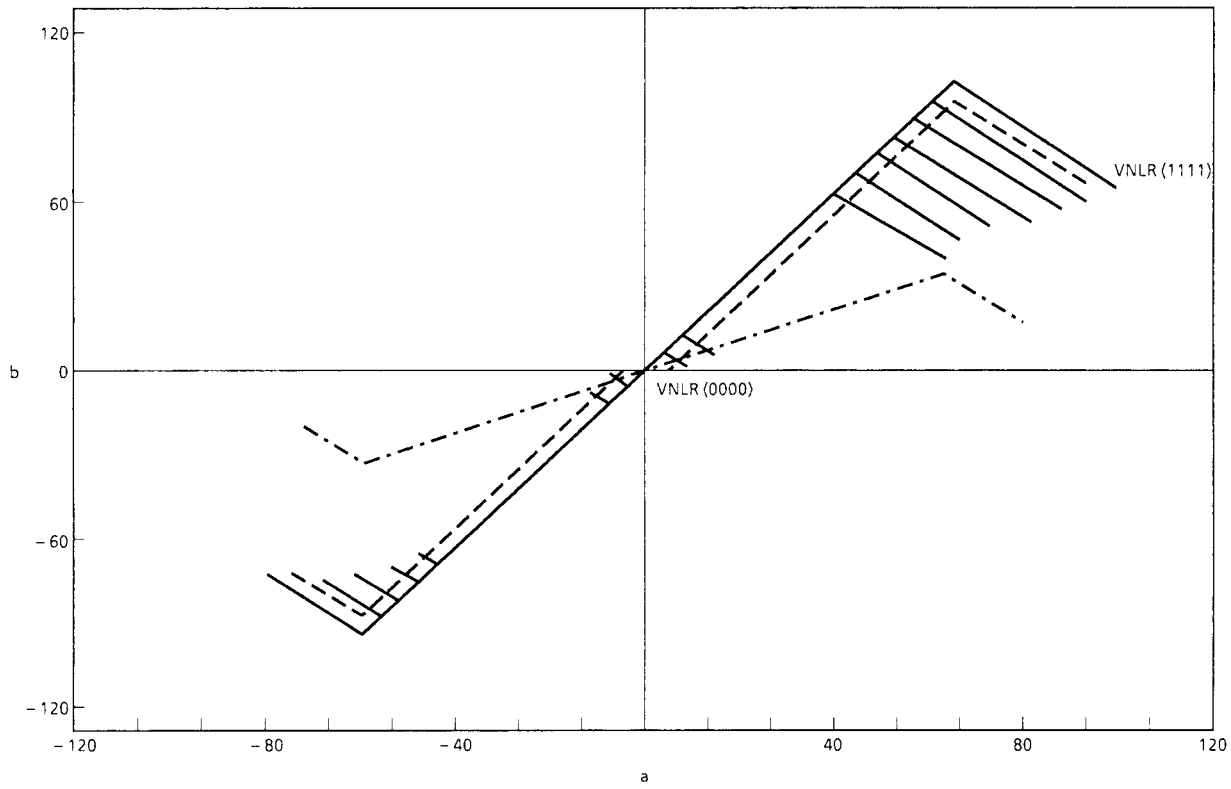
a : Vertical edge level

(2) Output signal



b : Enhance level

Vertical edge enhancement characteristic

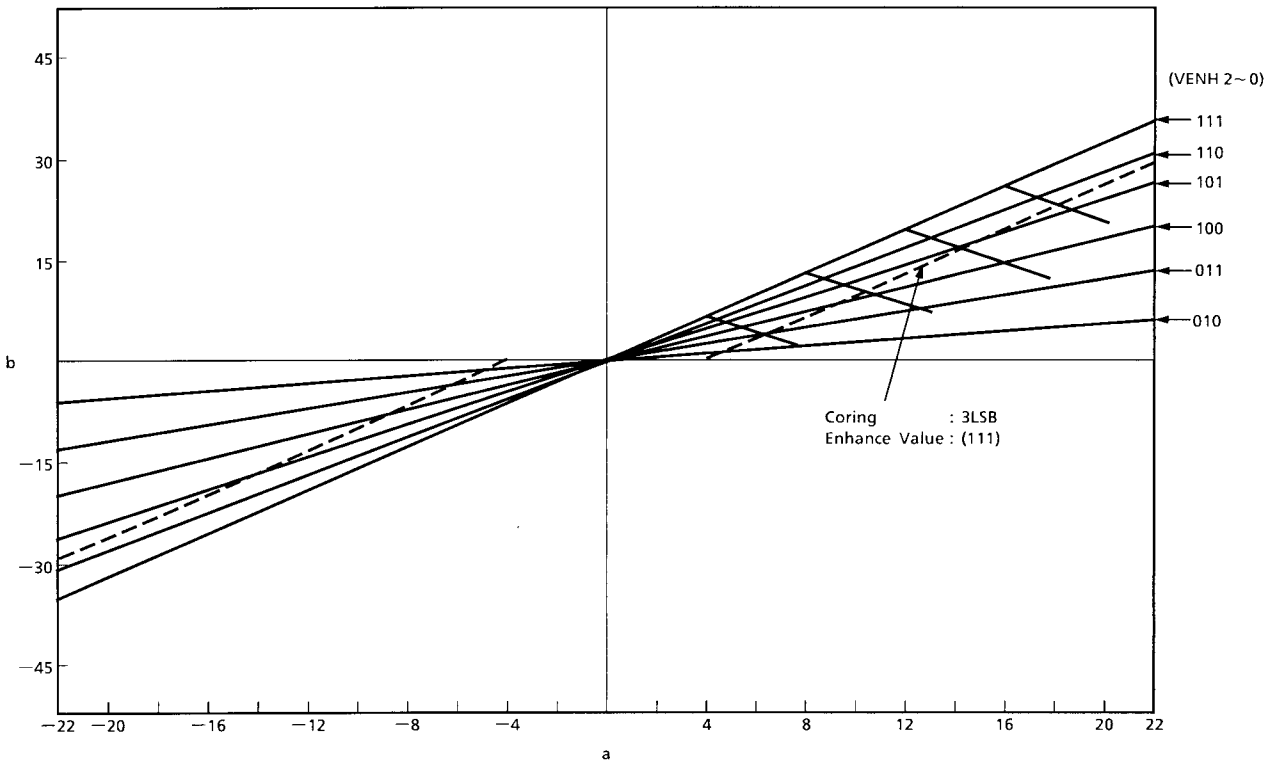


Enhance Value : 111 (+1.5)
Non liner point : 0000~1111
Coring : 0LSB

Enhance Value : 111 (+1.5)
Non liner point : 1111
Coring : 3LSB

Enhance Value : 011 (+0.5)
Non liner point : 1111
Coring : 0LSB

Vertical edge enhancement characteristic (Zoom)



Relation between difference a in luminous signal to be enhanced during 1H and applied enhance amount b.
Both a and b are LSB amounts. 1LSB ≒ 0.005 V
Coring : 0LSB

—— Enhance Value : (111) —— (110) —— (101)

—— Enhance Value : (100) —— (011) —— (010) —— (001)

Coring : 3LSB
— — — Enhance Value : (111)

7. PLL 8 × multiplier circuit

Multiplies by eight the input subcarrier signal which is locked to the frequency of burst signal to generate 8 fsc and 4 fsc system clocks.

8. DA converter (DAC)

The Y / C signal separated using the 4 fsc clock as the basic clock is over-sampled by the 8 fsc clock, then DA-converted.

9. Color killer circuit

When the input video signal is a monochrome image, this circuit enables effective use of the luminance signal information regardless of whether there is a burst signal. It does this by preventing the chroma signal output from the comb filter from being subtracted from the luminance signal.
While the VBI signal is active it is better not to use the comb function. Setting the KILLER pin to High at this time enables the use of character multiplex and other signals from the Y output unchanged.

10. RESET / TEST pin

Switches between normal comb operation and test operation. Also used for I^2C bus reset input. Change in voltage from Low to High triggers a reset. Normal use is Low.

11. I^2C bus interface

Some functions and setting values can be selected using the I^2C bus. The data transfer format conforms to the Philips I^2C bus format.

Data transfer format

S	Slave address (8 bit)	A	DATA1	A	DATA2	A	DATA3	A	P

S : start condition A : acknowledge P : end condition
Slave address : B4 (HEX)

12. I^2C bus control contents : When a reset signal is input, all the following bits are zero-cleared.

	MSB bit7	bit6	bit5	bit4	bit3	bit2	bit1	LSB bit0
DATA1	$MODE_2$	$MODE_1$	$MODE_0$	$VENH_2$	$VENH_1$	$VENH_0$	PDSOFF	CB
DATA2	$VNLR_3$	$VNLR_2$	$VNLR_1$	$VNLR_0$	$GSEL_1$	$GSEL_0$	COR_1	COR_0
DATA3	TRAP	CHTRAP	Fixed to 0	CBPF	Fixed to 0	Fixed to 0	Fixed to 0	ENHOFF

Mode 2 to Mode 0 : Select video signal format.

000 : Analog Through Mode 001 : M-PAL 010 : N-PAL 011 : PAL 100 : NTSC

When Analog Through mode is selected, input video signals are output to Yout and Cout unchanged. In Analog Through mode, the delay time for output signals differs from those used for other modes. Therefore, when changing modes to Analog Through mode, to decide the input signal format, provide some delay time until an image is displayed.

There is a case where a 1 LSB error voltage at frequency fsc is multiplexed with the output signal. When deciding the input signal format, to avoid an erroneous decision due to fsc leakage, be careful when setting the decision sensitivity (killer sensitivity).

When the input signal is SECAM or 4.43 NTSC, select Analog Through mode. A separate BELL filter or a BPF is required.

$VENH_2$ to $VENH_0$: Set vertical enhancer gain.

000 : (+0.0) to 111 : (+1.5)

PDSOFF : Switches pedestal clip ON / OFF after vertical edge enhancement circuit.

0 : ON 1 : OFF

CB : Sets Color Killer mode to ON / OFF

0 : Y signal comb function ON

1 : Y signal comb function OFF (Same composite signal is output from Y and C pins.)

$VNIR_3$ to $VNIR_0$: Set vertical enhancer non-linear point.

0000 : 4 LSB (internal set of IC to 4 LSB) to 1111 : 64 LSB (internal set of IC to 64 LSB)

$GSEL_1$: Sets Y output horizontal peaking gain.

0 : 1.5 dB 1 : 3.0 dB

$GSEL_0$: Switches Y output horizontal peaking ON / OFF.

0 : ON 1 : OFF

COR_1 and COR_0 : Set vertical enhancer coring level.

00 : 0 LSB to 11 : 3 LSB

TRAP : Sets C output 1 / 2 fsc trap ON / OFF.

0 : ON 1 : OFF

CHTRAP : Sets C output trap gain.

0 : −24 dB 1 : −16 dB

CBPF : Switches C output BPF ON / OFF (BPF characteristic after dynamic comb filter output).

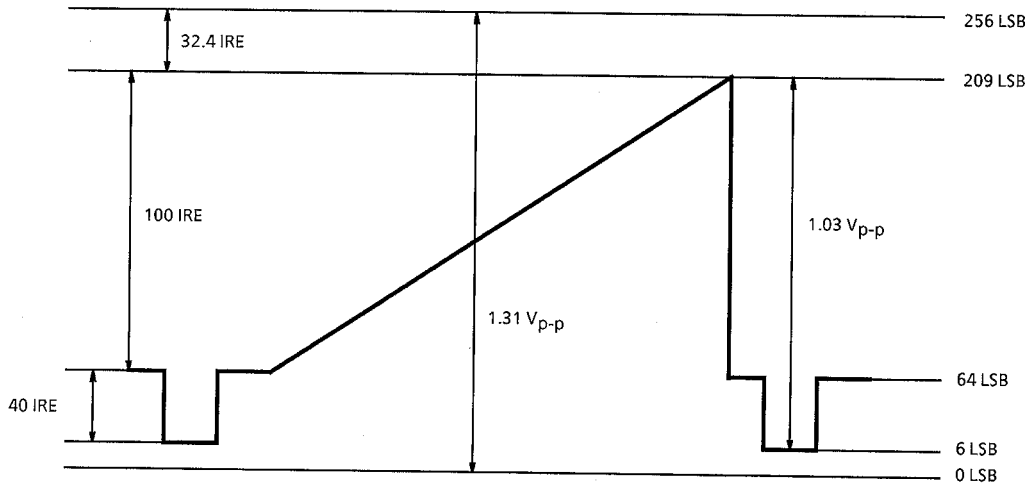
0 : Narrow band = BPF → ON 1 : Wide band = BPF → OFF

ENHOFF : Sets KILLER pin function.

0 : Comb ON / OFF 1 : Comb ON / OFF and vertical edge enhancement ON / OFF

Signal level inside the IC

The sync tip of the input video signal is clamped to an internal level equivalent to 6 LSB. When a signal amplitude of 1.0 V is equivalent to 140 IRE, 100% white status becomes an internal level of 209 LSB. At this time, the input dynamic range of 256 LSB is equivalent to 1.3 $V_{p\text{-}p}$.



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC			SYMBOL	RATING	UNIT
Power Supply Voltage			V_{DD}	V_{SS} + 6.0	V
Pin Voltage		Max	V_{inmax}	V_{DD} + 0.3	V
		Min	V_{inmin}	V_{SS} − 0.3	
Power Dissipation	49P (Note)		P_D	550	mW
Power Dissipation	49F (Note)		P_D	458	mW
Storage Temperature			T_{stg}	−55~125	°C

(Note) : Ta = 70°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
Digital Input Voltage	V_{DIN}	0	−	V_{DD}	V	
Operating Temperature	T_{opr}	−10	−	70	°C	

ELECTRICAL CHARACTERISTICS (Pin no. corresponds to DIP package pin no.)

DC CHARACTERISTICS

(Ta = 25°C, V_{DD} = 5.0 V, CKIN = 3.58 MHz, 1.0 V_{p-p} input, A_{in} = no input, in all modes)

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Power Supply Current	I_{DD}	40	75	85	mA	Supply current, in all modes
Pin Voltage	V_2	0.5	1.3	2.1	V	Pin 2 : ADC bias
	V_3	2.85	3.15	3.48	V	Pin 3 : AD range D upper limit
	V_4	1.65	1.85	2.02	V	Pin 4 : A_{in} input pin voltage
	V_5	1.65	1.85	2.02	V	Pin 5 : AD range D lower limit
	V_{18}	2.85	3.15	3.48	V	Pin 18 : DA range D upper limit
	V_{19}	1.65	1.85	2.02	V	Pin 19 : DA range D lower limit

DC CHARACTERISTICS

(Ta = 25°C, V_{DD} = 5.0 V, CKIN = each fsc, A_{in} = no input, unless otherwise specified, in all modes)

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Output Voltage	Y_{OUT}	1.65	1.85	2.02	V	Pin 20 : Y_{OUT}
	C_{OUT}	1.65	1.85	2.02	V	Pin 17 : C_{OUT}

DC CHARACTERISTICS

(Ta = 25°C, V_{DD} = 5.0 V, CKIN = each fsc, A_{in} = no input, unless otherwise specified, in all modes)

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Output Voltage	Y_{OUT}	1.65	1.85	2.02	V	Pin 20 : Y_{OUT}
	C_{OUT}	2.25	2.5	2.67	V	Pin 17 : C_{OUT}
FIL Pin (pin 14) Voltage	V_{14}	−	2.2	−	V	NTSC mode 3.579545 MHz
FIL Pin (pin 14) Voltage	V_{14}	−	2.4	−	V	PAL mode 4.433619 MHz
FIL Pin (pin 14) Voltage	V_{14}	−	2.2	−	V	M-PAL mode 3.575611 MHz
FIL Pin (pin 14) Voltage	V_{14}	−	2.2	−	V	N-PAL mode 3.582056 MHz

PLL CHARACTERISTICS

(Ta = 25°C, V_{DD} = 5.0 V, CKIN = 1.0 Vp-p input, A_{in} = no input, unless otherwise specified, in all modes)

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Pull-in Frequency Range (NTSC)	ΔfckN	−	−	±100	kHz	In relation to fsc center frequency
Pull-in Frequency Range (PAL)	ΔfckP	−	−	±100	kHz	In relation to fsc center frequency
Pull-in Frequency Range (NPAL)	ΔfckN	−	−	±100	kHz	In relation to fsc center frequency
Pull-in Frequency Range (MPAL)	ΔfckM	−	−	±100	kHz	In relation to fsc center frequency
Input Amplitude (fsc sine wave)	Vck	0.3	1.0	2.0	V_{p-p}	

DIGITAL CHARACTERISTICS (Ta = 25°C, V_{DD} = 5.0 V)

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Input Voltage	V_{IH}	4	−	−	V	Pin 9, Pin 10, Pin 12
	V_{IL}	−	−	1	V	Pin 9, Pin 10, Pin 12
Current at ACK Output	Ack	4	−	−	mA	Pin 9 VOLmax : 0.4 V

AC CHARACTERISTICS (Ta = 25°C, V_{DD} = 5.0 V, CKIN = 1.0 V_{p-p} input)

(1)Y Input (A_{in} = input, unless otherwise specified, in all modes except Analog Through Mode)

CHARACTERISTIC		SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Input D Range	AD Input Top Level	V_{ADt}	2.85	3.15	3.48	V	
	AD Input Bottom Level	V_{ADb}	1.65	1.85	2.02	V	
	AD Input Difference Between Top and Bottom	V_{AD}	−20	−	+20	mV	
Output D Range	YDA Output Top Level	V_{DAt}	2.85	3.15	3.48	V	
	YDA Output Bottom Level	V_{DAb}	1.65	1.85	2.02	V	
	YDA Output Difference Between Top and Bottom	V_{DA}	−20	−	+20	mV	
Y_{OUT} Low Frequency Gain		GY	−0.5	0.0	0.5	dB	Input / output gain measured in ADDA Through mode
Y_{OUT} Frequency Characteristic (Peaking OFF)		FW	−	4.7	−	MHz	−3 dB frequency
Y_{OUT} Frequency Characteristic (Peaking 1.5 dB)		FW1	−	6.2	−	MHz	−3 dB frequency
Y_{OUT} Frequency Characteristic (Peaking 3.0 dB)		FW2	−	6.7	−	MHz	−3 dB frequency
Y_{OUT} Comb Characteristic		Y_{com}	40	45	−	dB	Difference between comb top and bottom
Y_{OUT} Differential Accidental		L	−1	0	+1	LSB	(Reference value)
Y_{OUT} Integral Accidental		B	−3	0	+3	LSB	(Reference value)
Output Impedance		Zy	300	600	900	Ω	

(2)C Output (A_{in} = input, unless otherwise specified, in all modes except Analog Through Mode)

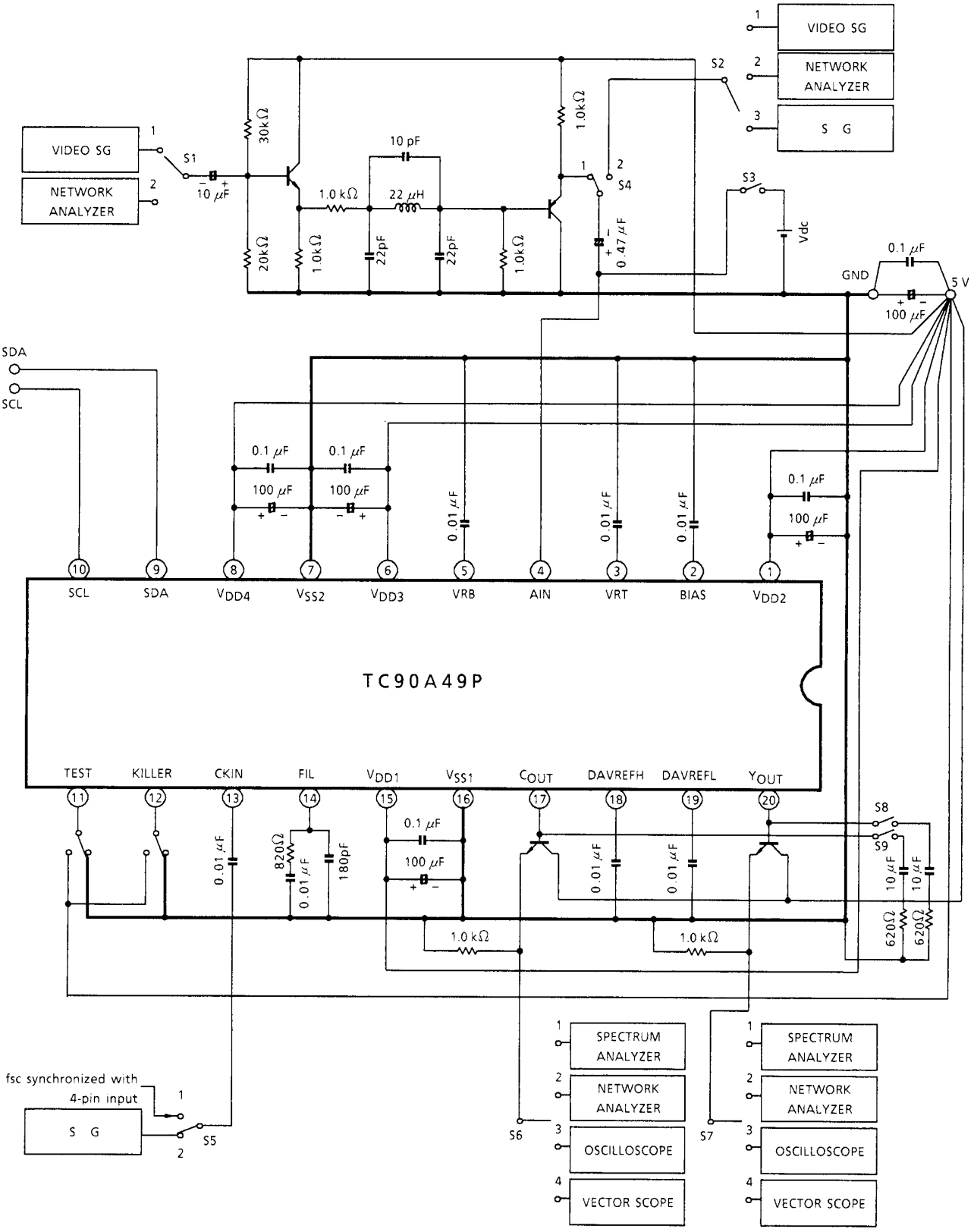
CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Output Dynamic Range	VC_{OUT}	−	1.0	1.0	V	D Range of C
C_{OUT} Gain Input	GC	−0.5	0.0	+ 0.5	dB	Output gain at comb operation
C_{OUT} Gain Comb Characteristic	C_{com}	35	40	−	dB	Difference between comb top and bottom
Differential Gain	DG	0	2	5	%	
Differential Phase	DP	0	2	5	°	
Output Impedance	Zc	300	600	900	Ω	

(3)CHARACTERISTICS BY BUS SETTING

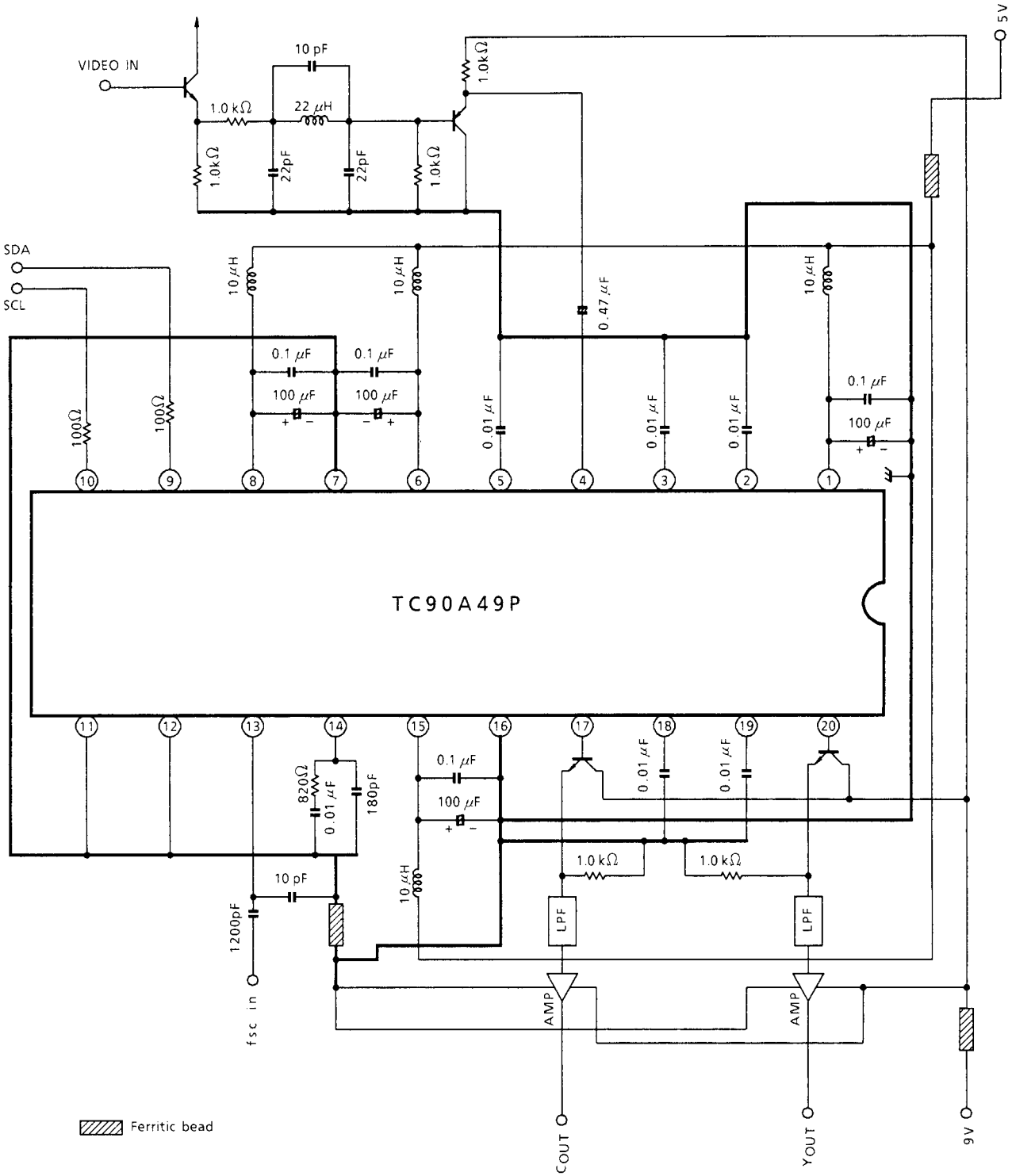
(A_{in} = input, unless otherwise specified, in all modes except Analog Through Mode)

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
C-BPF Characteristic (Wide Band)	BW_1	−	−2.5	−	dB	Attenuation at fsc −0.5 MHz
C-BPF Characteristic (Narrow Band)	BW_0	−	−3.0	−	dB	Attenuation at fsc −0.5 MHz

TEST CIRCUIT (TC90A49P)



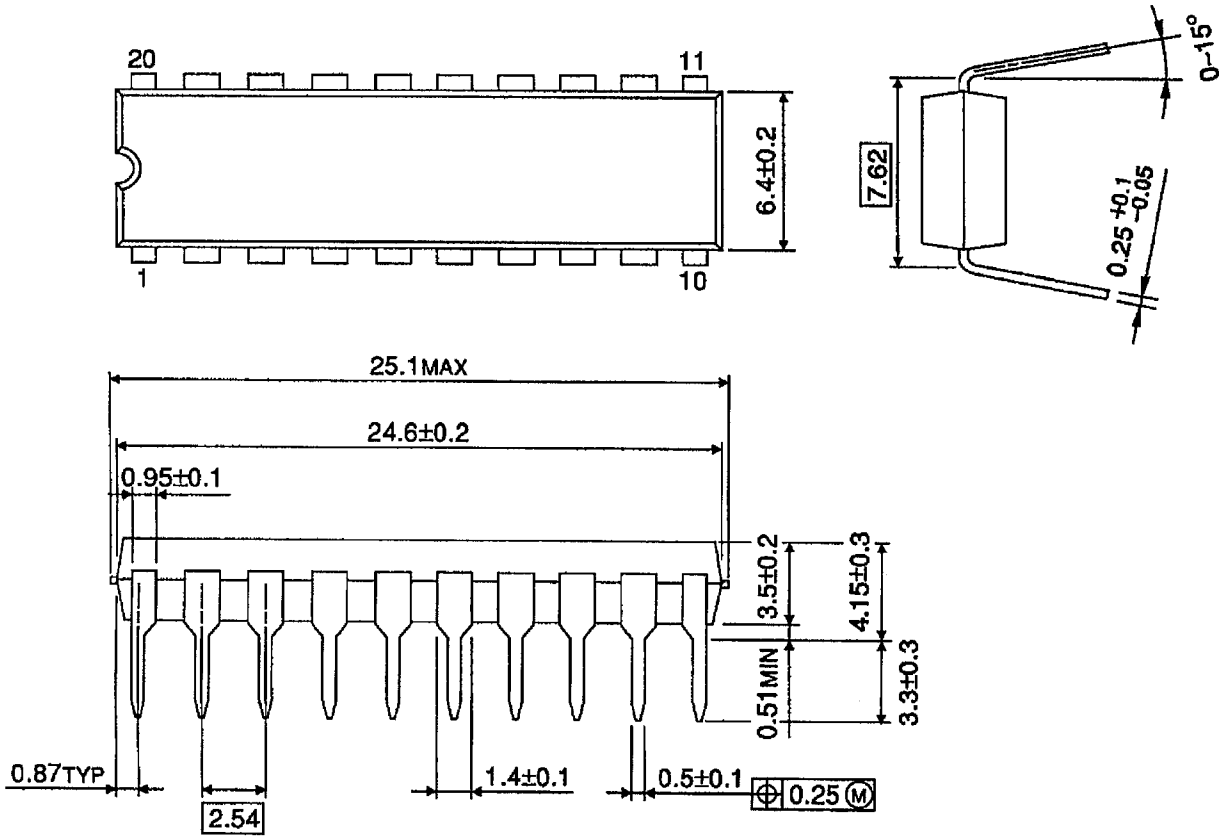
APPLICATION CIRCUIT (TC90A49P)



PACKAGE DIMENSIONS

DIP20-P-300-2.54A

Unit : mm

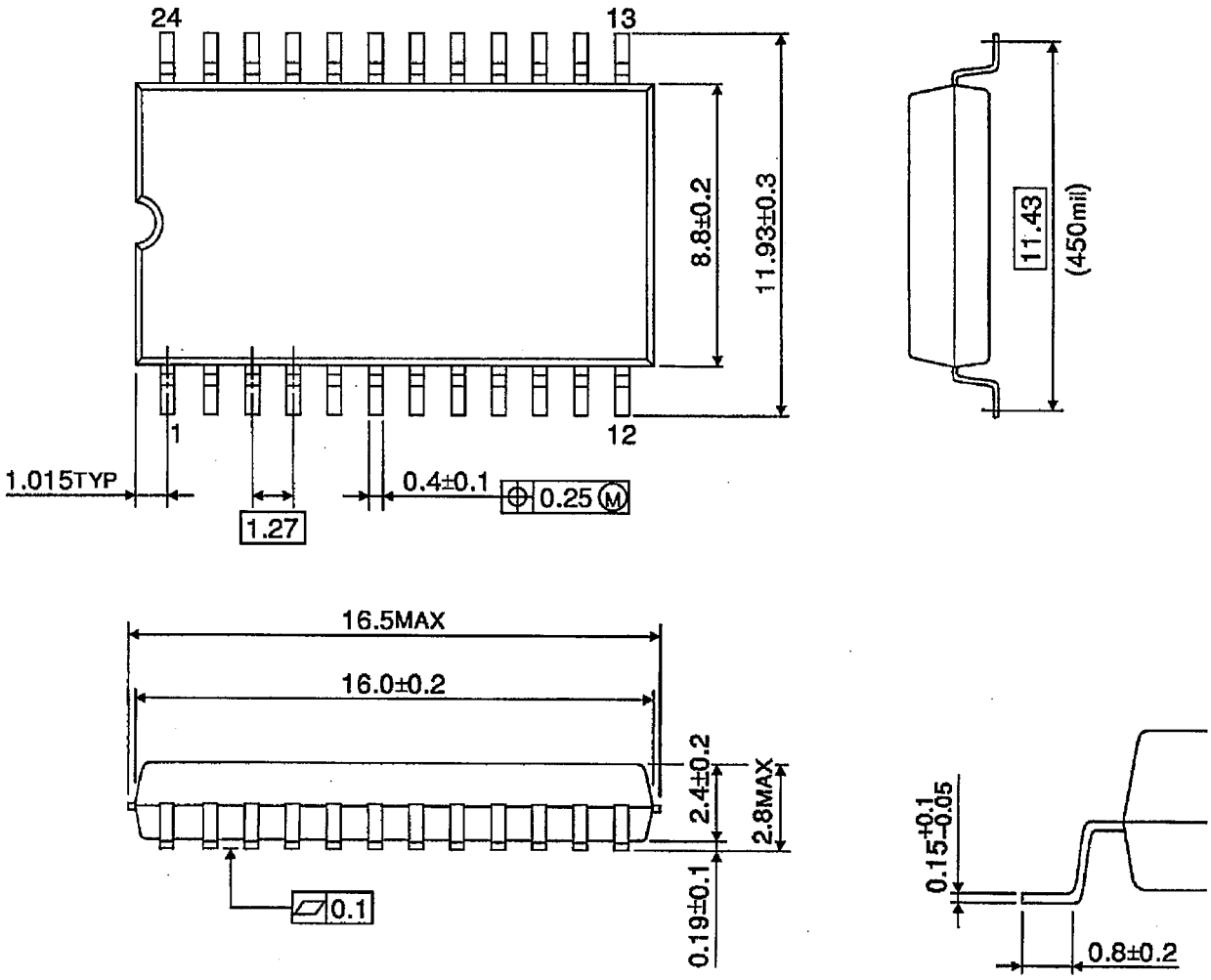


Weight : 1.11g (Typ.)

PACKAGE DIMENSIONS

SOP24-P-450-1.27B

Unit : mm



Weight : 0.44g (Typ.)