THC63LVD103

135MHz 30Bits COLOR LVDS Transmitter

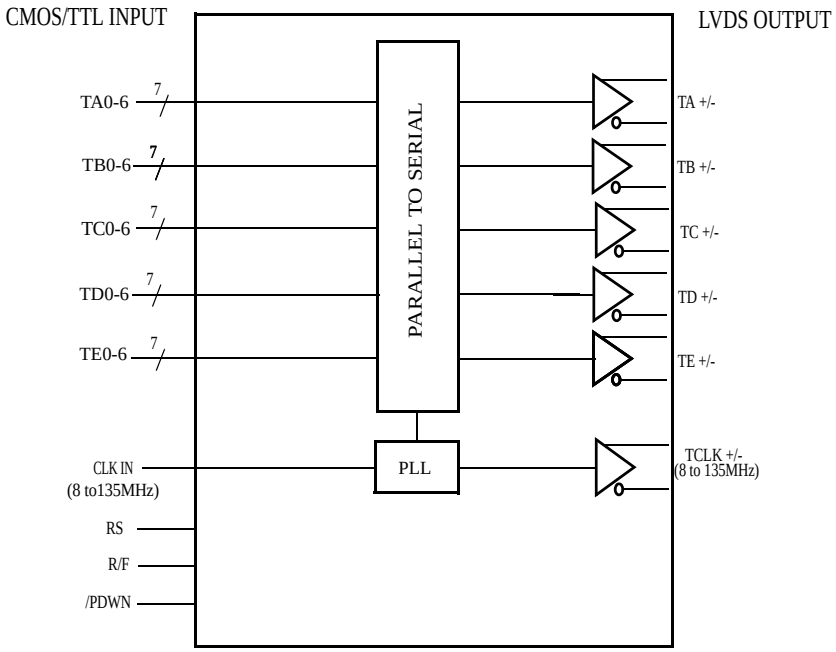
General Description

The THC63LVD103 transmitter is designed to support pixel data transmission between Host and Flat Panel Display from NTSC up to SXGA+ resolutions.
The THC63LVD103 converts 35bits of CMOS/TTL data into LVDS(Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 135MHz, 30bits of RGB data and 5bits of timing and control data (HSYNC, VSYNC, DE, CNTL1, CNTL2) are transmitted at an effective rate of 945Mbps per LVDS channel.

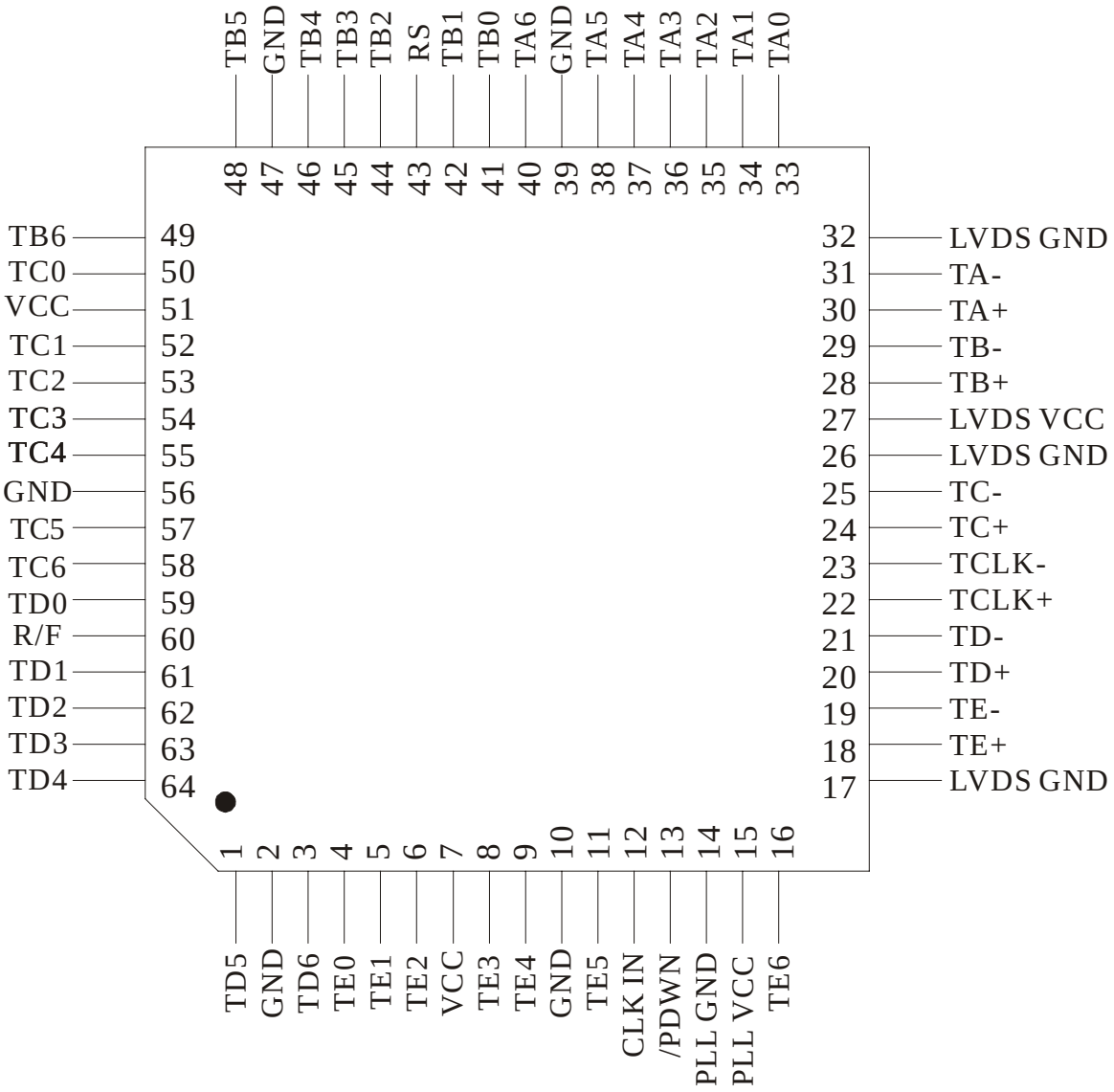
Features

- Wide dot clock range: 8-135MHz suited for NTSC, VGA, SVGA, XGA,SXGA and SXGA+
- PLL requires no external components
- Supports spread spectrum clock generator
- On chip jitter filtering
- Clock edge selectable
- Supports reduced swing LVDS for low EMI
- Power down mode
- Low power single 3.3V CMOS design
- 64pin TQFP
- Backward compatible with THC63LVDM63R(18bits) / M83R(24bits)

Block Diagram



Pin Out



Pin Description

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Type</th><th>Description</th></tr>
<tr><td>TA+, TA-</td><td>30, 31</td><td>LVDS OUT</td><td rowspan="5">LVDS Data Out.</td></tr>
<tr><td>TB+, TB-</td><td>28, 29</td><td>LVDS OUT</td></tr>
<tr><td>TC+, TC-</td><td>24, 25</td><td>LVDS OUT</td></tr>
<tr><td>TD+, TD-</td><td>20, 21</td><td>LVDS OUT</td></tr>
<tr><td>TE+,TE-</td><td>18, 19</td><td>LVDS OUT</td></tr>
<tr><td>TCLK+, TCLK-</td><td>22, 23</td><td>LVDS OUT</td><td>LVDS Clock Out.</td></tr>
<tr><td>TA0 ~ TA6</td><td>33,34,35,36,37,38,40</td><td>IN</td><td rowspan="5">Pixel Data Inputs.</td></tr>
<tr><td>TB0 ~ TB6</td><td>41,42,44,45,46,48,49</td><td>IN</td></tr>
<tr><td>TC0 ~ TC6</td><td>50,52,53,54,55,57,58</td><td>IN</td></tr>
<tr><td>TD0 ~ TD6</td><td>59,61,62,63,64,1,3</td><td>IN</td></tr>
<tr><td>TE0 ~ TE6</td><td>4,5,6,8,9,11,16</td><td>IN</td></tr>
<tr><td>/PDWN</td><td>13</td><td>IN</td><td>H: Normal operation,
L: Power down (all outputs are Hi-Z)</td></tr>
<tr><td>RS</td><td>43</td><td>IN</td><td>LVDS swing mode, VREF select.
<table><tr><th>RS</th><th>LVDS Swing</th><th>Small Swing Input Support</th></tr><tr><td>VCC</td><td>350mV</td><td>N/A</td></tr><tr><td>0.6 ~ 1.4V</td><td>350mV</td><td>RS=VREF[a]</td></tr><tr><td>GND</td><td>200mV</td><td>N/A</td></tr></table>a. VREF is Input Reference Voltage.</td></tr>
<tr><td>R/F</td><td>60</td><td>IN</td><td>Input Clock Triggering Edge Select.
H: Rising edge, L: Falling edge</td></tr>
<tr><td>VCC</td><td>51, 7</td><td>Power</td><td>Power Supply Pins for TTL inputs and digital circuitry.</td></tr>
<tr><td>CLKIN</td><td>12</td><td>IN</td><td>Clock in.</td></tr>
<tr><td>GND</td><td>2, 10, 39, 47, 56</td><td>Ground</td><td>Ground Pins for TTL inputs and digital circuitry.</td></tr>
<tr><td>LVDS VCC</td><td>27</td><td>Power</td><td>Power Supply Pins for LVDS Outputs.</td></tr>
<tr><td>LVDS GND</td><td>17, 26, 32</td><td>Ground</td><td>Ground Pins for LVDS Outputs.</td></tr>
<tr><td>PLL VCC</td><td>15</td><td>Power</td><td>Power Supply Pin for PLL circuitry.</td></tr>
<tr><td>PLL GND</td><td>14</td><td>Ground</td><td>Ground Pins for PLL circuitry.</td></tr>
</table>

Absolute Maximum Ratings [1]

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Driver Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +150°C
Resistance to soldering heat	+260°C /10sec
Maximum Power Dissipation @+25°C	1.0W

1. "Absolute Maximum Ratings" are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage	RS=VCC or GND	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage	RS=VCC or GND	GND		0.8	V
V_{DDQ}[1]	Small Swing Voltage		1.2		2.8	V
V_{REF}	Input Reference Voltage	Small Swing (RS=V_{DDQ}/2)		V_{DDQ}/2		
V_{SH}[2]	Small Swing High Level Input Voltage	V_{REF} = V_{DDQ}/2	V_{DDQ}/2 +100mV			V
V_{SL}[2]	Small Swing Low Level Input Voltage	V_{REF} = V_{DDQ}/2			V_{DDQ}/2 -100mV	V
I_{INC}	Input Current	$0V \le V_{IN} \le V_{CC}$			±10	µA

Notes: [1] V_{DDQ} voltage defines max voltage of small swing input. It is not an actual input voltage.
[2] Small swing signal is applied to TA[6:0], TB[6:0], TC[6:0], TD[6:0], TE[6:0] and CLKIN.

LVDS Transmitter DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

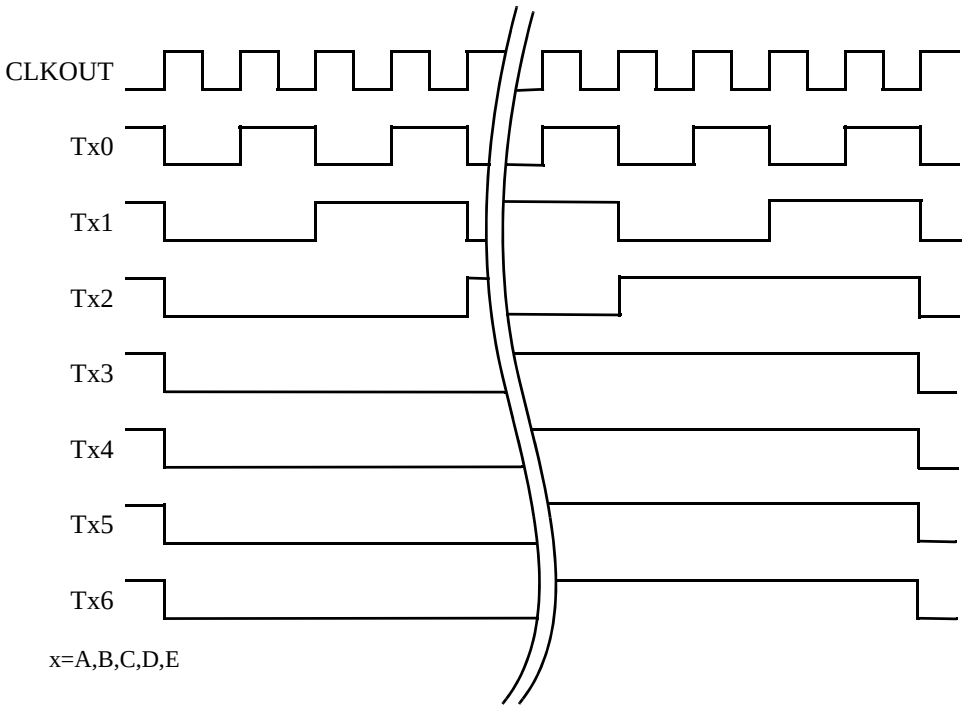
Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
VOD	Differential Output Voltage	RL=100Ω	Normal swing RS=VCC	250	350	450	mV
			Reduced swing RS=GND	100	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω				35	mV
VOC	Common Mode Voltage			1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states					35	mV
I_{OS}	Output Short Circuit Current	VOUT=0V, RL=100Ω				-24	mA
I_{OZ}	Output TRI-STATE Current	/PDWN=0V, V_{OUT}=0V to VCC				±10	µA

Supply Current

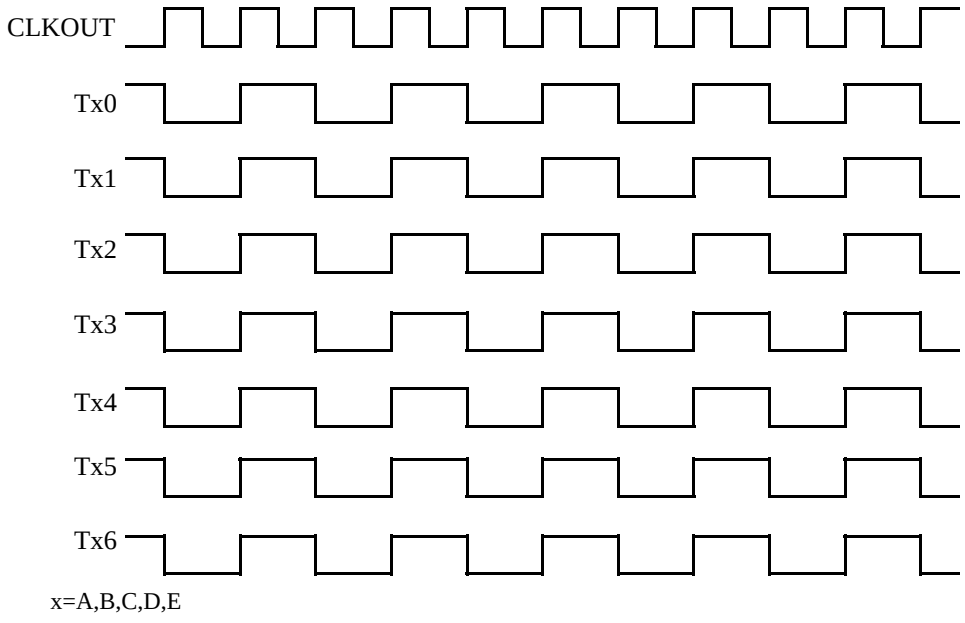
V_{CC} = 3.0V ~ 3.6V, Ta =0°C ~ +70°C

Symbol	Parameter	Conditions		Typ.	Max.	Units
I_{TCCG}	Transmitter Supply Current	RL=100Ω,CL=5pF V_{CC}=3.3V, RS=V_{CC} Gray Scale Pattern	f=85MHz	58	64	mA
			f=135MHz	70	76	mA
		RL=100Ω,CL=5pF V_{CC}=3.3V, RS=GND Gray Scale Pattern	f=85MHz	44	50	mA
			f=135MHz	56	62	mA

Gray Scale Pattern



Worst Case Pattern



Symbol	Parameter	Conditions		Typ.	Max.	Units
I_{TCCW}	Transmitter Supply Current	RL=100Ω, CL=5pF V_{CC}=3.3V, RS=V_{CC} Worst Case Pattern	f=85MHz	69	75	mA
			f=135MHz	87	93	mA
		RL=100Ω, CL=5pF V_{CC}=3.3V, RS=GND Worst Case Pattern	f=85MHz	55	61	mA
			f=135MHz	73	79	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN = L			10	μA

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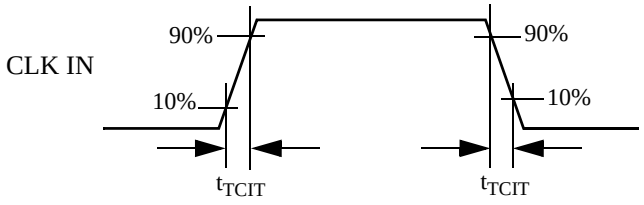
Switching Characteristics

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

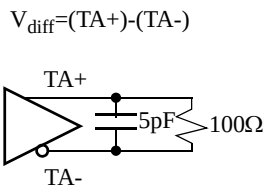
Symbol	Parameter	Min.	Typ.	Max.	Units
t_{TCIT}	CLK IN Transition time			5.0	ns
t_{TCP}	CLK IN Period	7.4		125.0	ns
t_{TCH}	CLK IN High Time	$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
t_{TCL}	CLK IN Low Time	$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
t_{TCD}	CLK IN to TCLK+/- Delay		$3t_{TCP}$		ns
t_{TS}	TTL Data Setup to CLK IN	2.5			ns
t_{TH}	TTL Data Hold from CKL IN	0			ns
t_{LVT}	LVDS Transition Time		0.6	1.5	ns
t_{TOP1}	Output Data Position0	-0.2	0.0	+0.2	ns
t_{TOP0}	Output Data Position1	$\frac{t_{TCP}}{7} - 0.2$	$\frac{t_{TCP}}{7}$	$\frac{t_{TCP}}{7} + 0.2$	ns
t_{TOP6}	Output Data Position2	$2\frac{t_{TCP}}{7} - 0.2$	$2\frac{t_{TCP}}{7}$	$2\frac{t_{TCP}}{7} + 0.2$	ns
t_{TOP5}	Output Data Position3	$3\frac{t_{TCP}}{7} - 0.2$	$3\frac{t_{TCP}}{7}$	$3\frac{t_{TCP}}{7} + 0.2$	ns
t_{TOP4}	Output Data Position4	$4\frac{t_{TCP}}{7} - 0.2$	$4\frac{t_{TCP}}{7}$	$4\frac{t_{TCP}}{7} + 0.2$	ns
t_{TOP3}	Output Data Position5	$5\frac{t_{TCP}}{7} - 0.2$	$5\frac{t_{TCP}}{7}$	$5\frac{t_{TCP}}{7} + 0.2$	ns
t_{TOP2}	Output Data Position6	$6\frac{t_{TCP}}{7} - 0.2$	$6\frac{t_{TCP}}{7}$	$6\frac{t_{TCP}}{7} + 0.2$	ns
t_{TPLL}	Phase Lock Loop Set			10.0	ms

AC Timing Diagrams

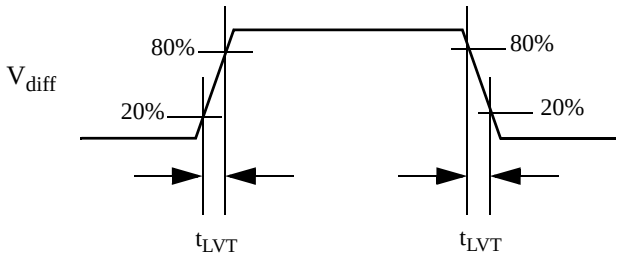
TTL Input



LVDS Output

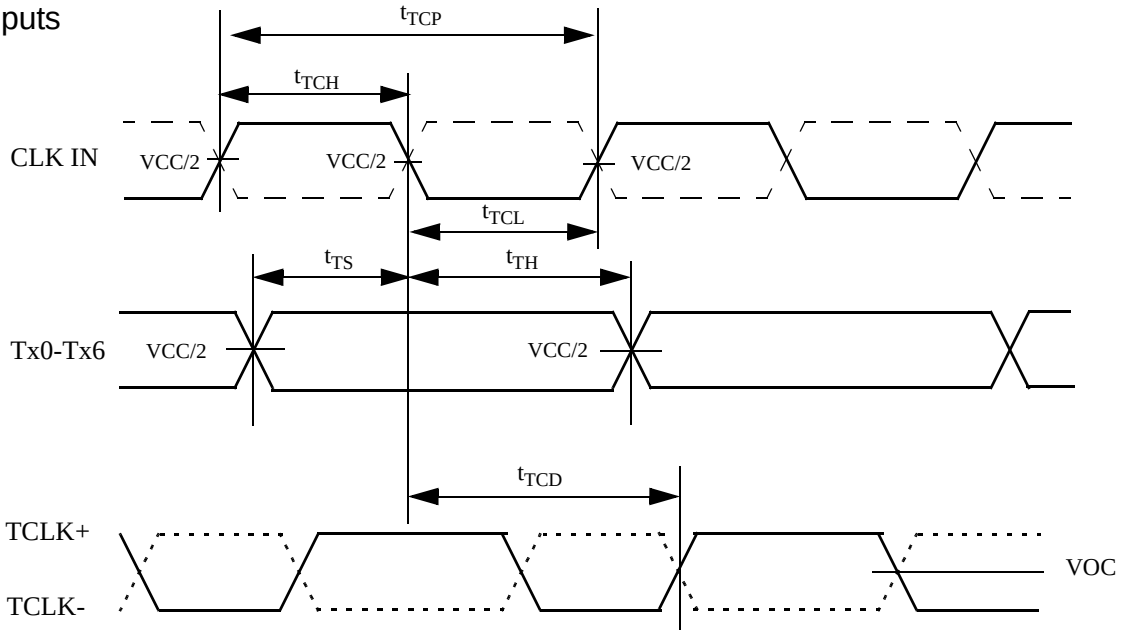


LVDS Output Load



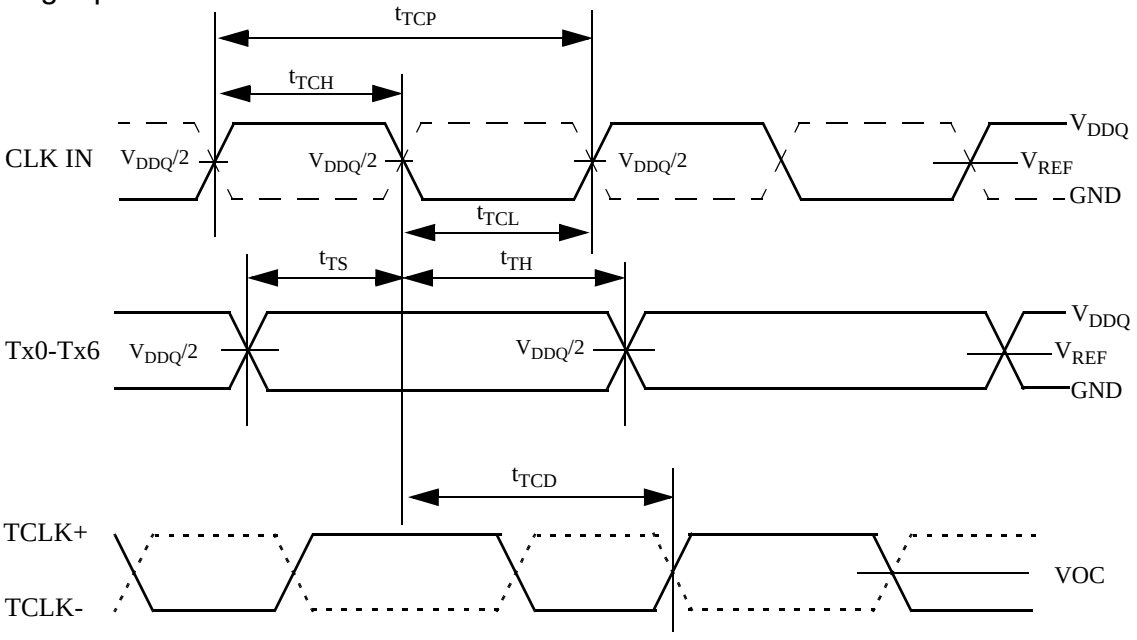
AC Timing Diagrams

TTL Inputs



Note:
CLK IN: for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line

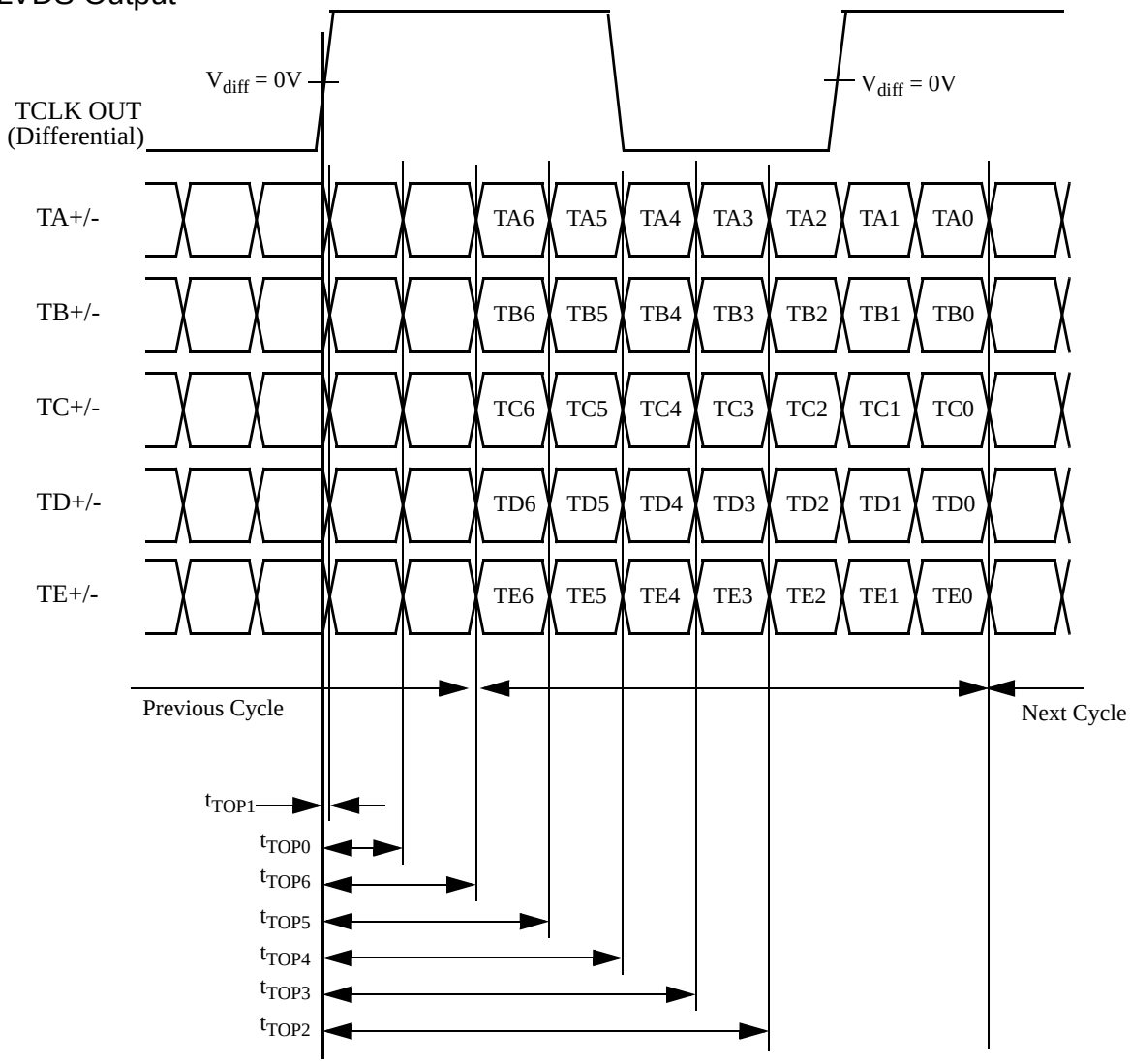
Small Swing Inputs



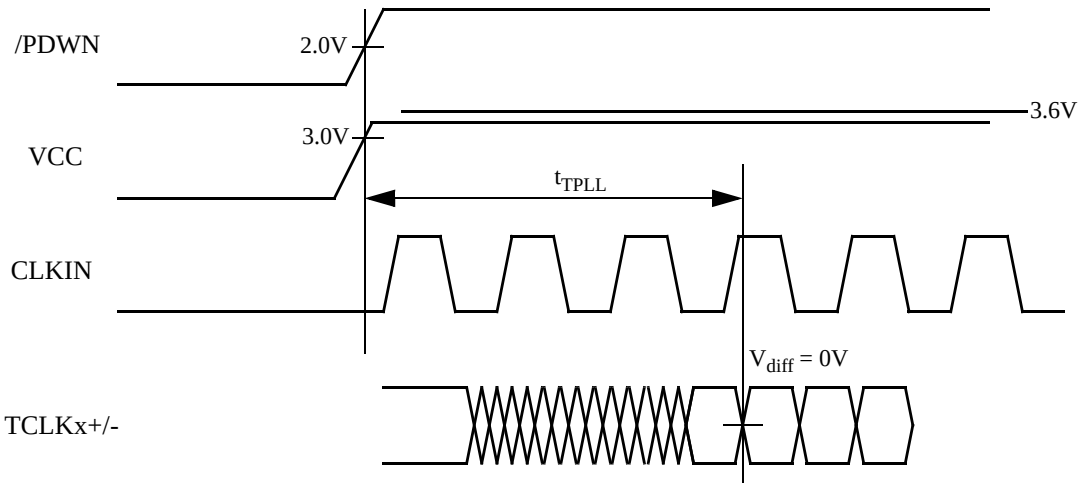
Note:
CLK IN: for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line

AC Timing Diagrams

LVDS Output

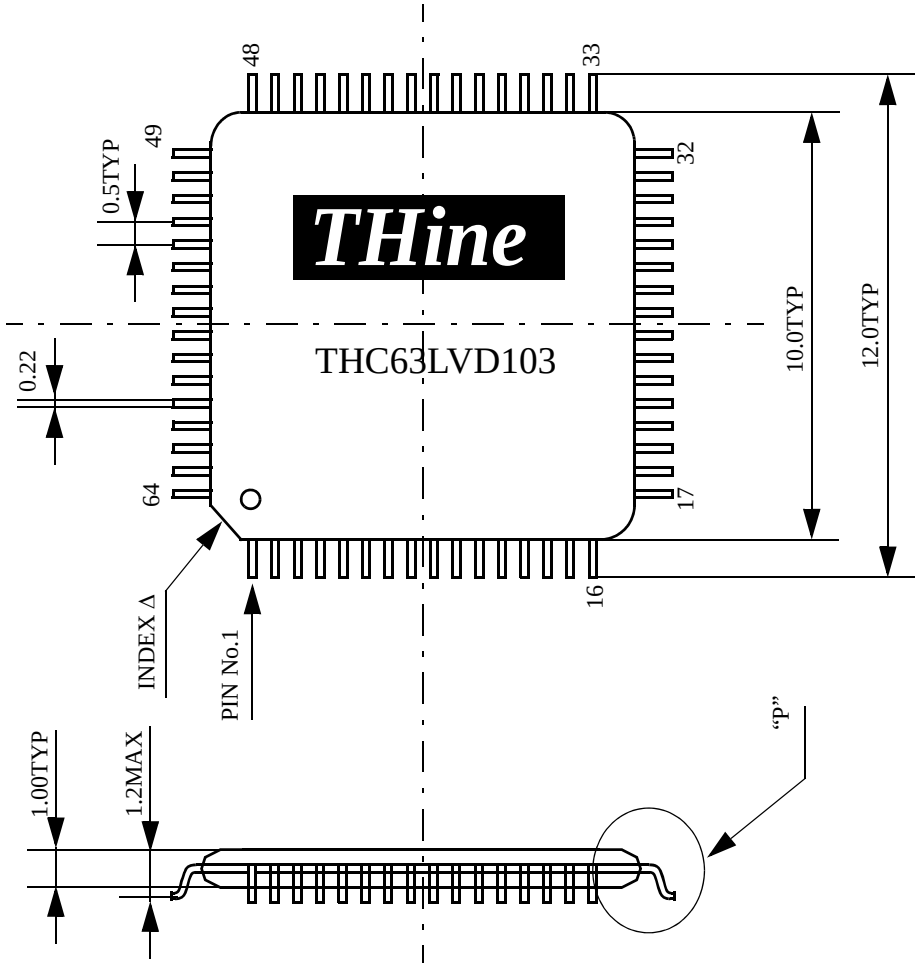


Phase Lock Loop Set Time



Package

64 Pin TQFP ,JEDEC



UNITS: mm

Notes to Users:

1. The contents of this data sheet are subject to change without prior notice.
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8. This technical document was provisionally created during development of THC63LVD103, so there is a possibility of differences between it and the product's final specifications. When designing circuits using THC63LVD103, be sure to refer to the final technical documents.

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