3-V to 20-V High-Current Load Switch

Check for Samples: TPS2590

FEATURES

- **Integrated Pass MOSFET**
- **3-V to 20-V Bus Operation**
- **Programmable Fault Timer**
- **Programmable Fault Current**
- **Programmable Hard Current Limit**
- **Fast Disable**
- **Thermal Shutdown**
- **Load Fault Alert**
- **Latching and Auto-retry Operation**
- **4-mm x 4-mm QFN**
- **-40°C to 125°C Junction Temperature Range**
- **UL Listed - File Number E169910**

APPLICATIONS

- **RAID Arrays**
- **Telecommunications**
- **Plug-In Circuit Boards**
- **Disk Drive**
- **Notebooks / Netbooks**

DESCRIPTION

The TPS2590 provides highly integrated hot-swap power management and superior protection in applications where the load is powered by voltages between 3.0 V and 20 V. This device is intended for systems where a voltage bus must be protected to prevent load shorts from interrupting or damaging other system components. The TPS2590 is in a 16-pin QFN package.

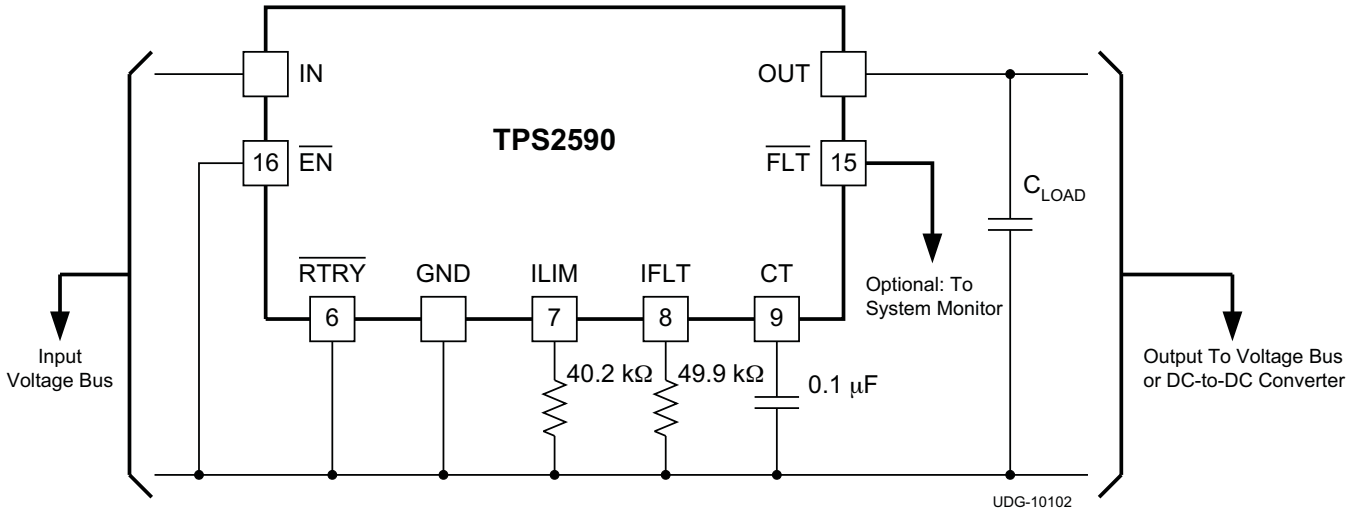
The TPS2590 has multiple programmable protection features. Load protection is accomplished by a non-current limiting fault threshold, a hard current limit threshhold, and a fault timer. The dual current thresholds allow the system to draw high current for short periods without causing a voltage droop at the load. An example of this is a disk drive startup. This technique is ideal for loads that experience brief high demand, but benefit from protection levels consistent with average current draw.

Hotswap MOSFET protection is provided by power limit circuitry which protects the internal MOSFET against SOA related failures.

The TPS2590 provides a fault indicator output and allows latch off or retry on fault.

12-V, 3.5-A Application

Figure 1.



ORDERING INFORMATION

DEVICE	JUNCTION TEMPERATURE	PACKAGE	ORDERING CODE	MARKING
TPS2590	-40°C to 125°C	RSA (4-mm x 4-mm QFN)	TPS2590RSA	TPS2590

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

		UNIT
Input voltage range IN, OUT	-0.3 to 25	V
Voltage range $\overline{FLT}$	-0.3 to 20	
Voltage IFAULT, ILIM	1.75	
Voltage CT	3.0	
Output sink current $\overline{FLT}$	10	mA
Input voltage range, $\overline{EN}$	-0.3 to 6	V
Input current, $\overline{RTRY}$ ($\overline{RTRY}$ internally clamped to 3 V) $\overline{RTRY}$ = 0 V	35	uA
Voltage range CT(3), IFLT(3) ,ILIM(3), $\overline{RTRY}$	-0.3 to 3	V
ESD rating, HBM	2 .5 k	
ESD rating, CDM	400	
Operating junction temperature range, T_J	Internally Limited	°C
Storage temperature range, T_{stg}	-65 to 150	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Do not apply voltage to pin.

DISSIPATION RATINGS(1) (2) (3) (4)

PACKAGE	θ_{JA} LOW K, °C/W	θ_{JA} HIGH K, °C/W	θ_{JA} BEST 4, °C/W
RSA	211	55	50

(1) Tested per JEDEC JESD51, natural convection. The definitions of high-k and low-k are per JESD 51-7and JESD 51-3.
(2) Low-k (2 signal - no plane, 3 in. by 3 in. board, 0.062 in. thick, 1 oz. copper) test board with the pad soldered, and an additional 0.12 in.2 of top-side copper added to the pad.
(3) High-k is a (2 signal – 2 plane) test board with the pad soldered.
(4) The best case thermal resistance is obtained using the recommendations per SLMA002A (2 signal - 2 plane with the pad connected to the plane).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	NOM	MAX	UNIT
Input voltage range IN, OUT	3		20	V
Voltage range $\overline{EN}$	0		5	
Voltage range $\overline{FLT}$	0		20	
Output sink current $\overline{FLT}$	0		1	mA
Voltage range $\overline{RTRY}$	0		3	V
CCT	100 p		10 m	F
Junction temperature	-40		125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN						
	UVLO	V_{IN} ↑	2.6	2.85	2.9	V
		Hysteresis		150		mV
	Bias current	$\overline{EN}$ = 2.4 V		25	100	µA
		$\overline{EN}$ = 0 V		3.9	5	mA
OUT						
	RON	$R_{VIN-VOUT}$, I_{VOUT} < I_{RLIM} or I_{VOUT} < (I_{SET} x 1.25), 1 A ≤ I_{VOUT} ≤ 4.5 A		29.5	42.0	mΩ
	Power limit	V_{IN}: 12 V, C_{OUT} = 1000 µF, $\overline{EN}$: 3 V → 0 V	3	5	7.5	W
	Reverse diode voltage	V_{OUT} > V_{IN} , $\overline{EN}$ = 5 V, I_{IN} = - 1 A		0.77	1.0	V
IFLT						
I_{FLT}	Fault current threshold	I_{VOUT} ↑, I_{CT}: sinking → sourcing, pulsed test (R_{RFLT} = 200 kΩ)	0.8	1	1.2	A
		I_{VOUT} ↑, I_{CT}: sinking → sourcing, pulsed test (R_{RFLT} = 100 kΩ)	1.8	2	2.2	
		I_{VOUT} ↑, I_{CT}: sinking → sourcing, pulsed test (R_{RFLT} = 49.9 kΩ)	3.6	4	4.4	
ILIM						
	Current limit program I_{VOUT} , V_{VIN}-V_{OUT} = 0.3 V, pulsed test	R_{RLIM} = 100 kΩ	1.6	2	2.4	A
		R_{RLIM} = 66.5 kΩ	2.6	3	3.4	
		R_{RLIM} = 40.2 kΩ	4.6	5	5.4	
CT						
	Charge/discharge current	I_{CT} sourcing, V_{CT} = 1 V	29	35	41	µA
		I_{CT} sinking, V_{CT} = 1 V	1.0	1.4	1.8	
	Threshold voltage	V_{CT} ↑	1.3	1.4	1.5	V
		V_{CT} ↓	0.1	0.16	0.3	
	ON/OFF fault duty cycle	V_{VOUT} = 0 V	2.8	3.7	4.6	%

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{EN}$						
	Threshold voltage	$V_{\overline{EN}}$ ↓	0.8	1.0	1.5	V
		Hysteresis	50	150	250	mV
	Input bias current	$V_{\overline{EN}}$ = 2.4 V (sinking)	-1.5	0	0.5	µA
		$V_{\overline{EN}}$ = 0.2 V (sourcing)	-2	1	0.5	
	Turn on propagation delay	V_{IN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 2.4 V → 0.2 V, V_{OUT}: ↑ 90% x VI_N		350	500	µs
	Turn off propagation delay	V_{IN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 0.2 V → 2.4 V, V_{OUT}: ↓10% x V_{IN}		10	20	
$\overline{FLT}$						
	VOUT LOW	V_{CT} = 1.8 V, $I_{\overline{FLT}}$ = 1 mA		0.2	0.4	V
	Leakage current	$V_{\overline{FLT}}$ = 18 V			1	µA
$\overline{RTRY}$						
	Low threshold voltage	Auto Retry Mode			0.8	V
	High threshold	Latch mode	2.0			
	Input bias current	$V_{\overline{RTRY}}$ = 3.0 V	-1.0	0.2	1.0	mA
		$V_{\overline{RTRY}}$ = 0.2 V	-50	-25	0	
Thermal Shutdown						
	Thermal shutdown	T_J		160		°C
		Hysteresis		10		

DEVICE INFORMATION

TPS2590 Functional Block Diagram

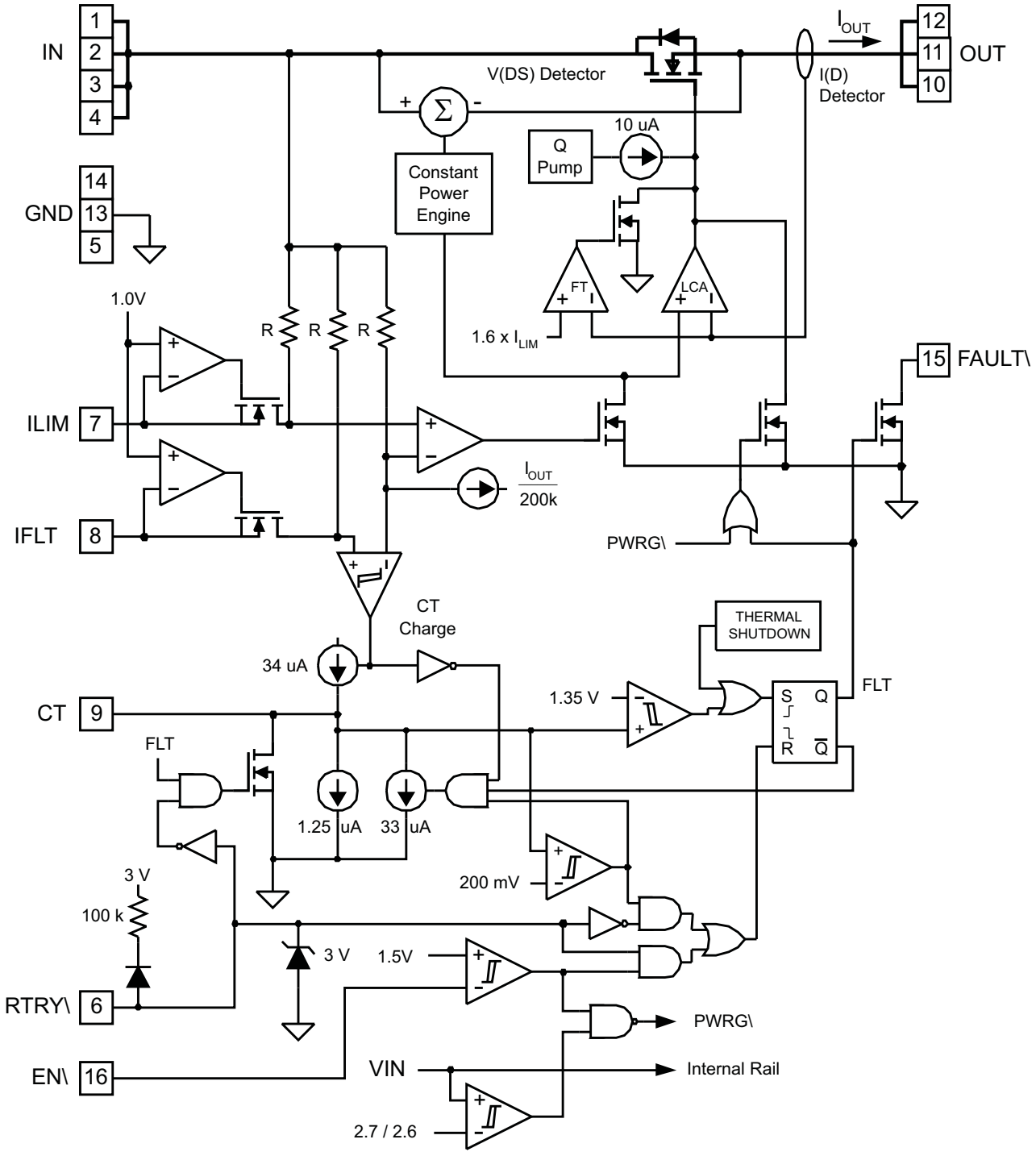
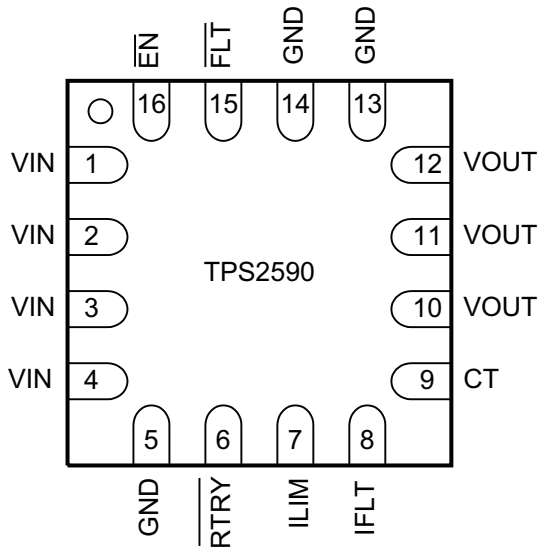


Figure 2.

TPS2590 PINOUT



TERMINAL FUNCTIONS

FUNCTION	TPS2590	DESCRIPTION
$\overline{EN}$	16	Device is enabled when this pin is pulled low.
IN	1-4	Power In and control supply voltage.
$\overline{RTRY}$	6	If low, the TPS2590 will attempt to restart after an overcurrent fault. If floating (high) the device will latch off after an overcurrent fault and will not attempt to restart until $\overline{EN}$ or Vin is cycled off and on.
ILIM	7	A resistor to ground sets the current limit level.
IFLT	8	A resistor to ground sets the fault current level.
CT	9	A capacitor to ground sets the fault time.
GND	5, 13, 14	GND
OUT	10, 11, 12	Output to the load.
$\overline{FLT}$	15	Fault low indicated the fault time has expired and the FET is switched off.

PIN DESCRIPTION

CT: Connect a capacitor form CT to GND to set the fault time. The fault timer starts when the fault current threshold is exceeded, charging the capacitor with 36 µA from GND towards an upper threshold of 1.4 V. If the capacitor reaches the upper threshold, the internal pass MOSFET is turned off. The MOSFET will stay off until $\overline{EN}$ is cycled if a latching version is used. If an auto-retry version is used, the capacitor will discharge at 5 µA to 0.2 V and then re-enable the pass MOSFET. When the device is disabled, CT is pulled to GND through a 100-kΩ resistor.

The timer period must be chosen long enough to allow the external load capacitance to charge. The fault timer period is selected using the following formula where T_{FAULT} is the minimum timer period in seconds and C_{CT} is in Farads.

$$C_{CT} = \frac{T_{FAULT}}{38.9 \times 10^3} \quad (1)$$

This equation does not account for component tolerances. In autoretry versions, the second and subsequent retry timer periods will be approximately 85 % as long as the first retry period.

In autoretry versions, the fault timer discharges the capacitor for a nominal t_{SD} in seconds with C_{CT} in Farads per the following equation.

$$t_{SD} = 1.0 \times 10^6 \times C_{CT} \quad (2)$$

The nominal ratio of on-to-off times represents about a 3% duty cycle when a hard fault is present on the output of an autoretry version part.

$\overline{\text{FLT}}$: Open-drain output that pulls low on any condition that causes the output to open. These conditions are either an overload with a fault time-out, or a thermal shutdown. $\overline{\text{FLT}}$ becomes operational before UV, when VIN is greater than 1 V. IFLT may not be set below 1 A to maintain the Fault Current Limit threshold accuracy listed in Electrical Characteristics. Some parts may not current limit or fault as expected.

GND: This is the most negative voltage in the circuit and is used as reference for all voltage measurements unless otherwise specified.

IFLT: A resistor connected from this pin to ground sets the fault current threshold (I_{FAULT}). Currents between the fault current threshold and the current limit are permitted to flow unimpeded for the period set by the fault timer programmed on CT. This permits loads to draw momentary surges while maintaining the protection provided by a lower average-current limit.

The fault timer implemented by CT starts charging CT when current through V_{IN} exceeds I_{FAULT}. If the current doesn't drop below the I_{FAULT} level before V_{CT} reaches its upper threshold, the output will be shut off. The fault current resistor is set by the following formula where I_{FAULT} is in Amperes and R_{RFLT} is in Ohms.

$$R_{RFLT} = \frac{200\,k\Omega}{I_{FAULT}} \quad (3)$$

ILIM: A resistor connected from this pin to ground sets I_{LIM}. The TPS2590 will limit current to I_{LIM}. If the current doesn't drop below the I_{FAULT} level before the timer times out then the output will be shut off. R_{LIM} is set by the formula:

$$R_{LIM} = \frac{201k\Omega}{I_{LIM}} \quad (4)$$

I_{LIM} must be set sufficiently larger than I_{FAULT} to ensure that I_{LIM} could never be less than I_{FAULT}, even after taking tolerances into account.

$\overline{\text{EN}}$: When this pin is pulled low, the IC is enabled. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit. $\overline{\text{EN}}$ is pulled to VIN by a 10-MΩ resistor, pulled to GND by 16.8 MΩ and is clamped to ground by a 7-V Zener diode. Because high impedance pullup/down resistors are used to reduce current draw, any external FET controlling this pin should be low leakage.

IN: Input voltage to the TPS2590. The recommended operating voltage range is 3 V to 18 V. All VIN pins should be connected together and to the power source.

OUT: Output connection for the TPS2590. When switched on the output voltage will be approximately:

$$V_{OUT} = V_{IN} - 0.04 \times I_{OUT} \quad (5)$$

All OUT pins should be connected together and to the load.

$\overline{\text{RTRY}}$: When pulled low the TPS2590 will attempt to restart after a fault. If left floating or pulled high the TPS2590 will latch off after a fault. This pin is internally clamped at 3 V and is pulled to the internal 3-V supply by a diode in series with a 100-kΩ resistor.

TYPICAL CHARACTERISTICS

CURRENT LIMIT vs JUNCTION TEMPERATURE

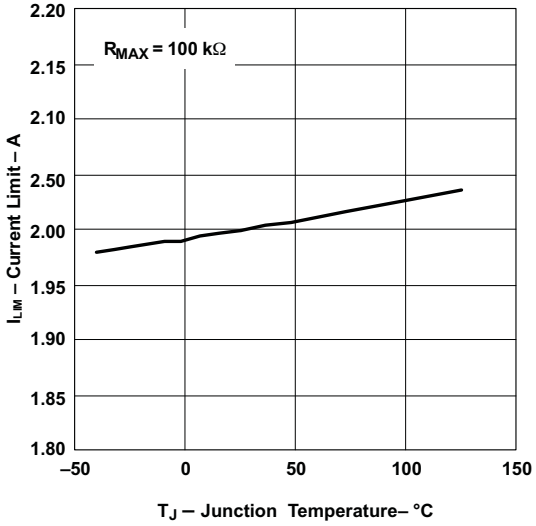


Figure 3.

FAULT CURRENT vs JUNCTION TEMPERATURE

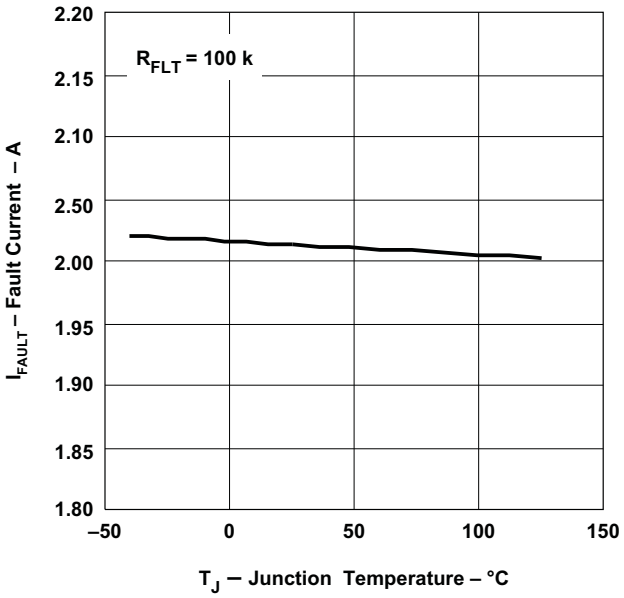


Figure 4.

POWER LIMIT vs JUNCTION TEMPERATURE

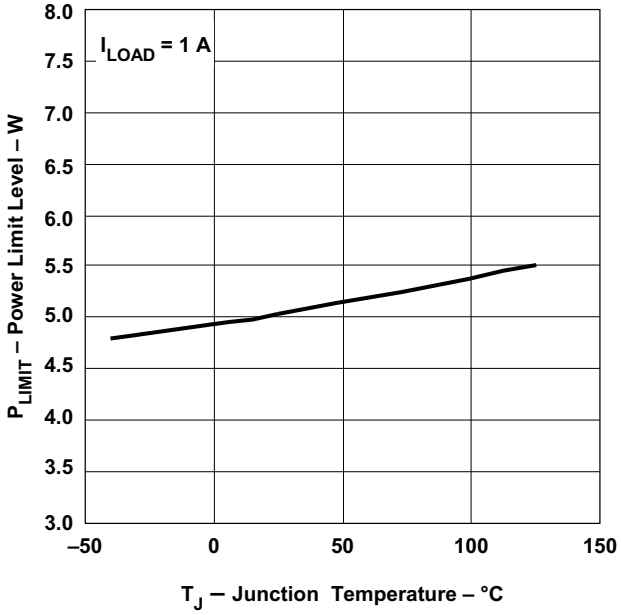


Figure 5.

SLEEP MODE SUPPLY CURRENT (VCC = 12 V) vs JUNCTION TEMPERATURE

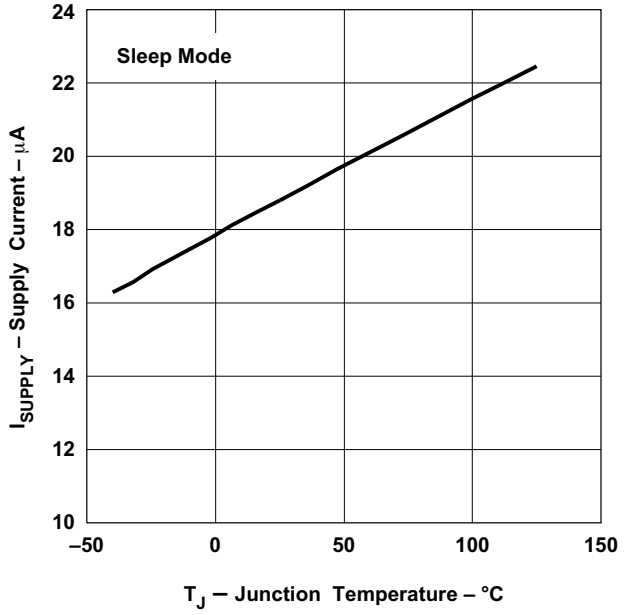


Figure 6.

TYPICAL CHARACTERISTICS (continued)

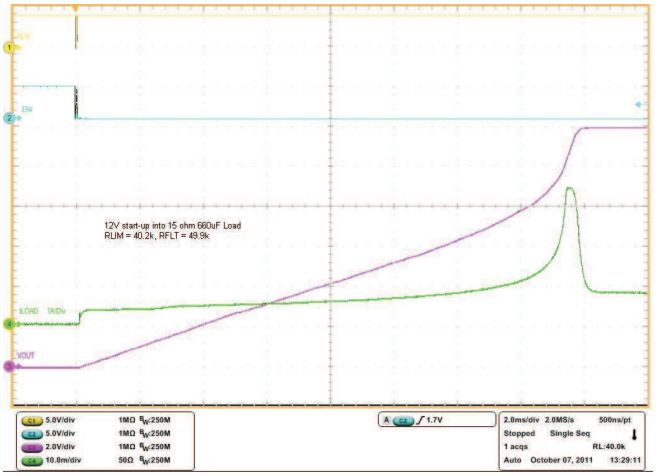


Figure 7. 12-V Startup into 15-Ω, 700-µF Load

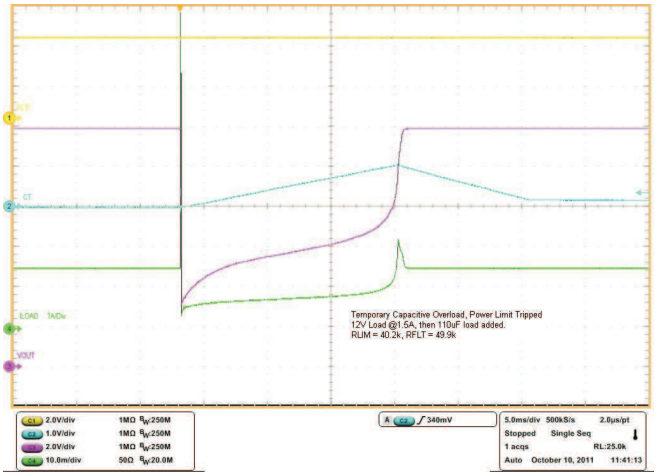


Figure 8. 12-V Input Addded to an 8-Ω Load

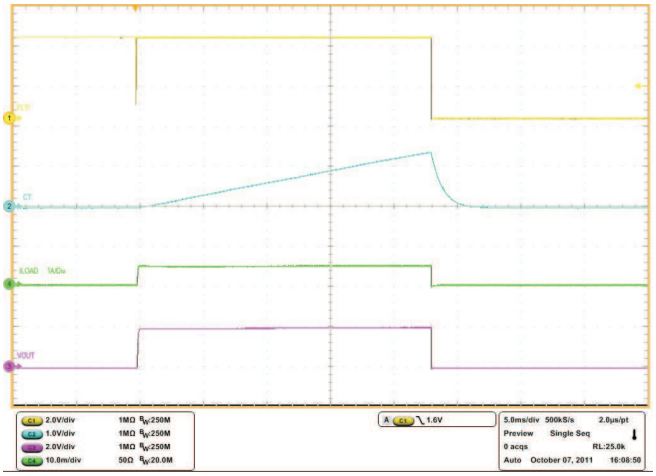


Figure 9. Failed Startup into a 4-Ω Load

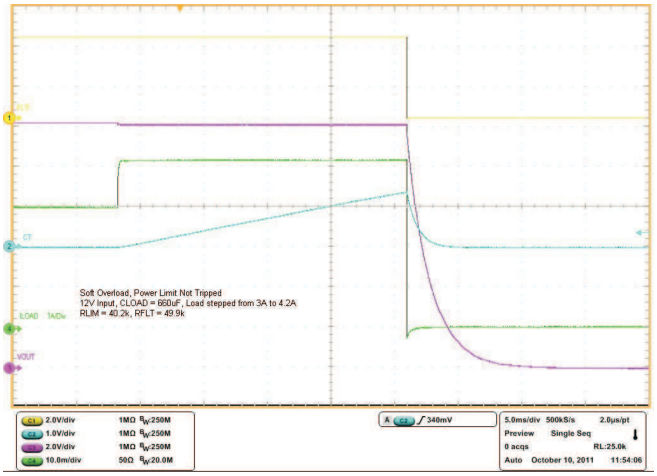


Figure 10. 12-V Soft Overload, 3-A to 4.2-A, Power Limit Not Tripped

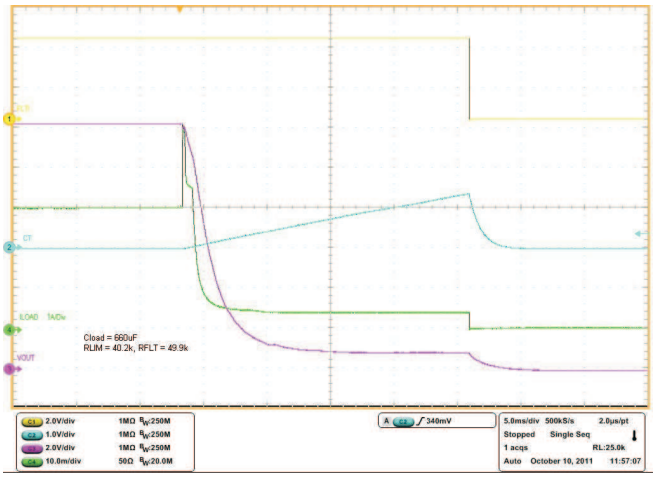


Figure 11. Firm Overload, 3-A to 5.4 A, Power Limit Tripped

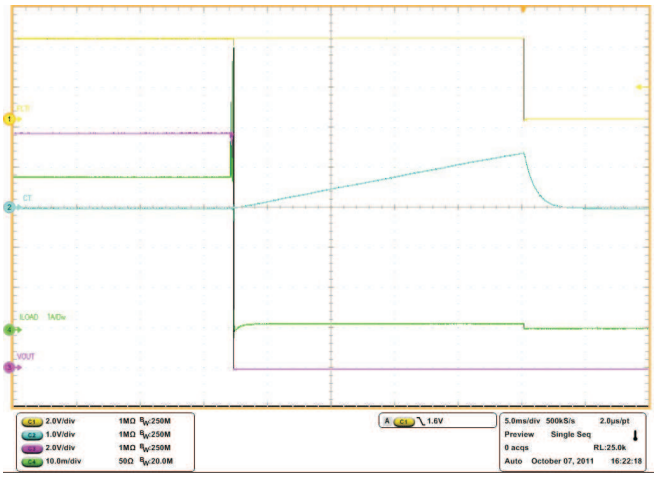


Figure 12. 12-V Hard Overload, 3.6-A Load then Short

TYPICAL CHARACTERISTICS (continued)

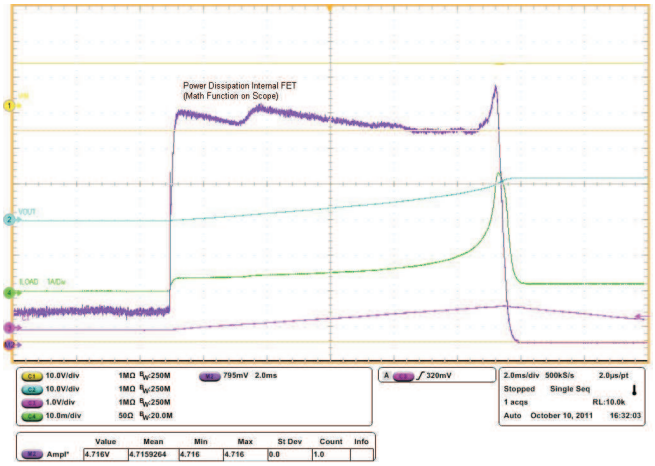


Figure 13. Power Dissipation During 12-V Startup into a 60-Ω, 660-µF Load

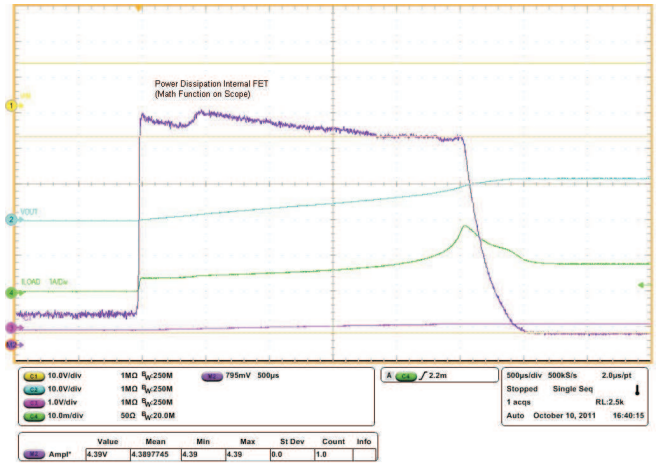


Figure 14. Power Dissipation During 12-V Startup into a 15-Ω, 110-µF Load

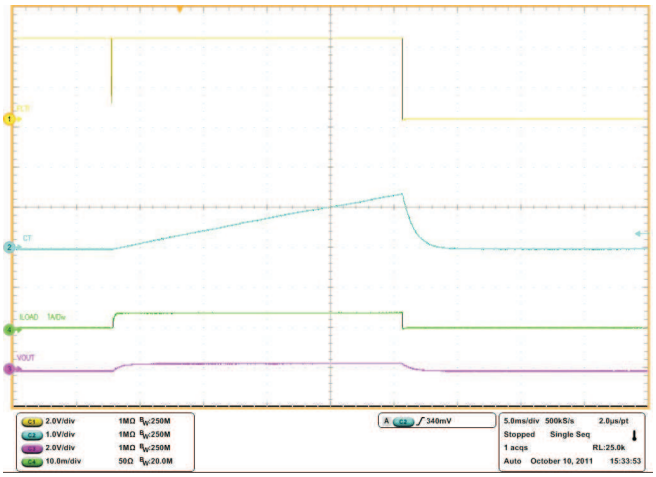


Figure 15. Startup into a 1-Ω Load

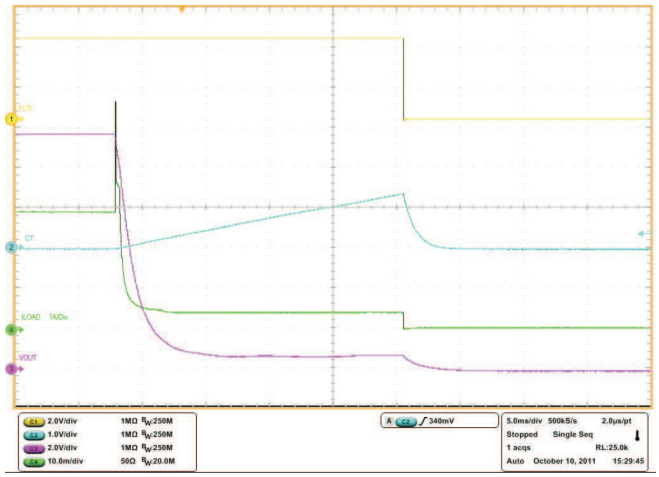


Figure 16. Firm Overload, Load Stepped From 3.8 A to 5.5 A

TYPICAL CHARACTERISTICS (continued)

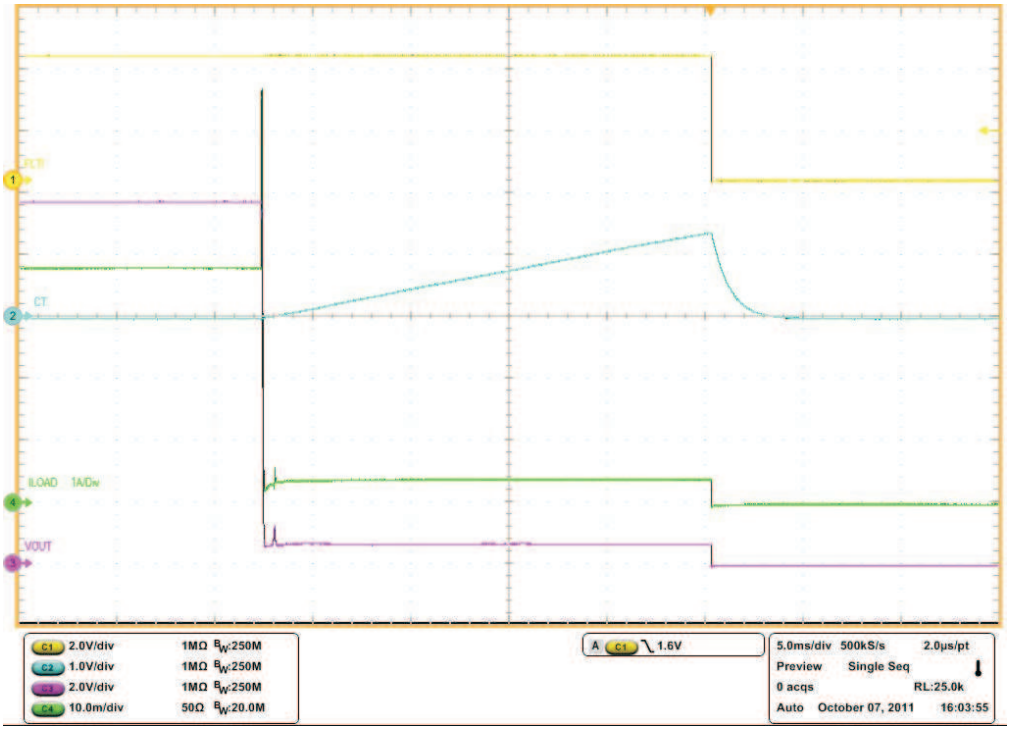


Figure 17. Hard Overload, Load Stepped from 3.8 A to 7.1 A

APPLICATION INFORMATION

Maximum Load at Startup

The power limiting function of the TPS2590 provides very effective protection for the internal FET. Expectedly, there is a supply voltage dependent maximum load which the device will be able to power up. Loads above this level may cause the device to shut off current before startup is complete. Neglecting any load capacitance, the maximum load (minimum load resistance) is calculated using the equation;

$$R_{MIN} = \frac{V_{IN}^2}{12} \quad (6)$$

Adding load capacitance may reduce the maximum load which can be present at start up.

If $\overline{EN}$ is tied to GND at startup and IN does not ramp quickly the TPS2590 may momentarily turn off then on during startup. This can happen if a capacitive load momentarily pulls down the input voltage below the UV threshold. If necessary, this can be avoided by delaying $\overline{EN}$ assertion until VIN is fully up.

Transient Protection

The need for transient protection in conjunction with hot-swap controllers should always be considered. When the TPS2590 interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. Such transients can easily exceed twice the supply voltage if steps are not taken to address the issue. Typical methods for addressing transients include;

- Minimizing lead length/inductance into and out of the device.
- Transient Voltage Suppressors (TVS) on the input to absorb inductive spikes.
- Shottky diode across the output to absorb negative spikes.
- A combination of ceramic and electrolytic capacitors on the input and output to absorb energy.

The following equation estimates the magnitude of these voltage spikes:

Where;

$$V_{SPIKE(absolute)} = V_{NOM} + I_{LOAD} \times \sqrt{L/C} \quad (7)$$

- V_{NOM} equals the nominal supply voltage.
- I_{LOAD} equals the load current.
- C equals the capacitance present at the input or output of the TPS2590.
- L equals the effective inductance seen looking into the source or the load.

The inductance due to a straight length of wire equals approximately.

Where;

$$L_{straightwire} \approx 0.2 \times L \times \ln\left(\frac{4 \times L}{D} - 0.75\right) (nH) \quad (8)$$

- L equals the length of the wire.
- D equals wire diameter.

Some applications may require the addition of a TVS to prevent transients from exceeding the absolute ratings if sufficient capacitance cannot be included.

REVISION HISTORY

Changes from Original (July 2009) to Revision A **Page**

- Changed , fixed typo in Application 1

Changes from Revision A (July 2010) to Revision B **Page**

- Added UL Listed - File Number E169910 1
- Changed , updated application diagram 1

Changes from Revision B (August 2010) to Revision C **Page**

- Added updated IFLT description 7
- Changed Current Limit vs Junction Temperature graph 8

Changes from Revision C (September 2011) to Revision D **Page**

- Changed Figure 7 through Figure 17. 8
- Changed Figure 7 through Figure 17. 9
- Changed Figure 7 through Figure 17. 10
- Changed Figure 7 through Figure 17. 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS2590RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2590RSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

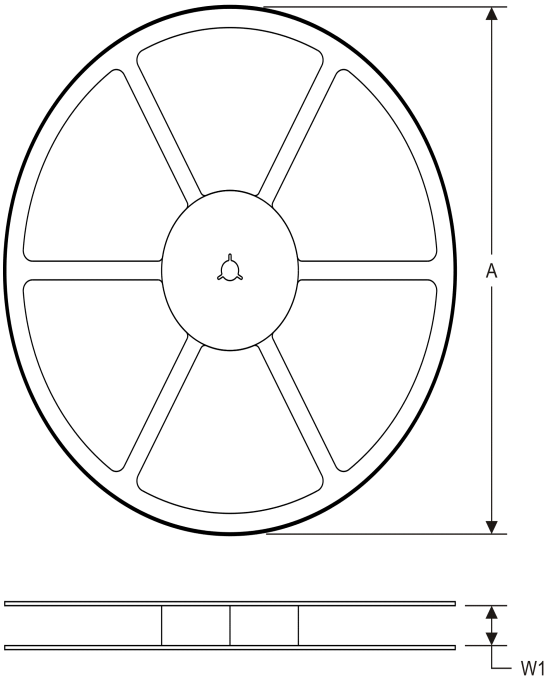
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

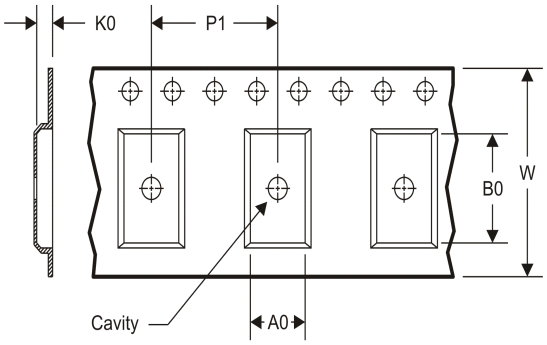
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



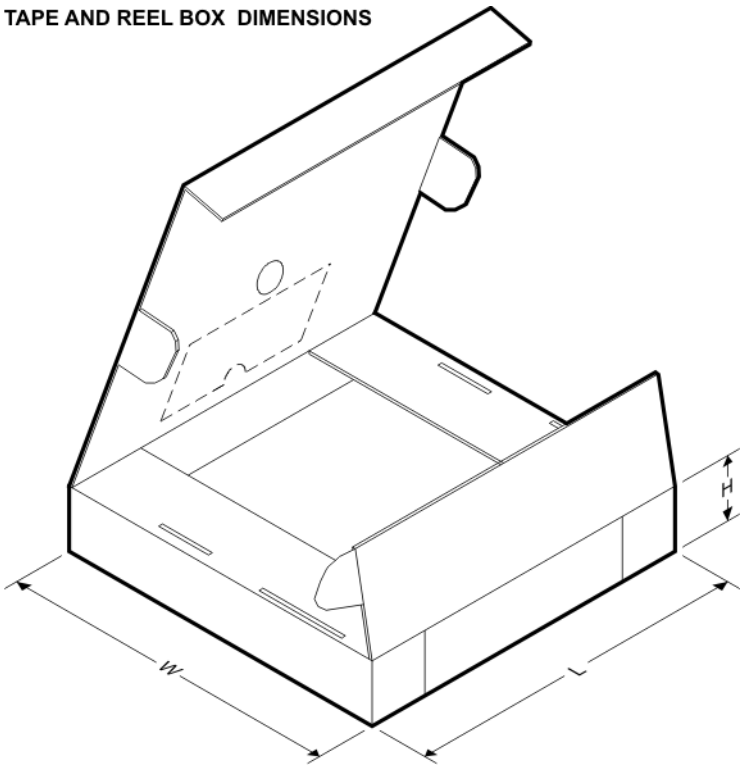
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2590RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS2590RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

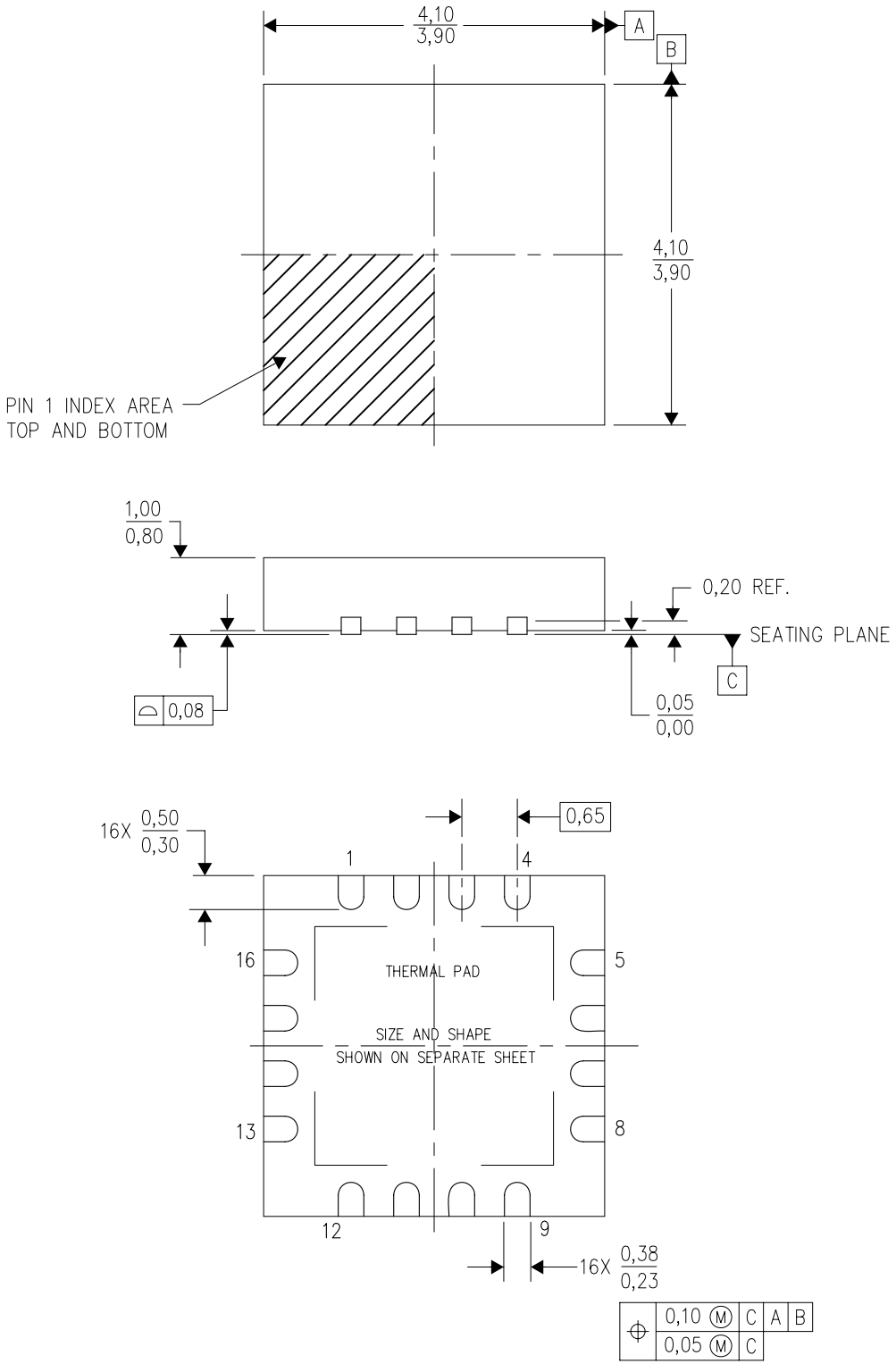
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2590RSAR	QFN	RSA	16	3000	367.0	367.0	35.0
TPS2590RSAT	QFN	RSA	16	250	210.0	185.0	35.0

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

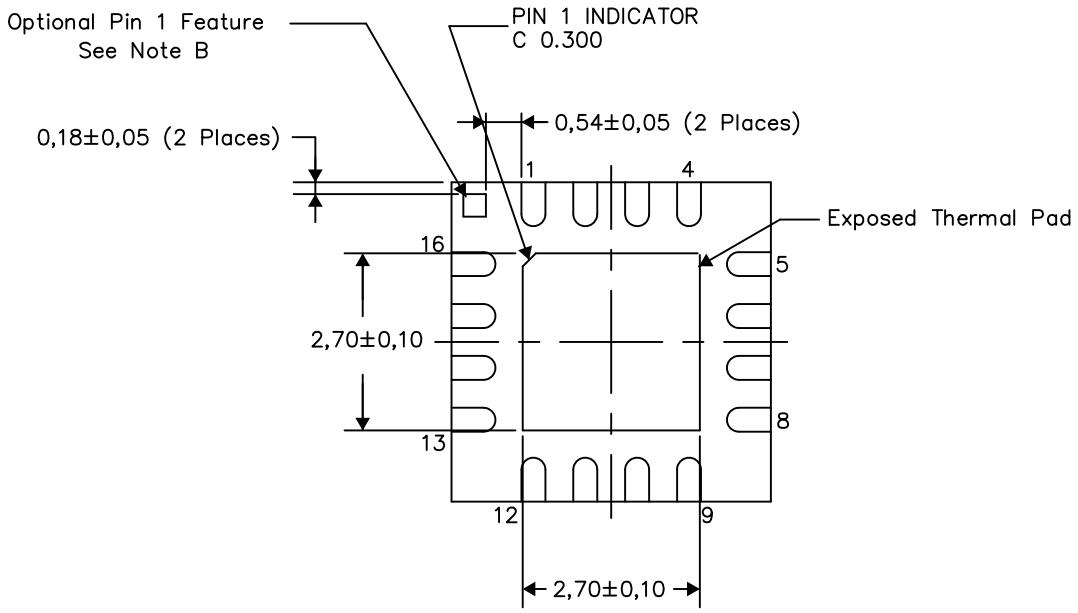
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

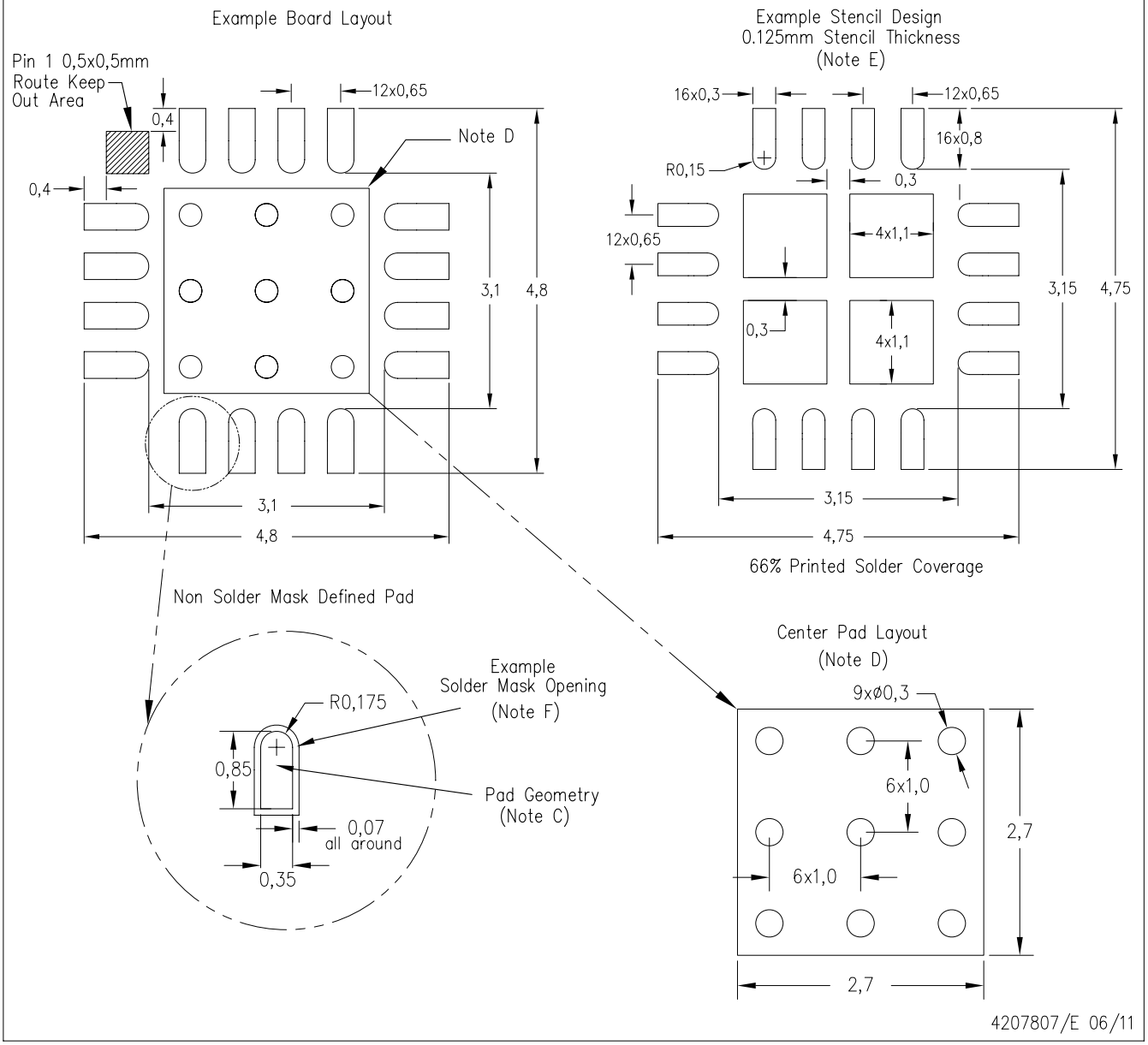
4206364/L 08/12

NOTES:

A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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