

**Document Title****512Kx8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Data</u></b>	<b><u>Remark</u></b>
0.0	Initial Draft	July 29, 2002	Preliminary
0.1	Revised - Added 55ns product( Vcc = 3.0V~3.6V)	October 14, 2002	Preliminary
0.2	Revised - Added Commercial product	December 2, 2002	Preliminary
0.21	Revised - Errata correction : corrected commercial product family name from K6X4008T1F-F to K6X4008T1F-B in PRODUCT FAMILY.	March 26, 2003	Preliminary
1.0	Finalized - Changed Icc from 4mA to 2mA - Changed Icc1 from 4mA to 3mA - Changed Icc2 from 30mA to 25mA - Changed Isb1(Commercial) from 15μA to 10μA - Changed Isb1(industrial) from 20μA to 10μA - Changed Isb1(Automotive) from 30μA to 20μA - Changed IDR(Commercial) from 15μA to 10μA - Changed IDR(industrial) from 20μA to 10μA - Changed IDR(Automotive) from 30μA to 20μA	September 16, 2003	Final

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## 512K×8 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology: Full CMOS
- Organization: 512K×8
- Power Supply Voltage: 2.7~3.6V
- Low Data Retention Voltage: 2V(Min)
- Three State Outputs
- Package Type: 32-SOP-525, 32-TSOP2-400F/R  
32-TSOP1-0813.4F

### GENERAL DESCRIPTION

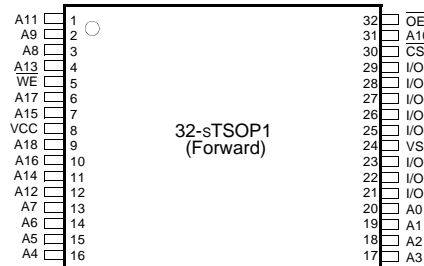
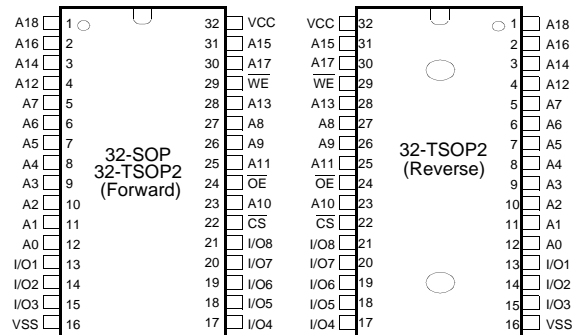
The K6X4008T1F families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support various operating temperature range and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Max)	Operating (I <sub>CC2</sub> , Max)	
K6X4008T1F-B	Commercial(0~70°C)	2.7~3.6V	55 <sup>1</sup> /70 <sup>2</sup> /85ns	10μA	25mA	32-SOP-525, 32-TSOP1-0813.4F 32-TSOP2-400F/R
K6X4008T1F-F	Industrial(-40~85°C)			10μA		
K6X4008T1F-Q	Automotive(-40~125°C)		70 <sup>2</sup> /85ns	20μA		32-SOP-525, 32-TSOP1-0813.4F 32-TSOP2-400F

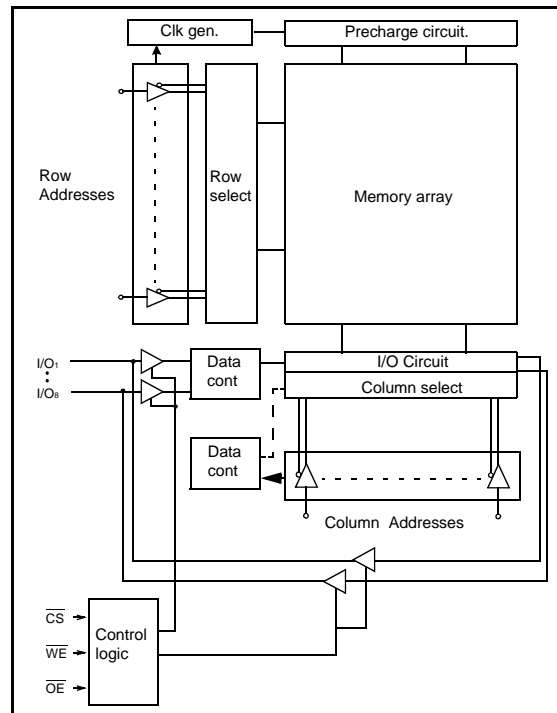
1. This parameter is measured in the voltage range of 3.0V~3.6V with 30pF test load.
2. This parameter is measured with 30pF test load.

### PIN DESCRIPTION



Name	Function	Name	Function
A0~A18	Address Inputs	Vcc	Power
WE	Write Enable Input	Vss	Ground
CS	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
OE	Output Enable Input		

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Commercial Products(0~70°C)		Industrial Products(-40~85°C)		Automotive Products(-40~125°C)	
Part Name	Function	Part Name	Function	Part Name	Function
K6X4008T1F-GB55 <sup>1)</sup>	32-SOP, 55ns, LL	K6X4008T1F-GF55 <sup>1)</sup>	32-SOP, 55ns, LL	K6X4008T1F-GQ70	32-SOP, 70ns, L
K6X4008T1F-GB70	32-SOP, 70ns, LL	K6X4008T1F-GF70	32-SOP, 70ns, LL	K6X4008T1F-GQ85	32-SOP, 85ns, L
K6X4008T1F-GB85	32-SOP, 85ns, LL	K6X4008T1F-GF85	32-SOP, 85ns, LL	K6X4008T1F-YQ70	32-sTSOP1-F, 70ns, L
K6X4008T1F-YB55 <sup>1)</sup>	32-sTSOP1-F, 55ns, LL	K6X4008T1F-YF55 <sup>1)</sup>	32-sTSOP1-F, 55ns, LL	K6X4008T1F-YQ85	32-sTSOP1-F, 85ns, L
K6X4008T1F-YB70	32-sTSOP1-F, 70ns, LL	K6X4008T1F-YF70	32-sTSOP1-F, 70ns, LL	K6X4008T1F-VQ70	32-TSOP2-F, 70ns, L
K6X4008T1F-YB85	32-sTSOP1-F, 85ns, LL	K6X4008T1F-YF85	32-sTSOP1-F, 85ns, LL	K6X4008T1F-VQ85	32-TSOP2-F, 85ns, L
K6X4008T1F-VB55 <sup>1)</sup>	32-TSOP2-F, 55ns, LL	K6X4008T1F-VF55 <sup>1)</sup>	32-TSOP2-F, 55ns, LL		
K6X4008T1F-VB70	32-TSOP2-F, 70ns, LL	K6X4008T1F-VF70	32-TSOP2-F, 70ns, LL		
K6X4008T1F-VB85	32-TSOP2-F, 85ns, LL	K6X4008T1F-VF85	32-TSOP2-F, 85ns, LL		
K6X4008T1F-MB55 <sup>1)</sup>	32-TSOP2-R, 55ns, LL	K6X4008T1F-MF55 <sup>1)</sup>	32-TSOP2-R, 55ns, LL		
K6X4008T1F-MB70	32-TSOP2-R, 70ns, LL	K6X4008T1F-MF70	32-TSOP2-R, 70ns, LL		
K6X4008T1F-MB85	32-TSOP2-R, 85ns, LL	K6X4008T1F-MF85	32-TSOP2-R, 85ns, LL		

1. Operating voltage range is 3.0V~3.6V

## FUNCTIONAL DESCRIPTION

CS	OE	WE	I/O	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care (Must be in low or high state)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.2 to V <sub>CC</sub> +0.3(max. 3.9V)	V	-
Voltage on V <sub>CC</sub> supply relative to Vss	V <sub>CC</sub>	-0.2 to 3.9	V	-
Power Dissipation	P <sub>d</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	K6F4008T1F-B
		-40 to 85	°C	K6F4008T1F-F
		-40 to 125	°C	K6F4008T1F-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.0/3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.2 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.2 <sup>3)</sup>	-	0.6	V

Note:

- Commercial Product: T<sub>A</sub>=0 to 70°C, otherwise specified  
Industrial Product: T<sub>A</sub>=-40 to 85°C, otherwise specified  
Automotive Product: T<sub>A</sub>=-40 to 125°C, otherwise specified
- Overshoot: V<sub>CC</sub>+2.0V in case of pulse width ≤ 30ns
- Undershoot: -2.0V in case of pulse width ≤ 30ns
- Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

## DC AND OPERATING CHARACTERISTICS

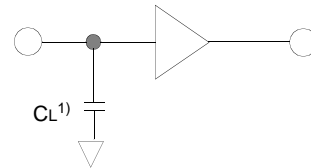
Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}=V_{IL}$ , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> , Read	-	-	2	mA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA $\overline{CS} \leq 0.2V$ , V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	-	3	mA	
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}=V_{IL}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	25	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}=V_{IH}$ , Other inputs = V <sub>IL</sub> or V <sub>IH</sub>	-	-	0.3	mA	
Standby Current (CMOS)	I <sub>SB1</sub>	$\overline{CS} \geq V_{CC}-0.2V$ , Other inputs=0~V <sub>CC</sub>	K6X4008T1F-B	-	-	10	μA
			K6X4008T1F-F	-	-	10	μA
			K6X4008T1F-Q	-	-	20	μA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V  
 Input rising and falling time: 5ns  
 Input and output reference voltage: 1.5V  
 Output load(see right):  $C_L=100\text{pF}+1\text{TTL}$   
 $C_L^1=30\text{pF}+1\text{TTL}$

1. 55ns, 70ns product



1. Including scope and jig capacitance

## AC CHARACTERISTICS

( $V_{CC}=2.7\sim 3.6\text{V}$ , Commercial product:  $T_A=0$  to  $70^\circ\text{C}$ , Industrial product:  $T_A=-40$  to  $85^\circ\text{C}$ , Automotive product:  $T_A=-40$  to  $125^\circ\text{C}$ )

Parameter List		Symbol	Speed Bins						Units
			55ns <sup>1)</sup>		70ns		85ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	55	-	70	-	85	-	ns
	Address access time	t <sub>AA</sub>	-	55	-	70	-	85	ns
	Chip select to output	t <sub>CO</sub>	-	55	-	70	-	85	ns
	Output enable to valid output	t <sub>OE</sub>	-	25	-	35	-	40	ns
	Chip select to low-Z output	t <sub>LZ</sub>	10	-	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	0	20	0	25	0	25	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	20	0	25	0	25	ns
	Output hold from address change	t <sub>OH</sub>	10	-	10	-	10	-	ns
Write	Write cycle time	t <sub>WC</sub>	55	-	70	-	85	-	ns
	Chip select to end of write	t <sub>CW</sub>	45	-	60	-	70	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	45	-	60	-	70	-	ns
	Write pulse width	t <sub>WP</sub>	40	-	55	-	55	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	20	0	25	0	25	ns
	Data to write time overlap	t <sub>DW</sub>	25	-	30	-	35	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	0	-	ns
	End write to output low-Z	t <sub>OW</sub>	5	-	5	-	5	-	ns

1. Voltage range is 3.0V~3.6V for commercial and industrial product.

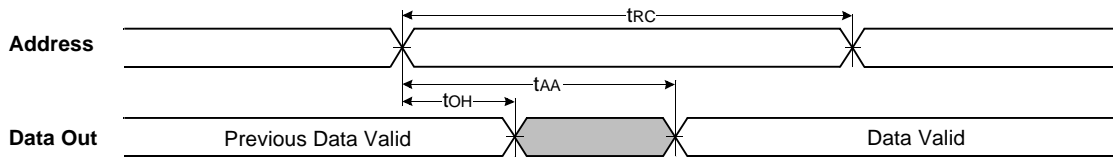
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ <sup>1)</sup>	Max	Unit	
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS} \geq V_{CC}-0.2\text{V}$	2.0	-	3.6	V	
Data retention current	I <sub>DR</sub>	$V_{CC}=3.0\text{V}, \overline{CS} \geq V_{CC}-0.2\text{V}$	K6X4008T1F-B	-	0.5	10	μA
			K6X4008T1F-F	-		10	μA
			K6X4008T1F-Q	-		20	μA
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms	
Recovery time	t <sub>RDR</sub>		5	-	-		

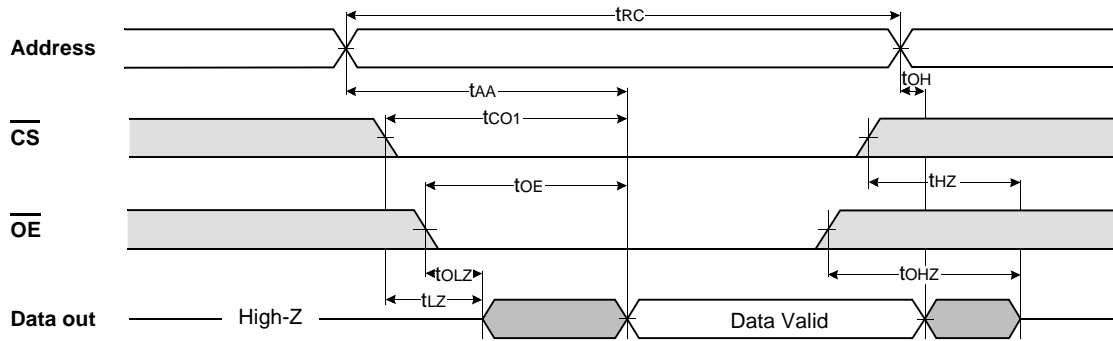
1. Typical values are measured at  $T_A = 25^\circ\text{C}$  and not 100% tested.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )



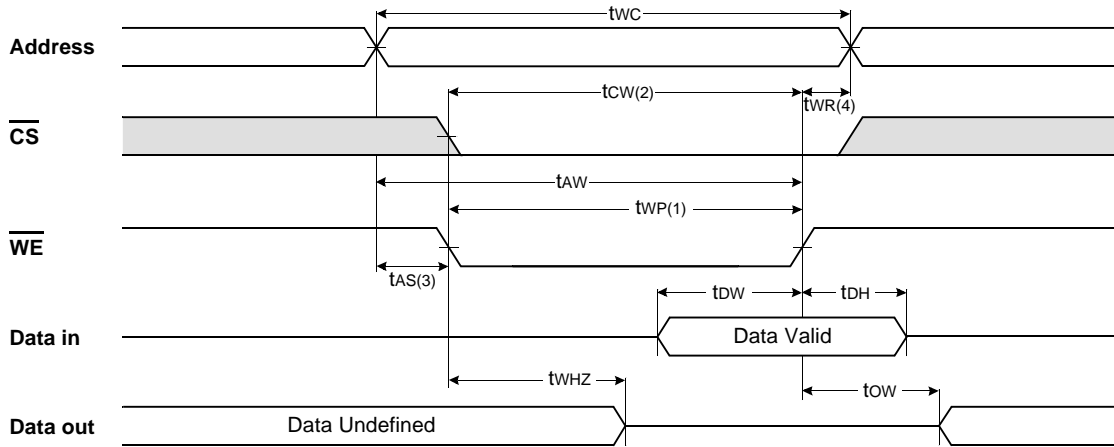
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



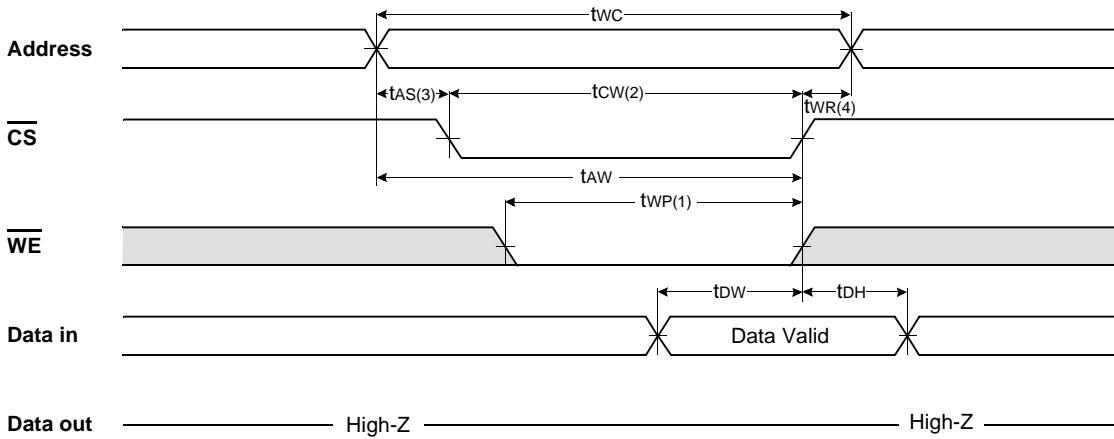
NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS}$  Controlled)

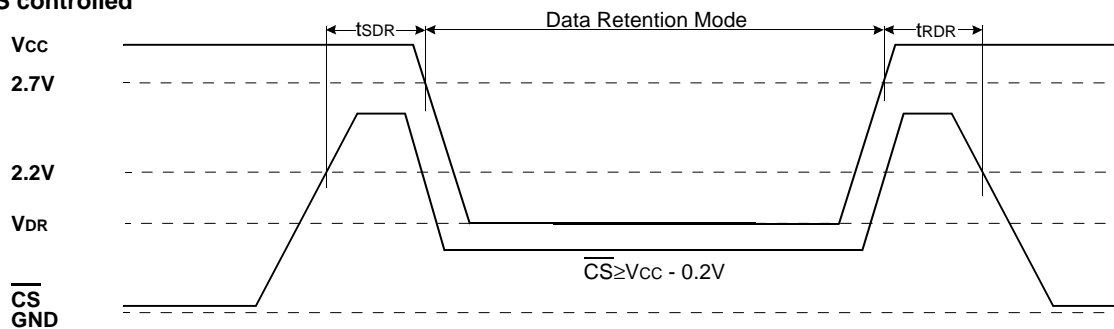


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}$  going Low and  $\overline{WE}$  going low : A write end at the earliest transition among CS going high and WE going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  is applied in case a write ends with  $\overline{CS}$  or  $\overline{WE}$  going high.

DATA RETENTION WAVE FORM

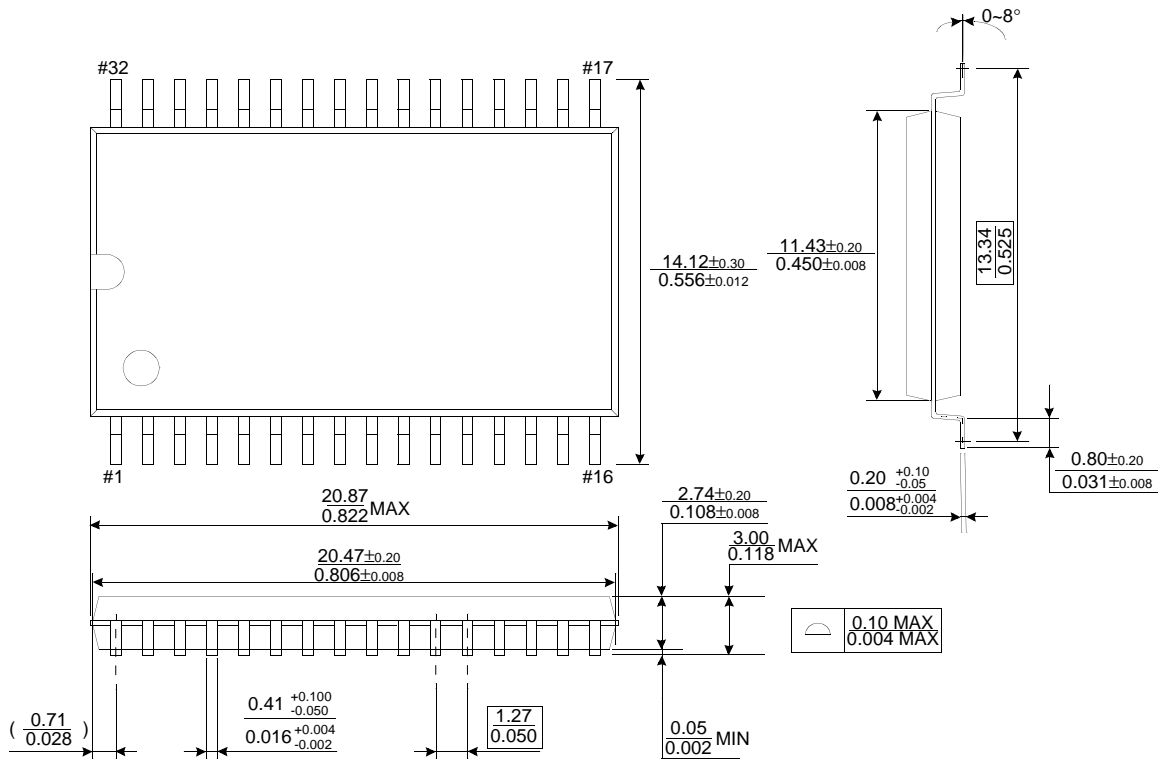
$\overline{CS}$  controlled



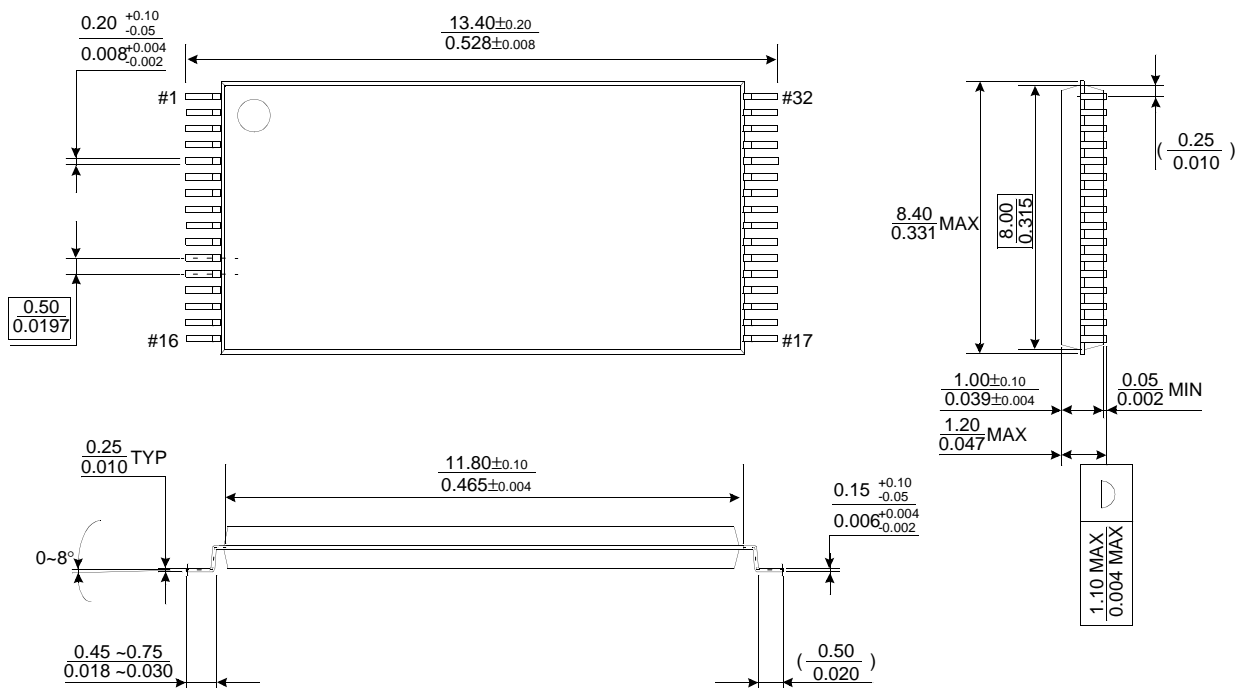
## PACKAGE DIMENSIONS

Units: millimeters(inches)

### 32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)



### 32 PIN SMALLER THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)

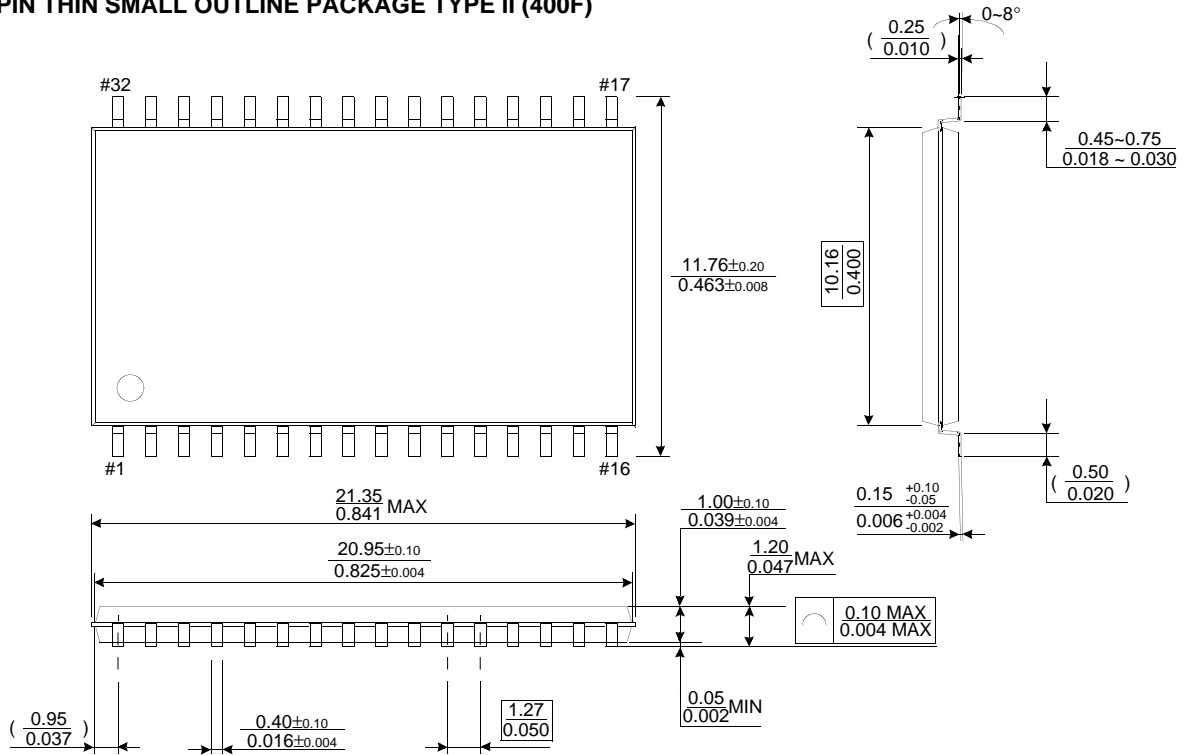




## PACKAGE DIMENSIONS

Units: millimeters(inches)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)

