HMC624LP4 / 624LP4E

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, DC - 6 GHz

Typical Applications

The HMC624LP4(E) is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

0.5 dB LSB Steps to 31.5 dB

High Input IP3: +55 dBm

Low Insertion Loss: 2.2 dB @ 3.5 GHz

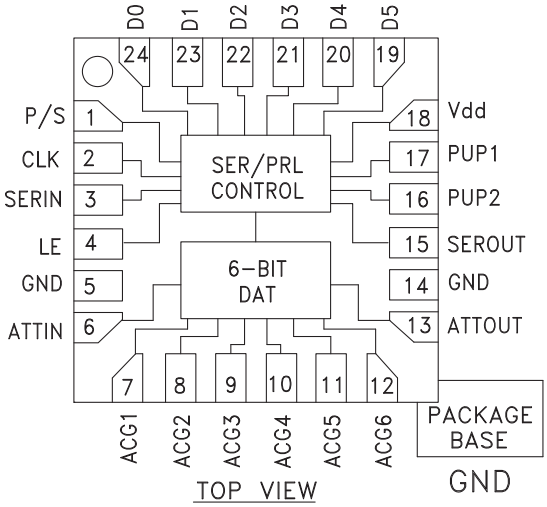
TTL/CMOS Compatible, Serial or Parallel Control

±0.25 dB Typical Step Error

Single +3V or +5V Supply

Compact 4x4mm SMT Package

Functional Diagram



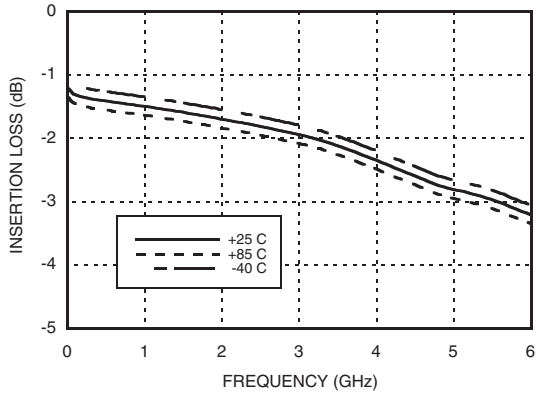
General Description

The HMC624LP4(E) is a broadband 6-bit GaAs IC Digital Attenuator in a low cost leadless SMT package. This versatile digital attenuator incorporates off-chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. The dual mode control interface is CMOS/TTL compatible, and accepts either a three wire serial input or a 6 bit parallel word. The HMC624LP4(E) also features a user selectable power up state and a serial output port for cascading other Hittite serial controlled components. The HMC624LP4(E) is housed in a RoHS compliant 4x4 mm QFN leadless package, and requires no external matching components.

Electrical Specifications, T_A = +25° C, with Vdd = +5V & Vctl = 0/+5V (Unless Otherwise Noted)

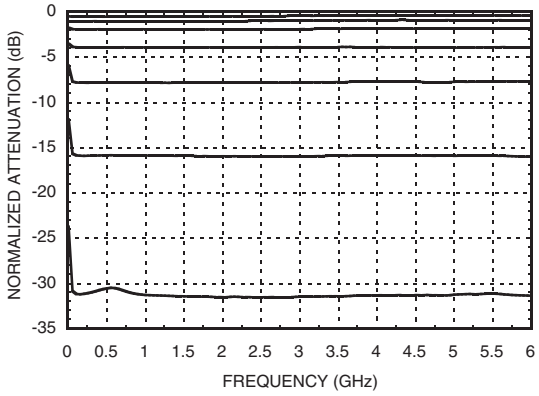
Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss	DC - 3.0 GHz 3.0 - 6.0 GHz		1.8 2.8	2.4 3.8	dB dB
Attenuation Range			31.5		dB
Return Loss (ATTIN, ATTOUT, All Atten. States)	DC - 6.0 GHz		15		dB
Attenuation Accuracy: (Referenced to Insertion Loss) All Attenuation States	DC - 0.8 GHz 0.8 - 6.0 GHz	± (0.10 + 5% of Atten. Setting) Max. ± (0.30 + 3% of Atten. Setting) Max.			dB dB
Input Power for 0.1 dB Compression	DC - 6.0 GHz		30		dBm
Input Third Order Intercept Point (Two-Tone Input Power= 10 dBm Each Tone)	DC - 6.0 GHz		55		dBm

Insertion Loss vs. Temperature [1]



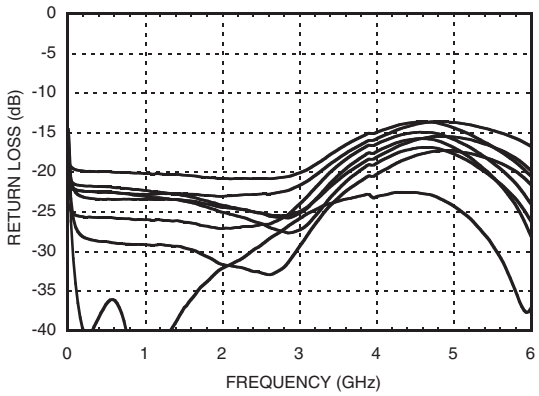
Normalized Attenuation [1]

(Only Major States are Shown)



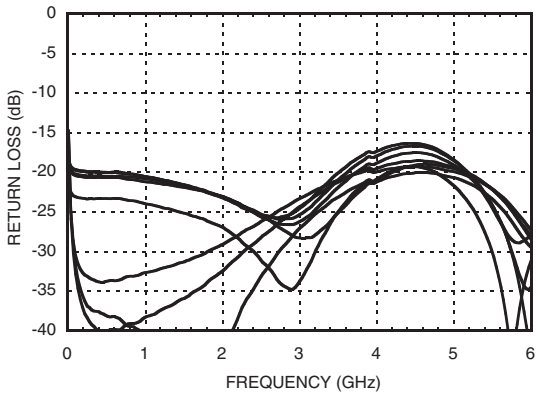
Input Return Loss [1]

(Only Major States are Shown)

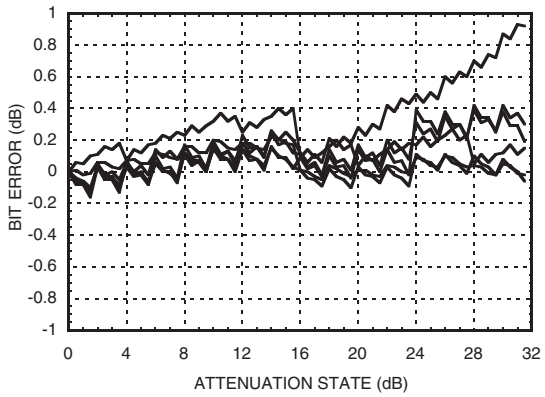


Output Return Loss [1]

(Only Major States are Shown)

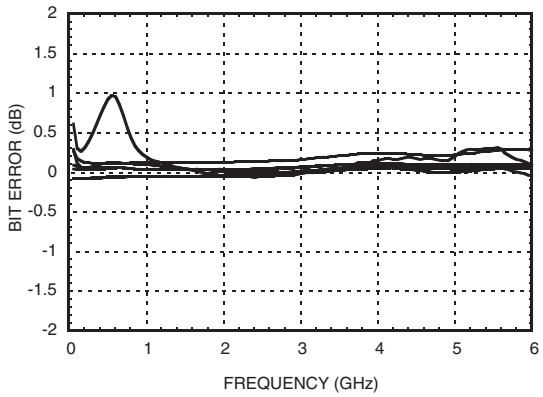


Bit Error vs. Attenuation State [2]



Bit Error vs. Frequency [2]

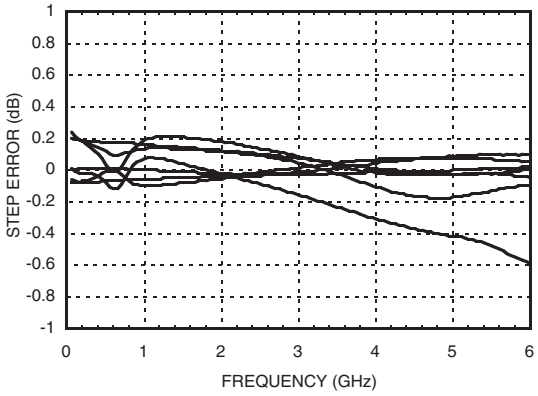
(Only Major States are Shown)



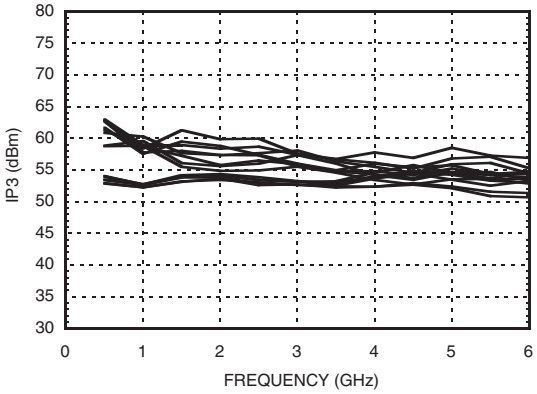
[1] Data taken with bias tees on input and output RF ports.

[2] C1, C6 = 330pF

Worst Case Step Error Between Successive Attenuation States [2]



IP3 vs. Temperature [2]

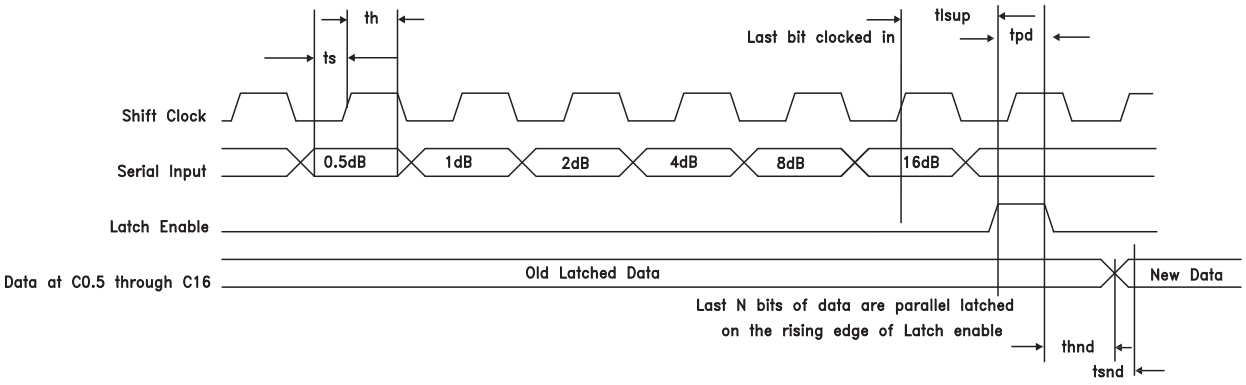


Serial Mode

The serial mode is enabled then P/S is set to high. Data is entered LSB first and after the 6th shift clock cycle the LE (Latch Enable) is pulsed High and then Low. See timing diagram below for reference.

Timing Diagram

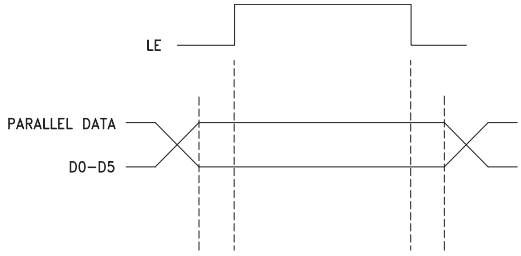
Serial data is shifted in on the rising edge of the Shift Clock, LSB first, and is latched on the rising edge of Latch Enable.



Timing

Parameter	Symbol	Vdd = +5V (Typ.)	Units
Serial Input Setup Time	ts	20	ns
Hold Time from Serial Input to Shift Clock	th	20	ns
Setup Time from Shift Clock to Latch Enable	tlsup	40	ns
Propagation Delay	tpd	10	ns
Setup Time for New Data	tsnd	10	ns

Timing Diagram (Latched Parallel Mode)



Parallel Mode (Direct Parallel Mode & Latched Parallel Mode)

Direct Parallel Mode - The attenuation state is changed by the Control Voltage Inputs directly. The LE (Latch Enable) must be at a logic high to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the Control Voltage Inputs and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram below for reference.

Power-Up States

Using the Parallel PUP truth table the attenuator can be turned on at a specific attenuation state. By using the PUP1 and PUP2 line four different attenuation states can be selected. It can also be used in the Direct Parallel Mode using the Control Voltage Inputs to select attenuation values.

Parallel PUP Truth Table

P/S	LE	PUP2	PUP1	Attenuation State
0	0	0	0	31.5 dB
0	0	1	0	24 dB
0	0	0	1	16 dB
0	0	1	1	8 dB
0	1	X	X	0.5 to 31.5 dB

Note: Power-Up with LE= 1 provides normal parallel operation with D0 - D5, and PUP1 and PUP2 are not active.

Absolute Maximum Ratings

RF Input Power (DC - 6 GHz) [1]	27 dBm (T = +85 °C)
Digital Inputs (Reset, Shift Clock, Latch Enable & Serial Input)	-1.5V to (Vdd +1.5V) Vdc
Bias Voltage (Vdd)	5.6 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 9.8 mW/°C above 85 °C) [1]	0.635 W
Thermal Resistance	102 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

[1] At max gain settling

Truth Table

Control Voltage Input						Attenuation State
D5	D4	D3	D2	D1	D0	
High	High	High	High	High	High	Reference I.L.
High	High	High	High	High	Low	0.5 dB
High	High	High	High	Low	High	1 dB
High	High	High	Low	High	High	2 dB
High	High	Low	High	High	High	4 dB
High	Low	High	High	High	High	8 dB
Low	High	High	High	High	High	16 dB
Low	Low	Low	Low	Low	Low	31.5 dB
Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.						

Bias Voltage

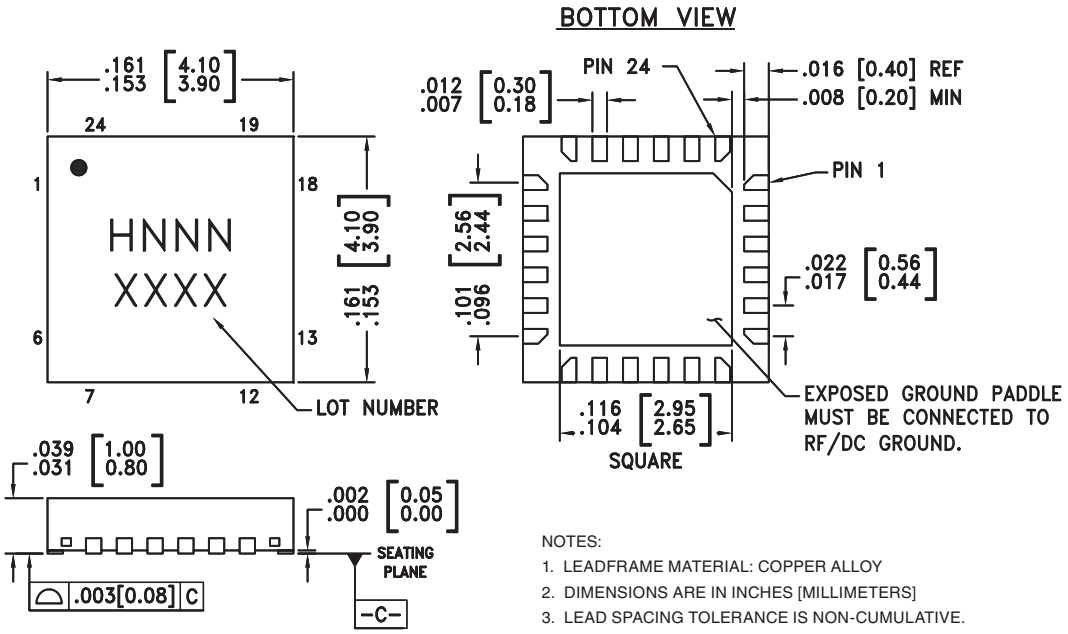
Vdd (Vdc)	Idd (Typ.) (mA)
3	1.8
5	2.0

TTL/CMOS Control Voltage

State	Vdd= +3V or +5V
Low	0 to 0.8V
High	2.0V to Vdd

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

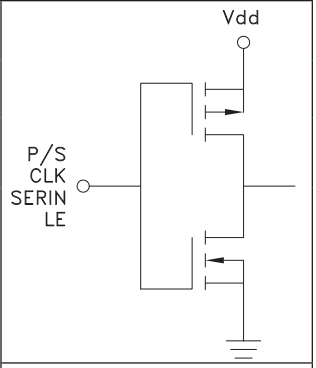
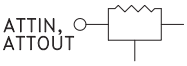
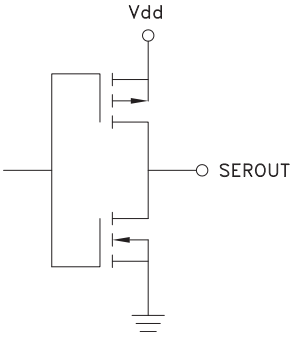
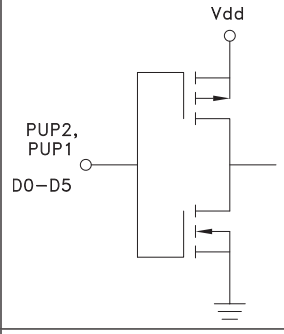
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

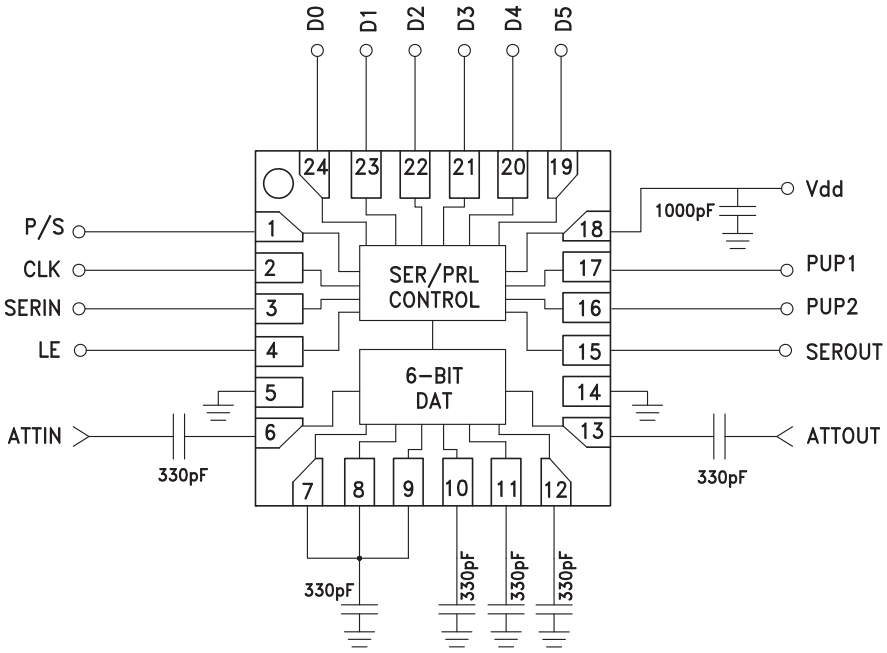
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC624LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H624 XXXX
HMC624LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H624 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

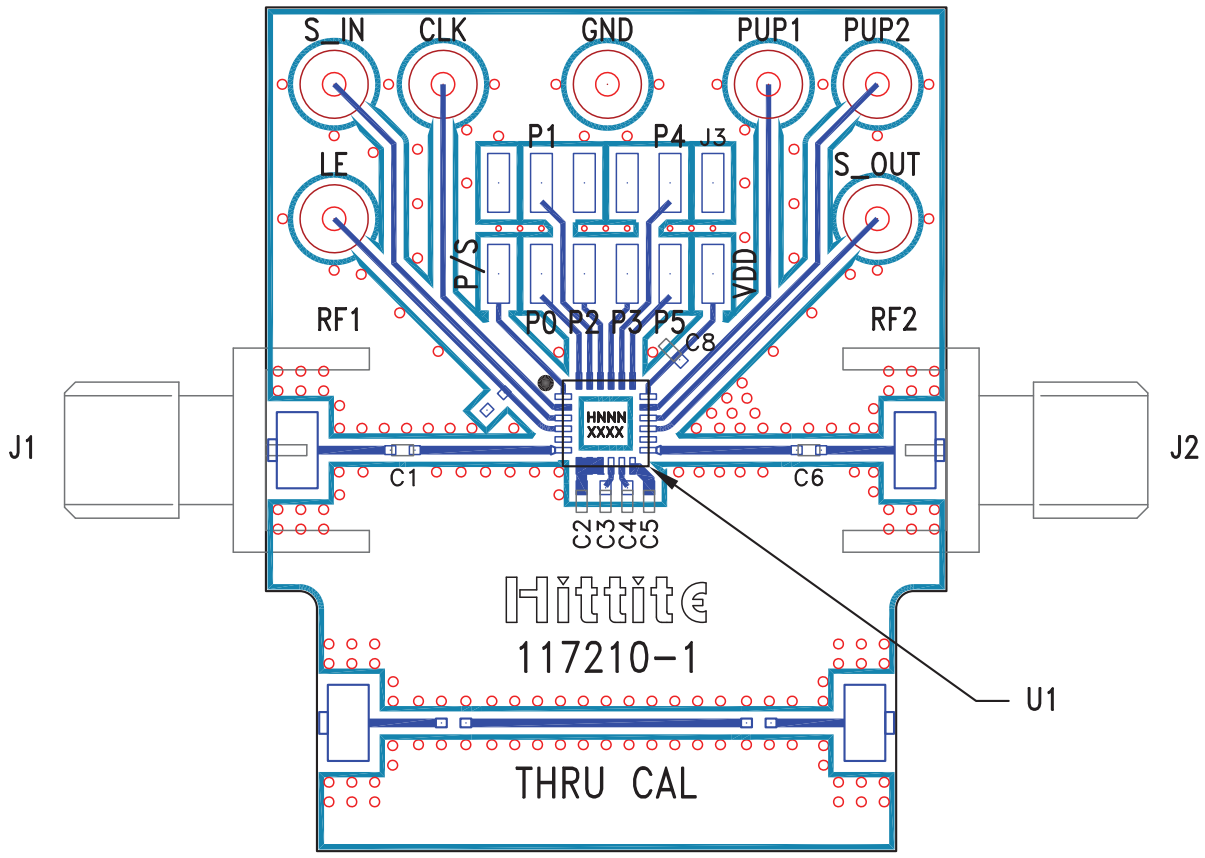
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	P/S	See truth table, control voltage table and timing diagram.	
2	CLK		
3	SERIN		
4	LE		
5, 14	GND	These pins and package bottom must be connected to RF/DC ground.	
6, 13	ATTIN, ATTOUT	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
7 - 12	ACG1 - ACG6	External capacitors to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	
15	SEROUT	Serial input data delayed by 6 clock cycles.	
16, 17 19 - 24	PUP2, PUP1 D5, D4, D3, D2, D1, D0	See truth table, control voltage table and timing diagram.	
18	Vdd	Supply voltage	

Application Circuit



Evaluation PCB



List of Materials for Evaluation PCB 117212 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3	14 Pin DC Connector
C1, C6	330 pF Capacitor, 0402 Pkg.
C7, C8	1000 pF Capacitor, 0402 Pkg.
U1	HMC472LP4(E) Digital Attenuator
PCB [2]	117210 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Notes: